

# LM2724A

*LM2724A High Speed 3A Synchronous MOSFET Driver*



Literature Number: SNVS242A

## High Speed 3A Synchronous MOSFET Driver

### General Description

The LM2724A is a dual N-channel MOSFET driver which can drive both the top and bottom MOSFETs in a push-pull structure simultaneously. The LM2724A takes a logic input and splits it into two complimentary signals with a typical 20ns dead time in between. The built-in cross-conduction protection circuitry prevents the top and bottom MOSFETs from turning on simultaneously. With a bias voltage of 5V, the peak sourcing and sinking current for each driver of the LM2724A is about 3A. Input UVLO (Under-Voltage-Lock-Out) ensures that all the driver outputs stay low until the supply rail exceeds the power-on threshold during system power on, or after the supply rail drops below power-on threshold by a specified hysteresis during system power down. The cross-conduction protection circuitry detects both driver outputs and will not turn on a driver until the other driver output is low. The top gate voltage needed by the top MOSFET is obtained through an external boot-strap structure. When not switching, the LM2724A only draws up to 195µA from the 5V rail. The syn-

chronization operation of the bottom MOSFET can be disabled by pulling the SYNC pin to ground.

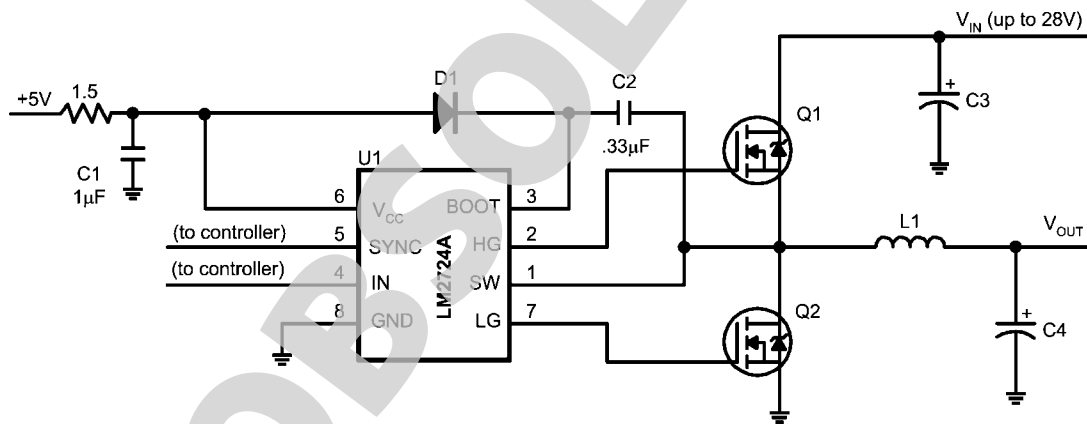
### Features

- Shoot-through protection
- Input Under-Voltage-Lock-Out
- 3A peak driving current
- 195µA quiescent current
- 28V input voltage in buck configuration
- SO-8 and LLP packages

### Applications

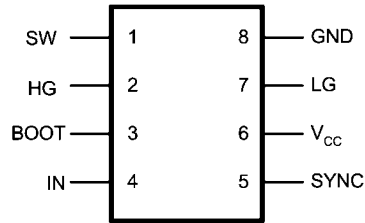
- High Current DC/DC Power Supplies
- High Input Voltage Switching Regulators
- Fast Transient Microprocessors
- Notebook Computers

### Typical Application

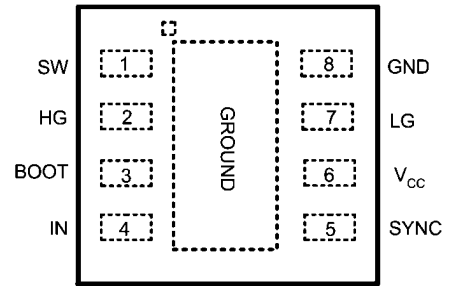


20073501

## Connection Diagram



8-Lead SO (NS Package # M08A)  
 $\theta_{JA} = 172^{\circ}\text{C/W}$



8-Lead LLP (NS Package # LDC08A)  
 $\theta_{JA} = 39^{\circ}\text{C/W}$

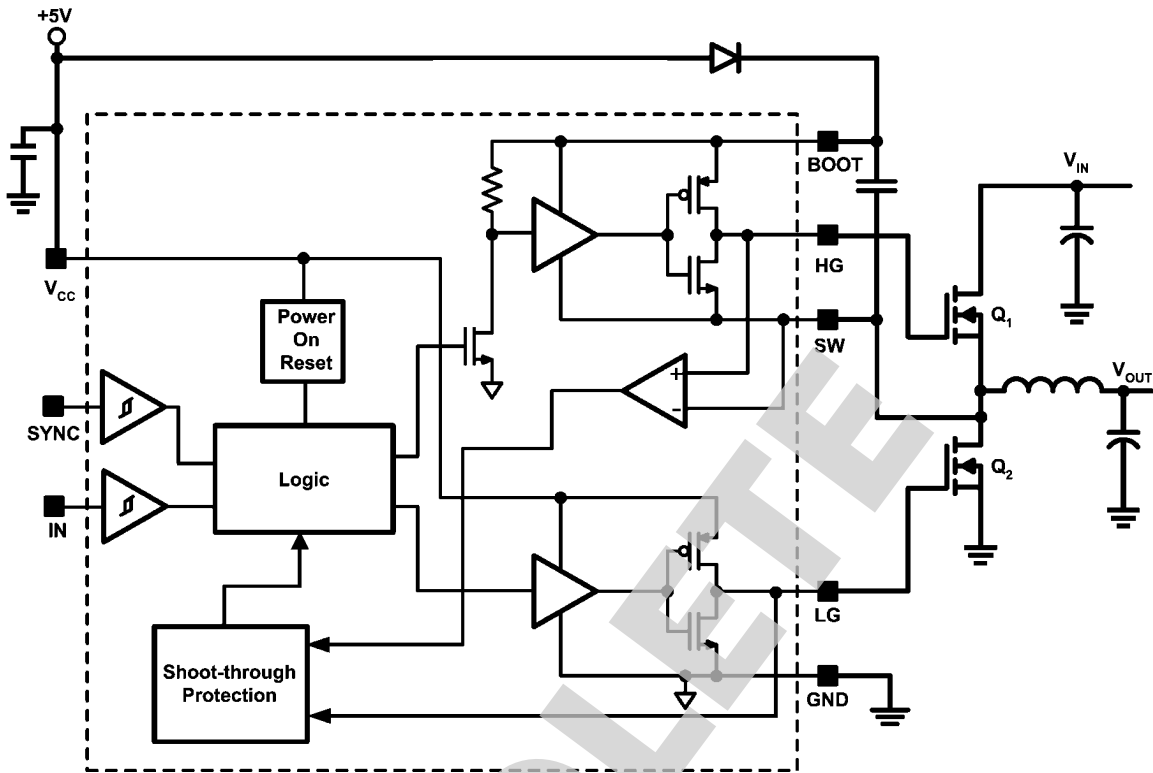
## Ordering Information

Order Number	Size	NSC Package Drawing	Supplied As
LM2724AM	SO-8	M08A	95 Units/Rail
LM2724AMX			2500 Units/Reel
LM2724ALD	LDC08A	LDC08A	1000 Units/Rail
LM2724ALDX			4500 Units/Reel

## Pin Descriptions

Pin	Name	Function
1	SW	Top driver return. Should be connected to the common node of top and bottom FETs
2	HG	Top gate drive output. Should be connected to the top FET gate.
3	BOOT	Bootstrap. Accepts a bootstrap voltage for powering the high-side driver
4	IN	Accepts a logic control signal
5	SYNC	Bottom gate enable
6	$V_{CC}$	Connect to +5V supply
7	LG	Bottom gate drive output. Should be connected to the bottom FET gate.
8	GND	Ground

# Block Diagram



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## Absolute Maximum Ratings *(Note 1)*

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

$V_{CC}$	7V
BOOT to SW	7V
BOOT to GND <i>(Note 2)</i>	35V
SW to GND <i>(Note 3)</i>	-2V to 30V
Junction Temperature	+150°C
Power Dissipation <i>(Note 4)</i>	720mW (SO-8) 3.2W (LLP-8)

Storage Temperature	-65°C to 150°C
ESD Susceptibility Human Body Model <i>(Note 5)</i>	2.0 kV
Soldering Time, Temperature	10sec., 300°C

## Operating Ratings *(Note 1)*

$V_{CC}$	4.3V to 6.8V
Junction Temperature Range	-40°C to 125°C

## Electrical Characteristics LM2724A

$V_{CC} = \text{BOOT} = \text{SYNC} = 5\text{V}$ ,  $\text{SW} = \text{GND} = 0\text{V}$ , unless otherwise specified. Typicals and limits appearing in plain type apply for  $T_A = T_J = +25^\circ\text{C}$ . Limits appearing in **boldface** type apply over the entire operating temperature range.

Symbol	Parameter	Condition	Min	Typ	Max	Units
<b>POWER SUPPLY</b>						
$I_{q\_op}$	Operating Quiescent Current	IN = 0V		145	<b>195</b>	$\mu\text{A}$
<b>TOP DRIVER</b>						
	Peak Pull-Up Current			3.0		A
	Pull-Up Rds_on	$I_{\text{BOOT}} = I_{\text{HG}} = 0.3\text{A}$		1.2		$\Omega$
	Peak Pull-down Current			-3.2		A
	Pull-down Rds_on	$I_{\text{SW}} = I_{\text{HG}} = 0.3\text{A}$		0.5		$\Omega$
$t_4$	Rise Time	Timing Diagram, $C_{\text{LOAD}} = 3.3\text{nF}$		17		ns
$t_6$	Fall Time			12		ns
$t_3$	Pull-Up Dead Time	Timing Diagram		19		ns
$t_5$	Pull-Down Delay	Timing Diagram, from IN Falling Edge		27		ns
<b>BOTTOM DRIVER</b>						
	Peak Pull-Up Current			3.2		A
	Pull-up Rds_on	$I_{\text{VCC}} = I_{\text{LG}} = 0.3\text{A}$		1.1		$\Omega$
	Peak Pull-down Current			3.2		A
	Pull-down Rds_on	$I_{\text{GND}} = I_{\text{LG}} = 0.3\text{A}$		0.6		$\Omega$
$t_8$	Rise Time	Timing Diagram, $C_{\text{LOAD}} = 3.3\text{nF}$		17		ns
$t_2$	Fall Time			14		ns
$t_7$	Pull-up Dead Time	Timing Diagram		22		ns
$t_1$	Pull-down Delay	Timing Diagram		13		ns
<b>LOGIC</b>						
$V_{\text{uvlo\_up}}$	$V_{CC}$ Under-Voltage-Lock-Out Upper Threshold	$V_{CC}$ rises from 0V toward 5V			<b>4</b>	V
$V_{\text{uvlo\_dn}}$	$V_{CC}$ Under-Voltage-Lock-Out Lower Threshold	$V_{CC}$ falls from 5V toward 0V	<b>2.5</b>			V
$V_{\text{uvlo\_hys}}$	$V_{CC}$ Under-Voltage-Lock-Out Hysteresis	$V_{CC}$ falls from 5V toward 0V		0.8		V
$V_{\text{IH\_SYNC}}$	SYNC Pin High Input		<b>55%</b>			$V_{CC}$
$V_{\text{IL\_SYNC}}$	SYNC Pin Low Input				<b>25%</b>	
$I_{\text{leak\_SYNC}}$	SYNC Pin Leakage Current	SYNC = 5V, Sink Current			<b>2</b>	$\mu\text{A}$
		SYNC = 0V, Source Current			<b>10</b>	
$I_{\text{leak\_IN}}$	IN Pin Leakage Current	IN = 0V, Source Current			<b>2</b>	$\mu\text{A}$
		IN = 5V, Sink Current			<b>10</b>	

Symbol	Parameter	Condition	Min	Typ	Max	Units
$t_{on\_min1}$	Minimum Positive Pulse Width at IN Pin (Note 6)			160		ns
$t_{on\_min2}$	Minimum Positive Pulse Width at IN Pin for HG to Respond (Note 7)			45		
$t_{on\_min3}$	Minimum Positive Pulse Width at IN Pin for LG to Respond (Note 8)			10		
$t_{off\_min1}$	Minimum Negative Pulse Width at IN Pin for LG to Respond (Note 9)			40		
$t_{off\_min2}$	Minimum Negative Pulse Width at IN Pin for HG to Respond (Note 10)			5		
$V_{IH\_IN}$	IN High Level Input Voltage	When IN pin goes high from 0V	55%			
$V_{IL\_IN}$	IN Low Level Input Voltage	When IN pin goes low from 5V			25%	

**Note 1: Absolute Maximum Ratings** are limits beyond which damage to the device may occur. **Operating ratings** are conditions under which the device operates correctly. The guaranteed specifications apply only for the listed test conditions. Some performance characteristics may degrade when the part is not operated under listed conditions.

**Note 2:** If BOOT voltage exceeds this value, the ESD structure will degrade.

**Note 3:** The SW pin can have -2V to -0.5V applied for a maximum duty cycle of 10% with a maximum period of 1 second. There is no duty cycle or maximum period limitation for a SW pin voltage range of -0.5V to 30V.

**Note 4:** Maximum allowable power dissipation is a function of the maximum junction temperature,  $T_{JMAX}$ , the junction-to-ambient thermal resistance,  $\theta_{JA}$ , and the ambient temperature,  $T_A$ . The maximum allowable power dissipation at any ambient temperature is calculated using:  $P_{MAX} = (T_{JMAX} - T_A) / \theta_{JA}$ . The junction-to-ambient thermal resistance,  $\theta_{JA}$ , for LM2724A is 172°C/W. For a  $T_{JMAX}$  of 150°C and  $T_A$  of 25°C, the maximum allowable power dissipation is 0.7W. The  $\theta_{JA}$ , for LM2724A LLP package is 39°C/W. For a  $T_{JMAX}$  of 150°C and  $T_A$  of 25°C, the maximum allowable power dissipation is 3.2W.

**Note 5:** ESD machine model susceptibility is 200V.

**Note 6:** If the positive pulse width at IN pin is below this value but above  $t_{on\_min2}$ , the pulse is internally stretched to  $t_{on\_min1}$ , so the HG width will be a constant value.

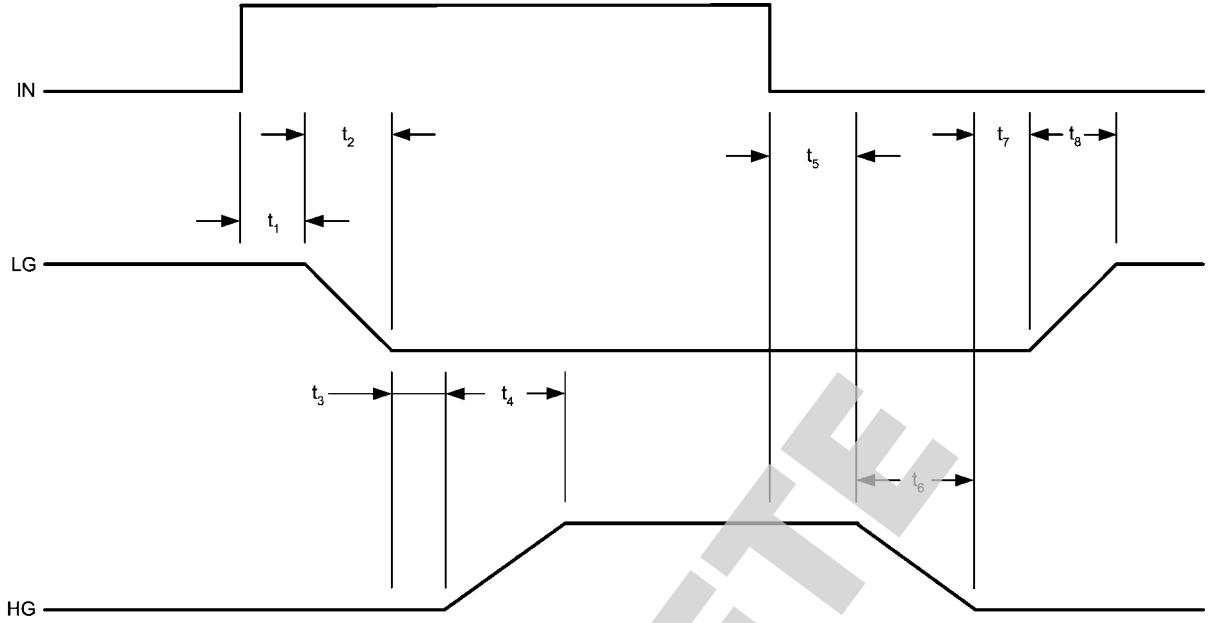
**Note 7:** If the positive pulse width at IN pin is below this value but above  $t_{on\_min3}$ , then HG stops responding while LG still responds to the pulse.

**Note 8:** If the positive pulse width at IN pin is below this value, the pulse will be completely ignored. Neither HG or LG will respond to it.

**Note 9:** If the negative pulse width at IN pin is below this value but above  $t_{off\_min2}$ , then LG stops responding while HG still responds.

**Note 10:** If the negative pulse width at IN pin is below this value, the pulse will be completely ignored. Neither HG or LG will respond to it.

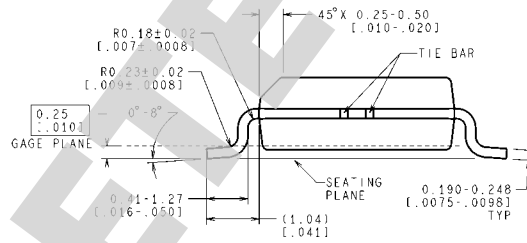
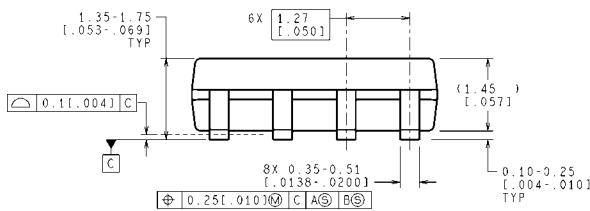
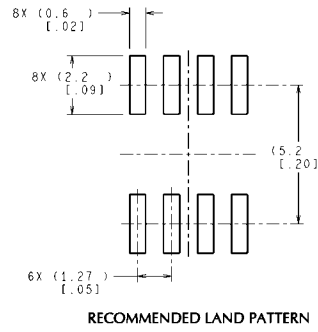
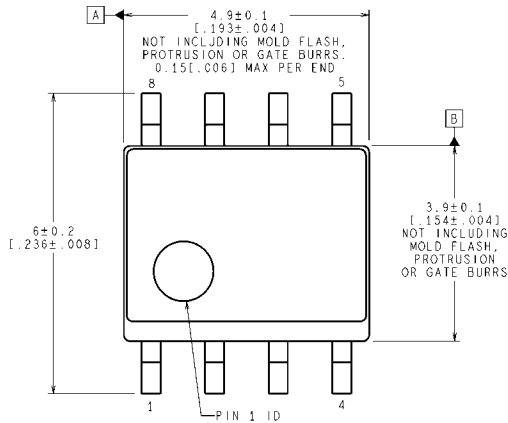
### Timing Diagram



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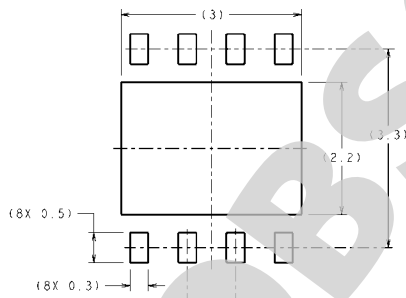
**Physical Dimensions** inches (millimeters) unless otherwise noted



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VALUES IN [ ] ARE INCHES  
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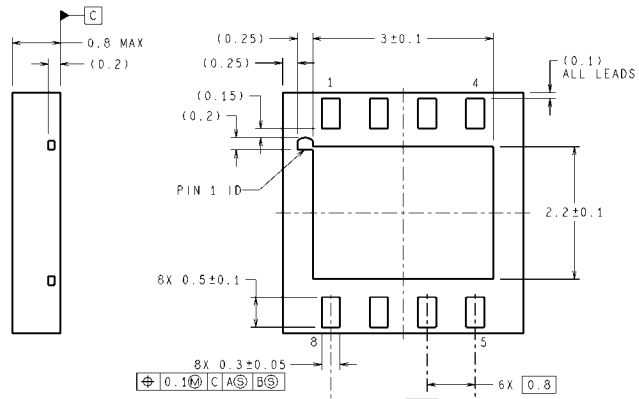
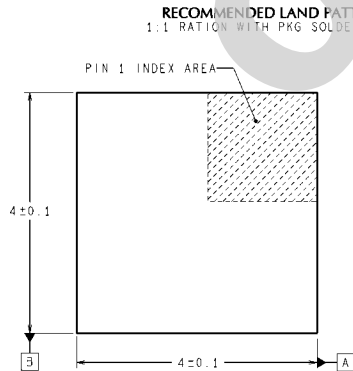
M08A (Rev M)

**8-Lead Small Outline Package**  
Order Number LM2724AM, LM2724AMX  
NS Package Number M08A



**RECOMMENDED LAND PATTERN**  
1:1 RATIO WITH PKG SOLDER PADS

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LDC08A (Rev B)

**8-Lead LLP Package**  
Order Number LM2724ALD, LM2724ALDX  
NS Package Number LDC08A



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