



# Hybrid, Tracking Resolver-to-Digital Converters

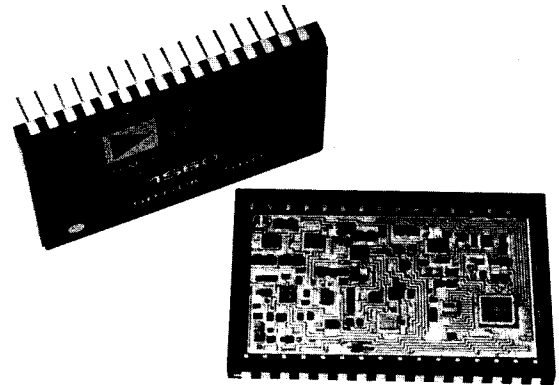
1S10/1S20/1S40/1S60/1S61

## FEATURES

- Low Cost
- 32-Pin Hybrid
- High Tracking Rate 170rps at 12 Bits
- Velocity Output
- DC Error Output
- Logic Outputs for Extension Pitch Counter
- Military Temperature Range Available

## APPLICATIONS

- Numerical Control of Machine Tools
- Robotics
- Avionics



## GENERAL DESCRIPTION

The 1S10/20/40/60/61 are a series of low cost hybrid converters with a high tracking rate and all essential features for numerically controlled machine applications. These converters are housed in a 32-pin DIL package.

The 1S10/20/40/60/61 convert resolver format input signals into a parallel natural binary digital word. Typically, these signals would be obtained from a brushless resolver and the resolver/converter combination gives a parallel absolute angular output word similar to that provided by an absolute encoder. The ratiometric conversion principle of the 1S10/20/40/60/61 series ensures high noise immunity and tolerance of lead length when the converter is at a distance from the resolver.

The output word is in three-state digital logic form with a high and low byte enable input so that the converter can communicate with an 8- or 16-bit digital highway. In this series there are 10-, 12-, 14- and two 16-bit resolution (identifiable by accuracy) models available.

Repeatability, under constant temperature conditions, is 1LSB for the 1S10/20/40/60 and 2LSB for the 1S61.

The 1S10/20/40/60/61 are available with three\* frequency options covering the range 400Hz to 10kHz.

### Models Available

Five models are available in this range and three\* frequency options for each model.

- 1S10 is a 10-bit up to 680 revolutions per second.
- 1S20 is a 12-bit up to 170 revolutions per second.
- 1S40 is a 14-bit up to 42.5 revolutions per second.
- 1S60 is a 16-bit up to 10.5 revolutions per second.
- 1S61 is a 16-bit up to 10.5 revolutions per second.

\*1S10 has only two frequency options.

## APPLICATIONS/USER BENEFITS

The 1S10/20/40/60/61 has been specifically designed for the numerically controlled machine and robot industry as well as military and aerospace multi-turn applications. Using the type 2 servo loop tracking principle ideally suits these converters to the electrically noisy environment found in these applications.

By using hybrid construction techniques, small size, low power and high reliability are further benefits offered by these converters. This small size with the three-state digital outputs makes these converters ideal for multichannel operation.

The layout of the connections simplifies the parallel connection to a digital highway.

The provision of the digital outputs of DIRECTION and RIPPLE CLOCK allow simple extension counters for multi-pitch operation to be implemented.

Analog outputs of velocity and dc error for control loop stabilization and bite (built in test) provide two more features required in these applications.

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# SPECIFICATIONS (typical @ +25°C, unless otherwise specified)

| Models  | 1S10   | 1S20    | 1S40    | 1S60    | 1S61    | Units             |
|---|--|---------|---------|---------|---------|-------------------|
| RESOLUTION  | 10   | 12      | 14      | 16      | 16      | Bits              |
| ACCURACY (max) <sup>1</sup>                                       |  |         |         |         |         |                   |
| 5YO   | ± 25   | ± 8.5   | ± 5.3   | ± 4.0   | ± 10    | arc-mins          |
| 4YO   | ± 25   | ± 8.5   | ± 5.3   | ± 2.6   | ± 4.0   | arc-mins          |
| REPEATABILITY <sup>2</sup>  |  |         |         |         |         |                   |
| At Constant Temp  | ± 1  | *       | *       | *       | ± 2     | LSB               |
| Additional over Temp Range  |  |         |         |         |         |                   |
| 5YO Option  | ± 2  | *       | *       | *       | ± 4     | arc-mins          |
| 4YO Option  | ± 2  | *       | *       | ± 1     | ± 2.5   | arc-mins          |
| SIGNAL AND REFERENCE FREQUENCY <sup>3</sup>                       | 2.6k-10k   | 400-10k | **      | **      | **      | Hz                |
| DIGITAL OUTPUT  | Parallel natural binary  |         |         |         |         |                   |
| Max Load  | 20   | *       | *       | *       | *       | LSTTL             |
| TRACKING RATE (min)   |  |         |         |         |         |                   |
| 400Hz-2.6kHz  | -  | 50      | 12.5    | 3.0     | 3.0     | rps               |
| 2.6kHz-5kHz   | 360  | 90      | 22.5    | 5.5     | 5.5     | rps               |
| 5kHz-10kHz  | 680  | 170     | 42.5    | 10.5    | 10.5    | rps               |
| SETTLING TIME (179° Step)   |  |         |         |         |         |                   |
| 400Hz-2.6kHz  | -  | 90      | 180     | 350     | 350     | ms                |
| 2.6kHz-5kHz   | 20   | 40      | 50      | 130     | 130     | ms                |
| 5kHz-10kHz  | 10   | 20      | 25      | 60      | 60      | ms                |
| ACCELERATION CONSTANT (K <sub>a</sub> )                           |  |         |         |         |         |                   |
| 400Hz-2.6kHz  | -  | 38,000  | 9,500   | 9,500   | 9,500   | sec <sup>-2</sup> |
| 2.6kHz-5kHz   | 1,150,000  | 144,000 | 144,000 | 144,000 | 144,000 | sec <sup>-2</sup> |
| 5kHz-10kHz  | 5,700,000  | 713,000 | 713,000 | 713,000 | 713,000 | sec <sup>-2</sup> |
| SIGNAL VOLTAGE  | 2.0(± 10%)   | *       | *       | *       | *       | V <sub>rms</sub>  |
| SIGNAL INPUT IMPEDANCE  | > 10   | *       | *       | *       | *       | MΩ                |
| REFERENCE VOLTAGE   | 2.0(+ 50%/- 20%)   | *       | *       | *       | *       | V <sub>rms</sub>  |
| REFERENCE INPUT IMPEDANCE   | 125  | *       | *       | *       | *       | kΩ                |
| ALLOWABLE PHASE SHIFT <sup>4</sup><br>(Signal to Reference)       | ± 10   | *       | *       | *       | *       | Degrees           |
| BUSY OUTPUT <sup>5</sup>  | Logic "Hi" when Busy   | *       | *       | *       | *       |                   |
| Max Load  | 20   | *       | *       | *       | *       | LSTTL             |
| BUSY WIDTH  | 450  | *       | *       | *       | *       | ns                |
| ENABLE INPUTS   | Logic "Lo" to ENABLE   | *       | *       | *       | *       |                   |
| Load  | 1  | *       | *       | *       | *       | LSTTL             |
| ENABLE AND DISABLE TIMES  | 120(typ)<br>220(max)   | *       | *       | *       | *       | ns                |
| INHIBIT INPUT   | Logic "Lo" to INHIBIT  | *       | *       | *       | *       |                   |
| Load  | 1  | *       | *       | *       | *       | LSTTL             |
| DIRECTION OUTPUT (DIR) <sup>5</sup>                               | Logic "Hi" when counting up<br>Logic "Lo" when counting down   | *       | *       | *       | *       |                   |
| Max Load  | 20   | *       | *       | *       | *       | LSTTL             |
| RIPPLE CLOCK <sup>5</sup>   | Negative pulse indicating when<br>internal counters change from all<br>"1's" to all "0's" or vice versa. | *       | *       | *       | *       |                   |
| Max Load  | 20   | *       | *       | *       | *       | LSTTL             |
| VELOCITY OUTPUT <sup>6</sup><br>(at specified min tracking rate). |  |         |         |         |         |                   |
| Polarity  | positive for increasing angle  | *       | *       | *       | *       | -                 |
| Output Voltage <sup>7</sup>                                       | ± 10   | *       | *       | *       | *       | V <sub>dc</sub>   |
| Accuracy  | ± 10   | *       | *       | *       | *       | % FSD             |
| Zero Offset   | ± 8  | *       | *       | *       | *       | mV                |
| DC ERROR OUTPUT VOLTAGE <sup>6</sup>                              | 160  | 40      | 10      | 2.5     | 2.5     | mV/LSB            |
| POWER SUPPLIES <sup>8</sup>                                       |  |         |         |         |         |                   |
| +V <sub>S</sub>   | + 11.5 to + 16   | *       | *       | *       | *       | V                 |
| -V <sub>S</sub>   | - 11.5 to - 16   | *       | *       | *       | *       | V                 |
| +5V   | + 4.75 to + 5.25   | *       | *       | *       | *       | V                 |
| POWER SUPPLY CONSUMPTION <sup>7</sup>                             |  |         |         |         |         |                   |
| +V <sub>S</sub>   | 20, 30 (max)   | *       | *       | *       | *       | mA                |
| -V <sub>S</sub>   | 20, 30 (max)   | *       | *       | *       | *       | mA                |
| +5V   | 105, 125 (max)   | *       | *       | *       | *       | mA                |
| POWER DISSIPATION <sup>8</sup>                                    | 1.1, 1.5 (max)   | *       | *       | *       | *       | W                 |
| TEMPERATURE RANGE   |  |         |         |         |         |                   |
| Operating Option 5YO  | 0 to + 70  | *       | *       | *       | *       | °C                |
| Storage Option 5YO  | - 55 to + 125  | *       | *       | *       | *       | °C                |
| Operating Option 4YO  | - 55 to + 125  | *       | *       | *       | *       | °C                |
| Storage Option 4YO  | - 65 to + 150  | *       | *       | *       | *       | °C                |
| DIMENSIONS  |  |         |         |         |         |                   |
| Option 5YO  | 1.1 × 1.7 × 0.205(28 × 43.2 × 5.2)   | *       | *       | *       | *       | inches (mm)       |
| Option 4YO  | 1.14 × 1.74 × 0.28(29 × 44.2 × 4.6)  | *       | *       | *       | *       | inches (mm)       |
| WEIGHT  | 1(28)  | *       | *       | *       | *       | oz. (grms)        |

## NOTES

<sup>1</sup>Specified over the operating temperature range and for:

- ± 10% signal and + 50%/- 20% reference amplitude variation.
- 10% signal and reference harmonic distortion.
- ± 10% on frequency range of option.

<sup>2</sup>For 5YO design figure (not tested for). For 4YO worst case.

<sup>3</sup>See ordering information (last page).

<sup>4</sup>For no additional error with a static input, see "Dynamic Accuracy vs. Resolver Phase Shift".

<sup>5</sup>See timing diagram (Figure 3).

<sup>6</sup>These outputs should be connected via buffers or comparator inputs (max load 100pF).

<sup>7</sup>± V<sub>S</sub> = ± 15 volts.

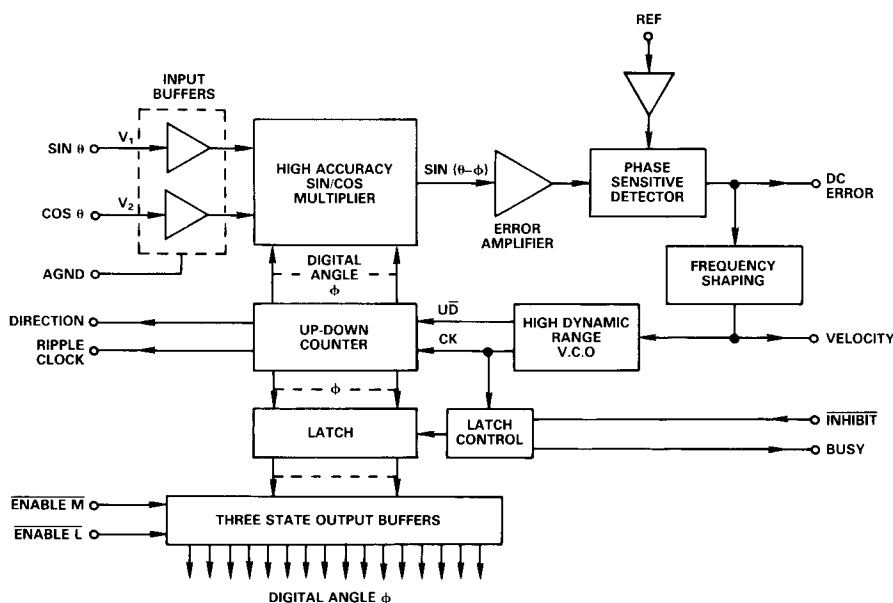
<sup>8</sup>Symmetry of the +V<sub>S</sub> and -V<sub>S</sub> power supplies must be within ± 5%.

\*Specifications same as 1S10.

\*\*Specifications same as 1S20.

Specifications subject to change without notice.

## FUNCTIONAL DIAGRAM



## BIT WEIGHT TABLE

| Bit Number | Weight in Degrees |
|------------|-------------------|
| 1 (MSB)    | 180.0000          |
| 2          | 90.0000           |
| 3          | 45.0000           |
| 4          | 22.5000           |
| 5          | 11.2500           |
| 6          | 5.6250            |
| 7          | 2.8125            |
| 8          | 1.4063            |
| 9          | 0.7031            |
| 10         | 0.3516            |
| 11         | 0.1758            |
| 12         | 0.0879            |
| 13         | 0.0440            |
| 14         | 0.0220            |
| 15         | 0.0110            |
| 16         | 0.0055            |

## THEORY OF OPERATION

The sine and cosine signals are applied to the signal input.

$$V_1 = K E_O \text{Sin } \omega t \text{ Sin } \theta$$

$$V_2 = K E_O \text{Sin } \omega t \text{ Cos } \theta$$

Where  $\theta$  is the angle of the resolver shaft or the distance through a particular pitch of the Inductosyn™

To understand the conversion process, then assume that the current word state of the up-down counter is  $\phi$ .

$V_1$  is multiplied by  $\text{Cos } \phi$  and  $V_2$  is multiplied by  $\text{Sin } \phi$  to give:

$$K E_O \text{Sin } \omega t \text{ Sin } \theta \text{ Cos } \phi$$

$$\text{and } K E_O \text{Sin } \omega t \text{ Cos } \theta \text{ Sin } \phi$$

These signals are subtracted by the error amplifier to give:

$$K' E_O \text{Sin } \omega t (\text{Sin } \theta \text{ Cos } \phi - \text{Cos } \theta \text{ Sin } \phi)$$

$$\text{or } K' E_O \text{Sin } \omega t \text{ Sin } (\theta - \phi)$$

A phase sensitive detector, integrator and Voltage Controlled Oscillator (VCO) form a closed loop system which seeks to null  $\text{Sin}(\theta - \phi)$ .

When this is accomplished, the word state of the up-down counter ( $\phi$ ), equals, within the rated accuracy of the converter, the resolver shaft angle  $\theta$ .

## OPERATION OF THE CONVERTER

The 1S10/20/40/60/61 are tracking converters, this means that the output automatically follows the input for speeds up to the specified tracking rate for the frequency option specified. No convert command is necessary as the conversion is initiated by each LSB increment of the input. Each LSB increment of the converter initiates a BUSY pulse.

As the digital output of the converter passes through the major carry; i.e., all "1's" to all "0's" or the converse, a RIPPLE CLOCK (RC) logic output is initiated indicating that a revolution or a pitch of the input has been completed.

The direction of input rotation is indicated by the DIRECTION (DIR) logic output. This direction data is *always* valid in advance of a RIPPLE CLOCK pulse and, as it is internally latched, only changes with a change in direction (see Figure 3).

Both the RIPPLE clock pulse and DIRECTION data are unaffected by the application of the INHIBIT.

The INHIBIT logic input only inhibits the data transfer from the up-down counter to the output latches and therefore does not interrupt the operation of the tracking loop. Releasing the INHIBIT automatically generates a BUSY pulse to refresh the output data.

Two ENABLE inputs are provided, ENABLE M for the Most Significant 8 bits and ENABLE L for the Least Significant remainder. The operation of these enables has no effect on the conversion process.

The tracking conversion technique produces an internal signal at the input to the VCO that is proportional to the rate of the input angle. This is a bipolar dc analog signal that is made available at the VELOCITY (VEL) pin. As this is an internal control signal it is not closely characterized.

The signal at the output of the phase sensitive detector is the input to the internal nulling loop and hence is proportional to the error between the input angle and the output digital angle. As the converter is a type 2 servo loop, this DC ERROR signal will increase if the output angle fails to track the input for any reason; it is therefore an indication that the input has exceeded the specified tracking rate of the converter or due to some internal malfunction, the converter is unable to reach a null. By the use of two external comparators this voltage can be used as a "built in test"

**NOTE: The DC ERROR voltage has no internal filtering.**

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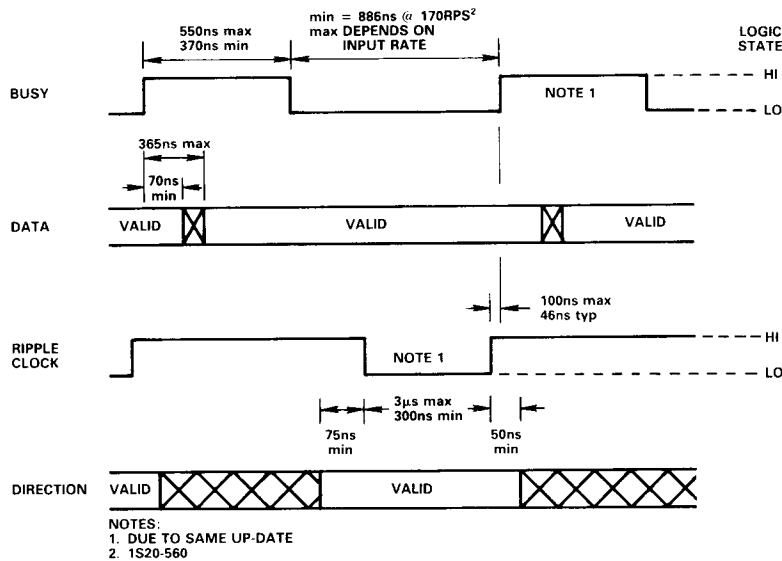


Figure 3. Timing Diagram

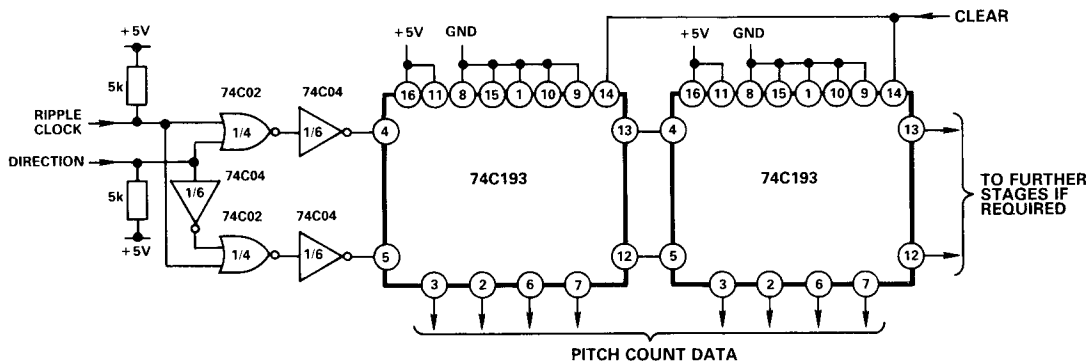


Figure 4. CMOS External Counter

**DATA TRANSFER**

The readiness of the converter for data transfer is given by the state of the BUSY output. The signal appearing on the BUSY output pin is a series of pulses of TTL levels when the angular input of the converter is changing. A BUSY pulse is initiated each time the input moves by an LSB and the internal counter is incremented or decremented. With the  $\overline{\text{INHIBIT}}$  input pin in the "Hi" TTL state, data will be transferred automatically to the output latches.

The  $\overline{\text{ENABLE}}$  input pin determines the state of the output data. A TTL logic "Hi" maintains the output data pins in a high impedance condition, the application of a logic "Lo" presents the data in the latches to the output pins.

From the above it can be seen that there are two methods available for transferring data.

One method is to transfer data when the BUSY is in a "Lo"

state or clock the data out on the trailing edge of the BUSY pulse. Both the  $\overline{\text{INHIBIT}}$  and the  $\overline{\text{ENABLE}}$ s must be in their correct state of "Hi" and "Lo's" respectively.

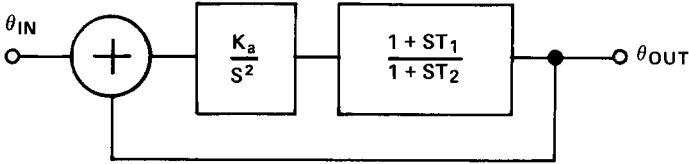
The alternative method is to use the  $\overline{\text{INHIBIT}}$  input. Data will always be valid one microsecond after the application of a logic "Lo" to the  $\overline{\text{INHIBIT}}$ . This is regardless of the time when the  $\overline{\text{INHIBIT}}$  is applied.

In order to count input revolutions or pitches, an external extension counter is required. A circuit performing this function is shown in Figure 2.

The DIRECTION (DIR) and RIPPLE CLOCK (RC) logic outputs should always be used in the manner shown in the application circuit. We recommend the circuit in Figure 2 to be used as the circuit in Figure 4 uses CMOS and great care must be taken to keep the stray capacitances low because of the high tracking rate of the converter.

## DYNAMIC PERFORMANCE

The transfer function of the converter is given below.



Open loop gain:

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{K_a}{S^2} \cdot \frac{1 + ST_1}{1 + ST_2}$$

Closed loop gain:

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{1 + ST_1}{1 + ST_1 + \frac{S^2}{K_a} + \frac{S^3 T_2}{K_a}}$$

1S10/1S20/1S40/1S60/1S61 (typical values)

| Constant<br>Option | 1S20<br>X10 | 1S40/60/61<br>X10 | 1S10<br>X50 | 1S20/40/60/61<br>X50 | 1S10<br>X60 | 1S20/40/60/61<br>X60 |
|--------------------|-------------|-------------------|-------------|----------------------|-------------|----------------------|
| $K_a$              | 38,000      | 9,500             | 1,150,000   | 144,000              | 5,700,000   | 713,000              |
| $T_1$              | 8.7ms       | 17.4ms            | 1.43ms      | 4.1ms                | 0.65ms      | 1.85ms               |
| $T_2$              | 1.3ms       | 2.6ms             | 0.22ms      | 0.6ms                | 0.084ms     | 0.25ms               |
| Gain Plot          | Figure 5    | Figure 5          | Figure 7    | Figure 7             | Figure 9    | Figure 9             |
| Phase Plot         | Figure 6    | Figure 6          | Figure 8    | Figure 8             | Figure 10   | Figure 10            |

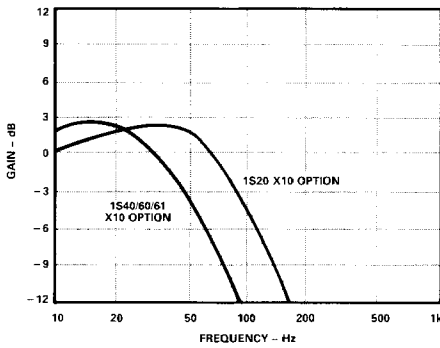


Figure 5.

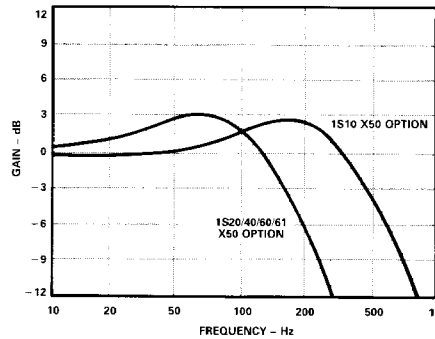


Figure 7.

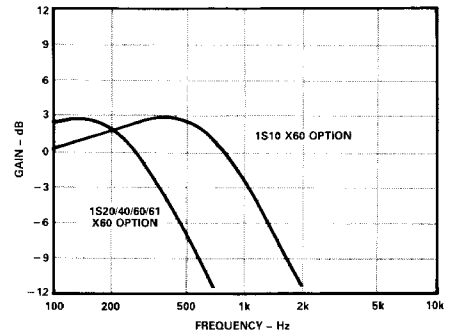


Figure 9.

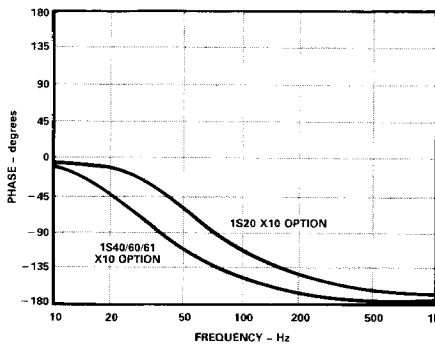


Figure 6.

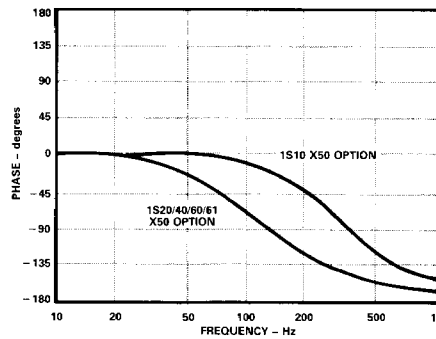


Figure 8.

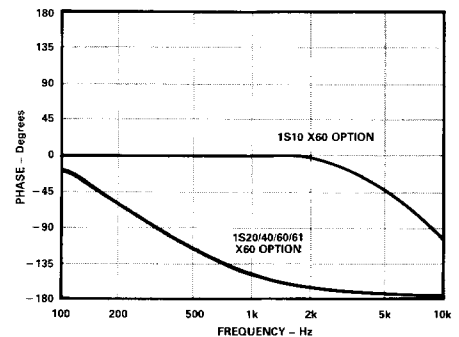


Figure 10.

### ACCELERATION ERROR

A tracking converter like the 1S20 employing a type 2 servo loop does not suffer any velocity lag, however, there is an additional error due to acceleration. This additional error can be defined using the acceleration constant  $K_a$  of the converter.

$$K_a = \frac{\text{Input acceleration}}{\text{Error in output angle}}$$

The numerator and denominator have the same units.  $K_a$  does not define maximum acceleration only the error due to acceleration, maximum acceleration is in the region of 10 times the  $K_a$  figure (deg/sec<sup>2</sup>).

An example using the  $K_a$  of the 1S60/560

Acceleration of 33 revolutions sec<sup>-2</sup> with  $K_a = 713,000$

Additional error = 1 arc-min

### DYNAMIC ACCURACY VS. RESOLVER PHASE SHIFT

Most resolvers, particularly those of the brushless type, exhibit a phase shift between the signal and the reference. This phase shift will give rise under dynamic conditions to an additional error defined by:

$$\frac{\text{Shaft Speed (RPS)} \times \text{Phase Shift (DEGS)}}{\text{Reference Frequency}}$$

For example, for a phase shift of 20°, a shaft rotation of 22rps and a reference frequency of 5kHz, the converter will exhibit an additional error of:

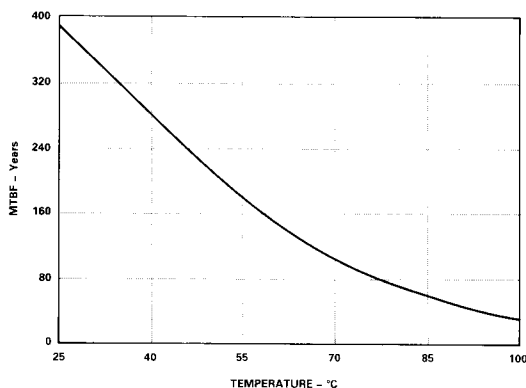
$$\frac{20 \times 22}{5000} = 0.088^\circ$$

This effect can be eliminated by putting a phase shift in the reference to the converter equivalent to the phase shift in the resolver.

### MEAN TIME BETWEEN FAILURES (MTBF)

The reliability of these products is very high due to the extensive use of custom chip circuitry. For details of MTBF figures under particular conditions please consult the factory.

The graph below shows the typical variation of MTBF with temperature for the 1S20, under ground benign environment.



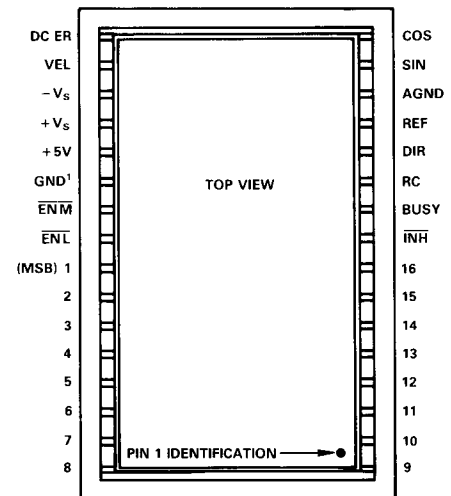
### ABSOLUTE MAXIMUM INPUTS (with respect to GND)

|                              |                   |
|------------------------------|-------------------|
| +V <sub>S</sub> <sup>1</sup> | 0V to +17V dc     |
| -V <sub>S</sub> <sup>1</sup> | 0V to -17V dc     |
| +5V <sup>2</sup>             | 0V to +7.0V dc    |
| Reference                    | ±17V dc           |
| Sine                         | ±17V dc           |
| Cosine                       | ±17V dc           |
| Any Logical Input            | -0.4V to +5.5V dc |

### CAUTION:

1. Correct polarity voltages must be maintained on the +V<sub>S</sub> and -V<sub>S</sub> pins.
2. The +5 volt power supply must *never* go below GND potential.

### PIN CONFIGURATION



NOTE: 1. GND IS INTERNALLY CONNECTED TO CASE ON 4YO (METAL PACKAGE) OPTIONS.

### PROCESSING FOR HIGH RELIABILITY

#### STANDARD PROCESSING

As part of the standard manufacturing procedure, all converters receive the following processing:

| Process                      | Condition         |
|------------------------------|-------------------|
| 1. Pre-Cap Visual Inspection | In-House Criteria |
| 2. Burn-In                   | 70°C              |
| 3. Constant Acceleration     | 5000G             |
| 4. Gross Leak Test           | In-House Criteria |
| 5. Final Electrical Test     | Performed at 25°C |

## HI-REL PROCESSING

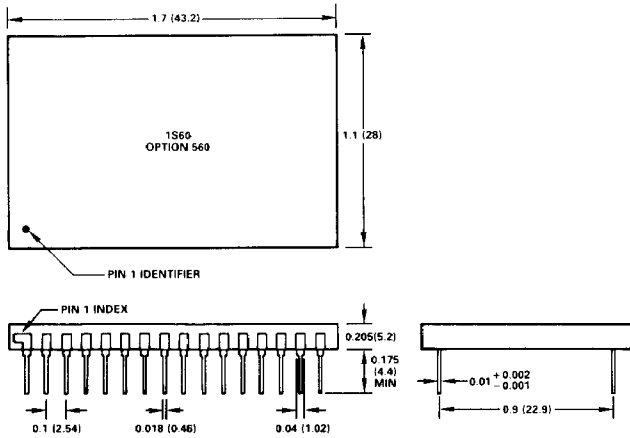
All models ordered to high reliability requirements will be identified with a B suffix, and will have received the following processing:

1. Internal visual inspection.
2. Stabilization bake, 24 hours at 150°C.

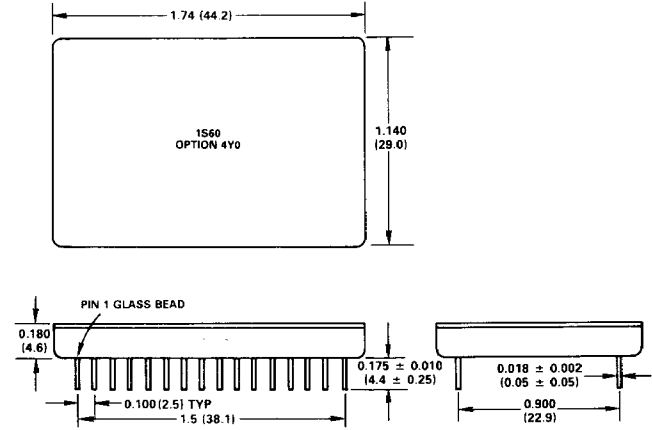
3. Temperature cycling, -65°C to +150°C.
4. Constant acceleration, 5000G.
5. Powered burn-in 160 hours at 125°C.
6. Final electrical test at  $T_{min}$  and  $T_{max}$ .
7. Seal test, fine and gross.
8. External visual inspection.

## OUTLINE DIMENSIONS PACKAGING SPECIFICATIONS

Dimensions shown in inches and (mm).



Package for 5YO Options (Ceramic)



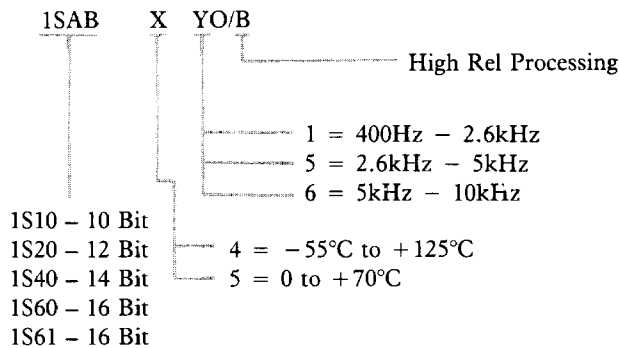
Package for 4YO and 4YO/B Options (Metal)

## OTHER PRODUCTS

- IRDC1732- Inductosyn<sup>TM</sup>/Resolver-to-Digital Converter (Hybrid)
- IPA1751- Inductosyn<sup>TM</sup> Pre-Amplifier
- OSC1754- Power Oscillator
- OSC1758- Power Oscillator (Hybrid)
- IPA1764- Inductosyn<sup>TM</sup> Pre-Amplifier (Hybrid)
- MCI1794- 3 Channel Inductosyn<sup>TM</sup>/Resolver-to-Digital Converter (Multibus Compatible Card)

<sup>TM</sup>Inductosyn is a trademark of Farrand Industries

## ORDERING INFORMATION



Note

In the case of the 1S10 there is no X10 option available.