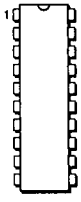
FEATURES

- ☐ Complete DTMF transmitter/receiver
- ☐ Excellent performance
- ☐ Single 5 Volt supply CMOS technology
- ☐ Microprocessor port
- ☐ Adjustable guard time/Automatic tone burst mode/Call progress mode

GENERAL DESCRIPTION

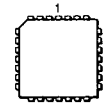
The SC11280 is a monolithic DTMF transceiver with call progress filter. It is fabricated in Sierra's proprietary 3 micron CMOS technology which provides low power dissipation and high reliability. The DTMF receiver is based upon the industry standard SC11270 monolithic DTMF receiver; the transmitter utilizes a switched capacitor filter for low distortion, high accuracy DTMF signaling. Internal counters provide a burst mode such that tone bursts can be transmitted with precise timing. A call progress filter can be selected allowing a microprocessor to analyze call progress tones. A standard microprocessor bus is provided and is directly compatible with 6800 series microprocessors.

20-PIN DIP PACKAGE



SC11280CN
SC11280EN*

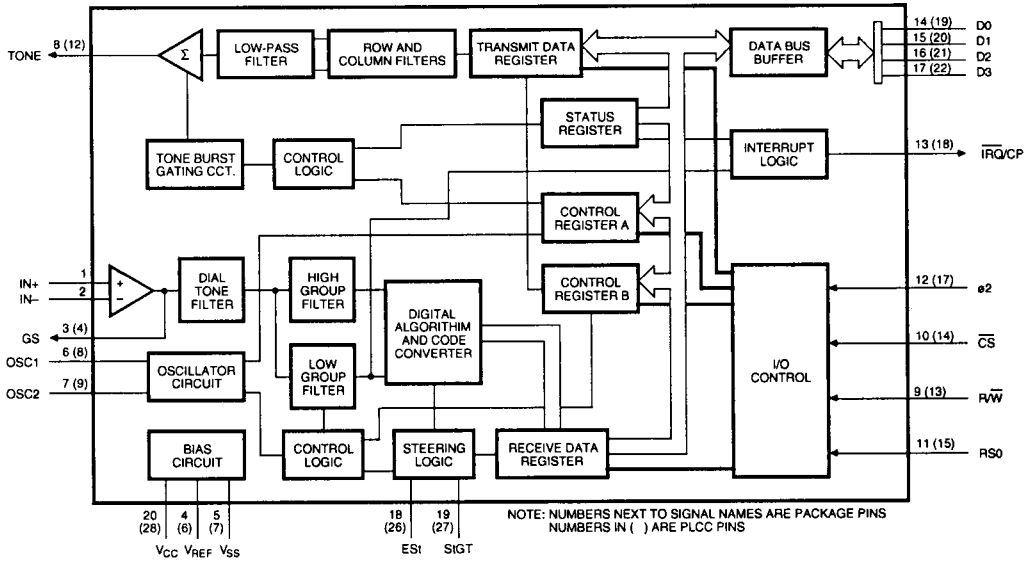
28-PIN PLCC PACKAGE



SC11280CV
SC11280EV*

*Special Order

BLOCK DIAGRAM



PIN DESCRIPTIONS

NAME	PIN #	DESCRIPTION
ø2	12 (17)	System clock input, TTL compatible.
$\overline{CS}$	10 (14)	Chip Select, TTL input ($\overline{CS}$ = 0 to select the chip).
D_0–D_3	14–17 (19–22)	Microprocessor data bus (TTL compatible).
ESt	18 (26)	Early Steering output. Presents a logic high once the digital algorithm has detected a valid tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low.
GS	3 (4)	Gain Select. Gives access to output of front end differential amplifier for connection of feedback resistor.
IN+	1	Non-inverting op-amp input.
IN–	2	Inverting op-amp input.
$\overline{IRQ}$/CP	13 (18)	Interrupt request to MPU (open drain output). Also, when call progress (CP) mode has been selected and interrupt enabled the $\overline{IRQ}$/CP pin will output a rectangular wave signal representative of the input signal applied at the input op-amp. The input signal must be within the bandwidth limits of the call progress filter. See Figure 11.
N.C.	(3, 5, 10, 11, 16, 23, 24, 25)	No Connection.
RS_0	11 (15)	Register select input. See register decode table, TTL compatible.
R/$\overline{W}$	9 (13)	Read/Write input. Controls the direction of data transfer to and from the MPU and the receiver/transmitter, TTL compatible.
StGT	19 (27)	Steering input/Guard Time output (bidirectional). A voltage greater than V_{TSt} detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than V_{TSt} frees the device to accept a new tone pair. The GT output acts to reset the external steering time-constant; its state is a function of ESt and the voltage on St.
TONE	8 (12)	Dual Tone Multi-Frequency output.
V_{CC}	20 (28)	Positive power supply input.
V_{REF}	4 (6)	Reference voltage output, nominally $V_{CC}/2$ is used to bias inputs at mid-rail (see application diagram).
V_{SS}	5 (7)	Negative power supply input.
$XTAL_{IN}$	6 (8)	DTMF clock/oscillator input.
$XTAL_{OUT}$	7 (9)	Clock output. A 3.5795 MHz crystal connected between OSC1 and OSC2 completes the internal oscillator circuit.

FUNCTIONAL DESCRIPTION

The SC11280 integrated DTMF Transceiver architecture consists of a high performance DTMF receiver with internal gain setting amplifier and a DTMF generator which employs a burst counter such that precise tone bursts and pauses can be synthesized. A call progress mode can be selected such that frequencies within the specified pass band can be detected. A standard microprocessor interface allows access to an internal status register, two control registers and two data registers.

Input Configuration

The input arrangement of the SC11280 provides a differential-input operational amplifier as well as a bias source (V_{REF}) which is used to bias the inputs at $V_{CC}/2$. Provision is made for connection of a feedback resistor to the op-amp output (GS) for adjustment of gain. In a single ended configuration, the input pins are connected as shown in Figure 1. Figure 2 shows the necessary connections for a differential input configuration.

Receiver Section

Separation of the low and high group tones is achieved by applying the DTMF signal to the inputs of two sixth-order switched-capacitor bandpass filters, the bandwidths of which correspond to the low and high group frequencies (see Figure 5). The low group filter also incorporates notches at 350 Hz and 440 Hz for exceptional dial-tone rejection. Each filter output is followed by a second-order switched-capacitor filter section which

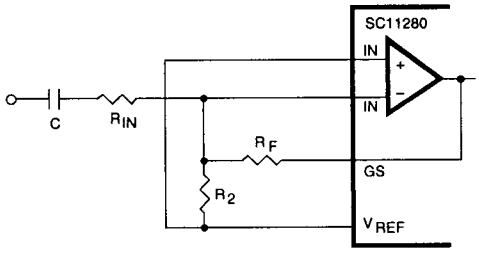


Figure 1. Single Ended Input Configuration

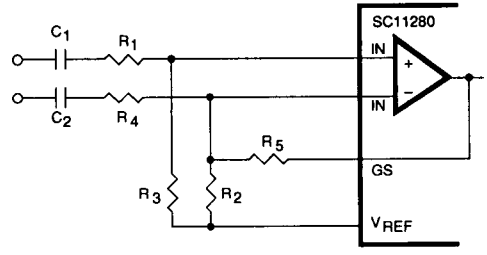


Figure 2. Differential Input Configuration

smooths the signals prior to limiting. Limiting is performed by high-gain comparators which are provided with hysteresis to prevent detection of unwanted low-level signals. The outputs of the comparators provide full rail logic swings at the frequencies of the incoming DTMF signals.

Following the filter section is a decoder employing digital counting techniques to determine the frequencies of the incoming tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm protects against tone simulation by extraneous signals such as voice while providing tolerance to small frequency deviations and variations. This averaging algorithm has been developed to ensure an optimum combination of immunity to talk-off and tolerance to the presence of interfering frequencies (third tones) and noise. When the detector recognizes the presence of two valid tones (this is referred to as the "signal condition" in some industry specifications) the "Early Steering" (ESt) output will go to an active state. Any subsequent loss of signal condition will cause ESt to assume an inactive state (see Steering Circuit).

Steering Circuit

Before registration of a decoded tone pair, the receiver checks for a valid signal duration (referred to as character recognition condition). This check is performed by an external RC time constant driven by ESt. A logic high on ESt causes V_C (see Figure 3) to rise as the capacitor discharges. Provided that the signal condition is maintained (ESt remains high) for the validation period (t_{GTP}), V_C reaches the threshold (V_{TSt}) of the steering logic to register the tone pair, latching its corresponding 4-bit code (see Figure 5) into the Receive Data Register. At this point the GT output is activated and drives V_C to V_{CC}. GT continues to drive high as long as ESt remains high. Finally, after a short delay to allow the output latch to settle, the delayed steering output flag goes high, signalling that a received tone pair has been registered. It is possible to monitor the status of the delayed steering flag by checking the appropriate bit in the status register. If interrupt mode has been selected, the IRQ/CP pin will pull low when the delayed steering flag is active.

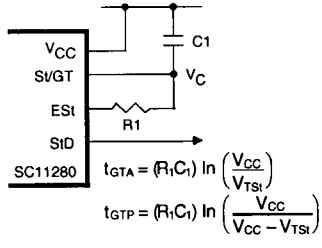


Figure 3. Basic Steering Circuit

The contents of the output latch are updated on an active delayed steering transition. This data is presented to the 4-bit bi-directional data bus when the Receive Data Register is read. The steering circuit works in reverse to validate the interdigit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (drop out) too short to be considered a valid pause. This facility, together with the capability of selecting the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

Guard Time Adjustment

The simple steering circuit shown in Figure 3 is adequate for most applications. Component values are chosen according to the formula:

$$t_{REC} = t_{DP} + t_{GTP}$$
$$t_{ID} = t_{DA} + t_{GTA}$$

The value of t_{DP} is a device parameter (see table) and t_{REC} is the minimum signal duration to be recognized by the receiver. A value for C of 0.1 µF is recommended for most applications, leaving R to be selected by the designer. Different steering arrangements may be used to select independently the guard times for tone present (t_{GTP}) and tone absent (t_{GTA}). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and interdigital pause. Guard time adjustment also allows the designer to tailor system parameters such as talk-off and noise immunity. Increasing t_{REC} improves talk-off performance since it reduces the probability that tones simulated by speech will maintain signal condition long enough to be registered. Alternatively, a relatively short t_{REC}