FAIRCHILD
A Schlumberger Company

F9450 (MIL-STD 1750A) 16-Bit Bipolar Microprocessor

Advance Product Information

Microprocessor Product

- **Single-Chip Microprocessor Fully Implements MIL-STD 1750A (Notice 1) ISA.**
- **High Performance Over Military Temperature Range: 700K IPS DAIS Mix with Floating Point; 0.2 μs ADD, 1.85 μs MULTIPLY**
- **Real-Time Processing, Two Programmable Timers, 16 Levels of Vectored Interrupt**
- **32- and 48-Bit Floating Point Arithmetic on Chip**
- **Bipolar VLSI I^3L® -II - 1 x 10^5 Radiation**
- **Multiprocessor Capabilities**
- **Single and Double Precision Arithmetic**
- **Direct Address of Up to 64K Words, Expandable to 1M Words**
- **16 General-Purpose Registers**
- **Static Operation with Single Clock (0-20 MHz)**
- **Low-Power Schottky Inputs and Outputs**
- **Single 5 V Supply; Injector Current Source Required**
- **64-Pin DIPs with 50-mil Pin Centers**

Description

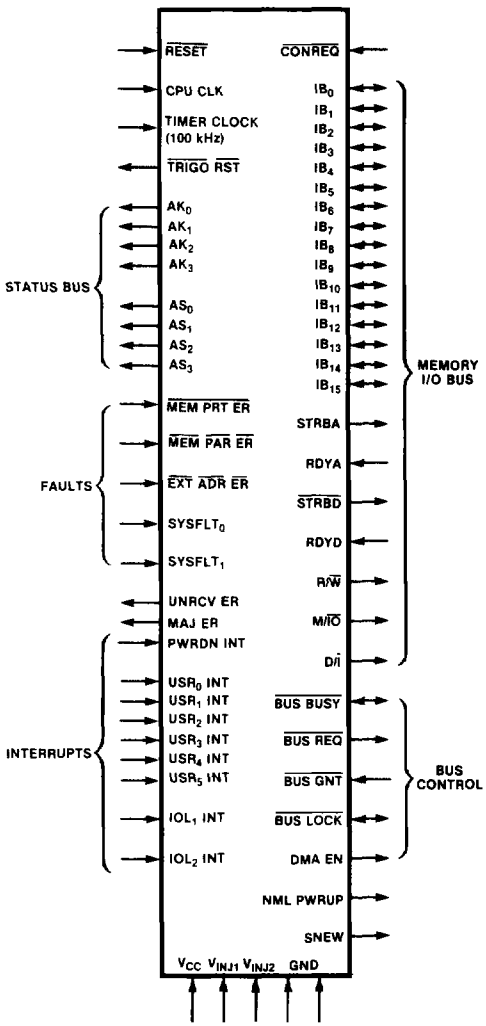
The F9450 microprocessor, in a single chip, completely implements MIL-STD 1750A (Notice 1) Instruction Set Architecture. This microprocessor is currently being developed as the heart of a high-performance processor family for commercial and military applications requiring high-speed, sophisticated, real-time processing.

Utilizing 16-bit architecture, the F9450 provides 16 user-accessible general-purpose registers and performs floating point operations on-chip. The I^3L-II bipolar VLSI technology affords static operation with 200 ns bus cycle times, low-power Schottky input/output, inherent radiation tolerance (1 x 10^5 rads), and operation at 20 MHz over the full military temperature range.

Real-time processing is achieved through advance design and architecture, incorporating two programmable timers, a complete 16-level interrupt processor, and a comprehensive fault handler on the chip.

Several support circuits and systems can provide additional capability. These include the F9443 Math Co-processor, options for MIL-STD 1750A built-in functions, user-programmable functions, and IEEE floating point; the F9446 Dynamic Memory Controller; the F9451 Memory Management Unit, providing memory-mapped expansion to 1M words; and the F9452 Block Protect RAM. A multi-user development system (FS-I) has been developed, as well as EMUTRAC™, which offers real-time system emulation and debugging.

Signal Functions



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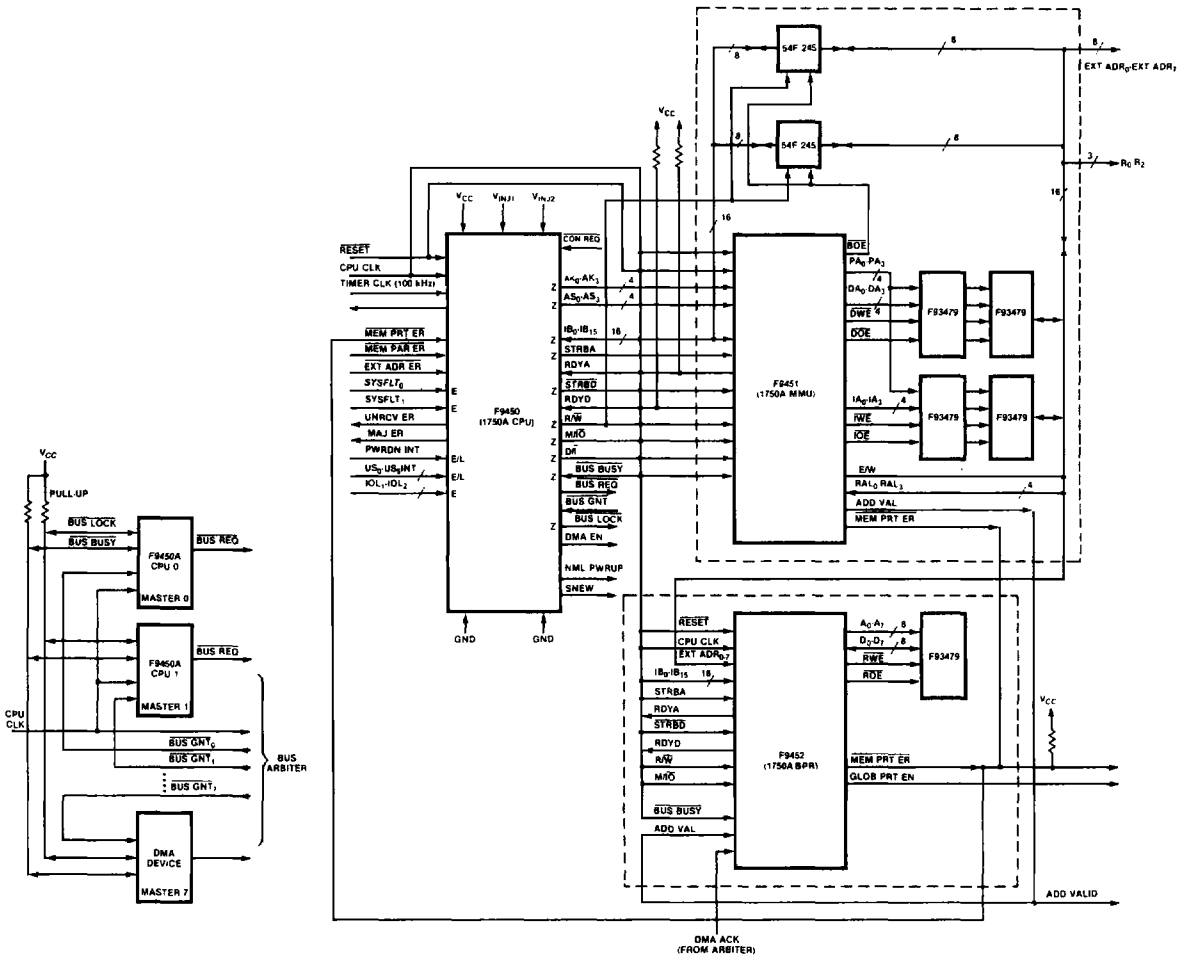

Instruction Execution Times (μs) - 50 ns CPU Clock Period

	Single Precision Integer	Double Precision Integer	Floating Point	Extended Floating Point
Register Add/Sub	0.2	0.8	4.5	5.75
Register Multipy	1.85	5.75	5.6	12.4
Register Divide	4.7	12.0	9.8	21.5
Load Direct	0.6	1.25	1.25	1.3
Branch	*Taken = 0.75 μs*		*Not Taken = 0.2 μs*	

External Arbitration

In an external arbitration of a multi-processor system, the bus arbiter receives requests (BUS REQ) from each of the bus masters and issues the bus grant (BUS GNT) to the highest priority bus master. That bus master will acquire the bus only if it is not locked (BUS LOCK not active).

Memory Protection and Management

In this configuration, the F9450 is connected to the MMU and the BPR. The MMU consists of the F9451, the maps for instruction and data (four F93479s), and two bidirectional drivers. The BPR consists of the F9452 and protection tables for CPU and DMA modes (F93479). Protection errors from the MMU and BPR units are wired-OR to the CPU MEM PRT ER input.