NEC

MOS INTEGRATED CIRCUIT

MC-421000A32, 421000A36 SERIES

1 M-WORD BY 32-BIT, 1 M-WORD BY 36-BIT DYNAMIC RAM MODULE FAST PAGE MODE

Description

The MC-421000A32 series is a 1 048 576 words by 32 bits dynamic RAM module on which 8 pieces of 4 M DRAM : μPD424400 are assembled.

The MC-421000A36 series is a 1 048 576 words by 36 bits dynamic RAM module on which 8 pieces of 4 M DRAM : μPD424400 and 4 pieces of 1 M DRAM : μPD421000 are assembled.

These modules provide high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 1 048 576 words by 32 bits organization (MC-421000A32 series)
- 1 048 576 words by 36 bits organization (MC-421000A36 series)
- Fast access and cycle time

Family	Access time (MAX.)	R/W cycle time (MIN.)	Power consumption (MAX.)	
			Active	Standby
MC-421000A32-60	60 ns	120 ns	5 040 mW	42 mW (CMOS level input)
MC-421000A32-70	70 ns	140 ns	4 200 mW	
MC-421000A32-80	80 ns	160 ns	3 780 mW	
MC-421000A32-10	100 ns	190 ns	3 360 mW	
MC-421000A36-60	60 ns	120 ns	6 510 mW	63 mW (CMOS level input)
MC-421000A36-70	70 ns	140 ns	5 880 mW	
MC-421000A36-80	80 ns	160 ns	5 250 mW	
MC-421000A36-10	100 ns	190 ns	4 620 mW	

- 1 024 refresh cycles/16 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- 72-pin single in-line memory module (Pin pitch = 1.27 mm)
- Single +5.0 V ± 5 % power supply
- Access time can be distinguished with charateristics of PD-pins(PD0 to PD3)

Ordering Information

[MC-421000A32 series]

Part number	Access time (MAX.)	Package	Mounted devices
MC-421000A32B-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector : Solder coating (HAL)	8 pieces of μPD424400LA (300 mil SOJ) (Single side)
MC-421000A32B-70	70 ns		
MC-421000A32B-80	80 ns		
MC-421000A32B-10	100 ns		
MC-421000A32F-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector : Gold plating	
MC-421000A32F-70	70 ns		
MC-421000A32F-80	80 ns		
MC-421000A32F-10	100 ns		

[MC-421000A36 series]

Part number	Access time (MAX.)	Package	Mounted devices
MC-421000A36B-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector : Solder coating (HAL)	8 pieces of μPD424400LA (300 mil SOJ) 4 pieces of μPD421000GX (6 mm × 16 mm TSOP (I)) (Single side)
MC-421000A36B-70	70 ns		
MC-421000A36B-80	80 ns		
MC-421000A36B-10	100 ns		
MC-421000A36F-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector : Gold plating	
MC-421000A36F-70	70 ns		
MC-421000A36F-80	80 ns		
MC-421000A36F-10	100 ns		
MC-421000A36BE-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector : Solder coating (HAL)	8 pieces of μPD424400LA (300 mil SOJ) 4 pieces of μPD421000LA (300 mil SOJ) (Double side)
MC-421000A36BE-70	70 ns		
MC-421000A36BE-80	80 ns		
MC-421000A36BE-10	100 ns		
MC-421000A36FE-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector : Gold plating	
MC-421000A36FE-70	70 ns		
MC-421000A36FE-80	80 ns		
MC-421000A36FE-10	100 ns		
MC-421000A36BJ-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector : Solder coating (HAL)	8 pieces of μPD424400LA (300 mil SOJ) 4 pieces of μPD421000LA (300 mil SOJ) (Single side)
MC-421000A36BJ-70	70 ns		
MC-421000A36BJ-80	80 ns		
MC-421000A36BJ-10	100 ns		
MC-421000A36FJ-60	60 ns	72-pin Single In-line Memory Module (Socket Type) Edge connector : Gold plating	
MC-421000A36FJ-70	70 ns		
MC-421000A36FJ-80	80 ns		
MC-421000A36FJ-10	100 ns		

Quality Grade

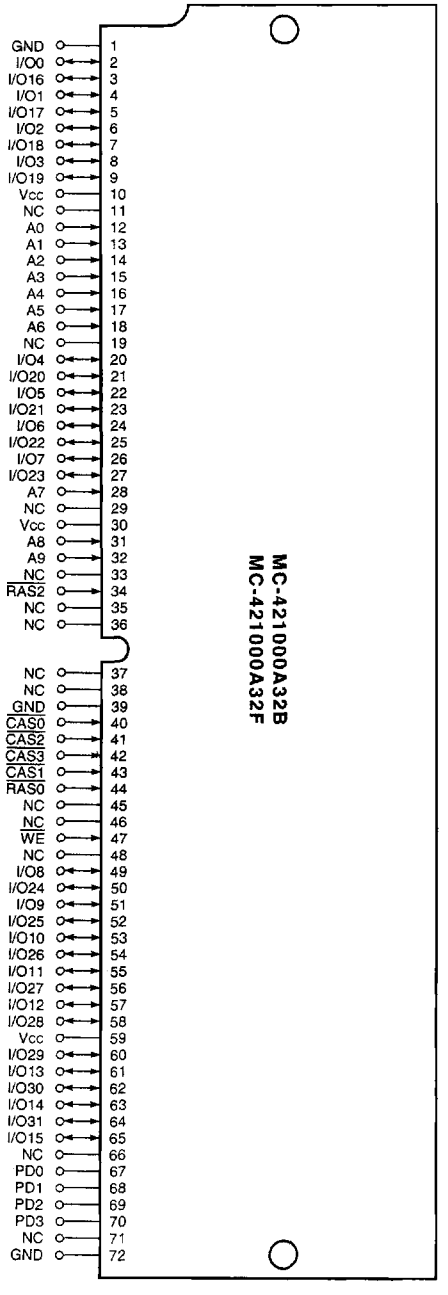
Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

Pin Configurations

[MC-421000A32 series]

72-pin Single In-line Memory Module Socket Type (Edge connector: Solder Coating, Gold Plating)



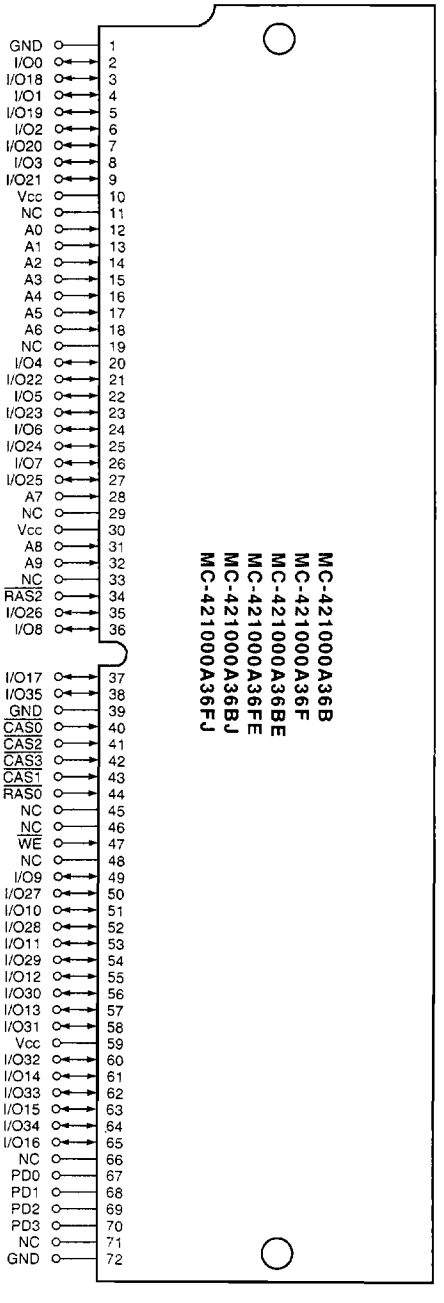
A0-A9	: Address Inputs
I/O0-I/O31	: Data Inputs/Outputs
$\overline{CAS0}$-$\overline{CAS3}$	: Column Address Strobe
$\overline{RAS0}$, $\overline{RAS2}$	: Row Address Strobe
$\overline{WE}$	: Write Enable
Vcc	: Power Supply
GND	: Ground
NC	: No connection

The internal connection of PD pins (PD0 - PD3) depends on access time.

Pin Name	Pin No.	Access Time			
		60 ns	70 ns	80 ns	100 ns
PD0	67	GND	GND	GND	GND
PD1	68	GND	GND	GND	GND
PD2	69	NC	GND	NC	GND
PD3	70	NC	NC	GND	GND

[MC-421000A36 series]

72-pin Single In-line Memory Module Socket Type (Edge connector: Solder Coating, Gold Plating)



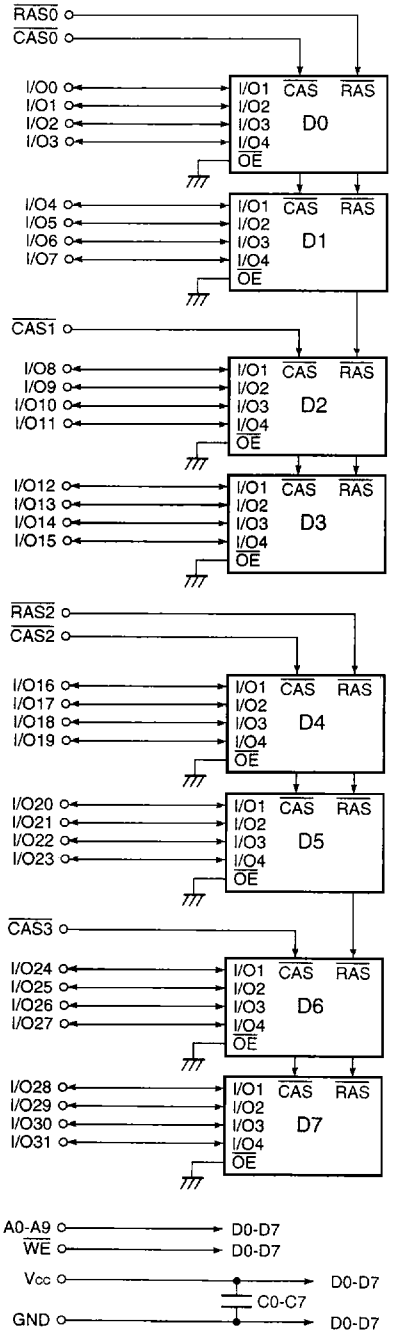
A0-A9	: Address Inputs
I/O0-I/O35	: Data Inputs/Outputs
$\overline{CAS0}$-$\overline{CAS3}$	: Column Address Strobe
$\overline{RAS0}$, $\overline{RAS2}$	: Row Address Strobe
$\overline{WE}$	: Write Enable
Vcc	: Power Supply
GND	: Ground
NC	: No connection

The internal connection of PD pins (PD0 - PD3) depends on access time.

Pin Name	Pin No.	Access Time			
		60 ns	70 ns	80 ns	100 ns
PD0	67	GND	GND	GND	GND
PD1	68	GND	GND	GND	GND
PD2	69	NC	GND	NC	GND
PD3	70	NC	NC	GND	GND

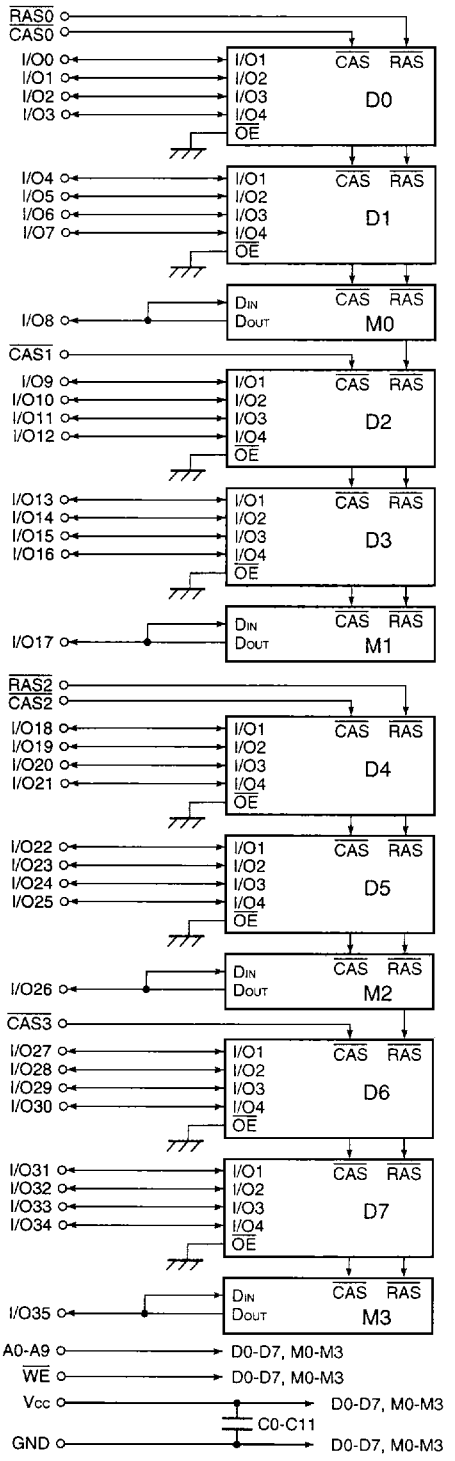
Block Diagram

[MC-421000A32 series]



Remark D0-D7 : μPD424400

[MC-421000A36 series]



Remark D0-D7 : μPD424400
M0-M3 : μPD421000

Electrical Specifications Notes 1, 2

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D	MC-421000A32	8	W
		MC-421000A36	12	
Operating temperature	T_{opt}		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.75	5.0	5.25	V
High level input voltage	V_{IH}		2.4		V_{CC} +1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Ambient temperature	T_a		0		70	°C

Capacitance (T_a = +25 °C, f = 1 MHz)

[MC-421000A32 series]

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A9			68	pF
	C_{I2}	$\overline{WE}$			76	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			43	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS3}$			29	
Data Input/Output capacitance	$C_{I/O}$	I/O0 - I/O31			17	pF

[MC-421000A36 series]

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A9			88	pF
	C_{I2}	$\overline{WE}$			104	
	C_{I3}	$\overline{RAS0}$, $\overline{RAS2}$			57	
	C_{I4}	$\overline{CAS0}$ - $\overline{CAS3}$			36	
Data Input/Output capacitance	$C_{I/O1}$	I/O0 - I/O7, I/O9 - I/O16, I/O18 - I/O25, I/O27 - I/O34			17	pF
	$C_{I/O2}$	I/O8 - I/O17, I/O26, I/O35			22	

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

[MC-421000A32 series]

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		960	mA	3,4,7
			t_{RAC} = 70 ns		800		
			t_{RAC} = 80 ns		720		
			t_{RAC} = 100 ns		640		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geqq V_{IH(MIN.)}$	I_O = 0 mA		16	mA	
		$\overline{RAS}$, $\overline{CAS} \geqq V_{CC}$ −0.2 V	I_O = 0 mA		8		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geqq V_{IH(MIN.)}$ $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		960	mA	3,4, 5,7
			t_{RAC} = 70 ns		800		
			t_{RAC} = 80 ns		720		
			t_{RAC} = 100 ns		640		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leqq V_{IL(MAX.)}$, $\overline{CAS}$ Cycling $t_{PC} = t_{PC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		720	mA	3,4,6
			t_{RAC} = 70 ns		640		
			t_{RAC} = 80 ns		560		
			t_{RAC} = 100 ns		480		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		960	mA	3,4
			t_{RAC} = 70 ns		800		
			t_{RAC} = 80 ns		720		
			t_{RAC} = 100 ns		640		
Input leakage current	$I_{I(L)}$	V_I = 0 to 5.5 V all other pins not under test = 0 V		−10	+10	μA	
Output leakage current	$I_{O(L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		−10	+10	μA	
High level output voltage	V_{OH}	I_O = −5.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +4.2 mA			0.4	V	

[MC-421000A36 series]

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		1 240	mA	3,4,7
			t_{RAC} = 70 ns		1 120		
			t_{RAC} = 80 ns		1 000		
			t_{RAC} = 100 ns		880		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geqq V_{IH(MIN.)}$	I_O = 0 mA		24	mA	
		$\overline{RAS}$, $\overline{CAS} \geqq V_{CC}$ −0.2 V	I_O = 0 mA		12		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $\overline{CAS} \geqq V_{IH(MIN.)}$ $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		1 240	mA	3,4,5,7
			t_{RAC} = 70 ns		1 120		
			t_{RAC} = 80 ns		1 000		
			t_{RAC} = 100 ns		880		
Operating current (Fast page mode)	I_{CC4}	$\overline{RAS} \leqq V_{IL(MAX.)}$, $\overline{CAS}$ Cycling $t_{PC} = t_{PC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		1 040	mA	3,4,6
			t_{RAC} = 70 ns		920		
			t_{RAC} = 80 ns		800		
			t_{RAC} = 100 ns		680		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 60 ns		1 240	mA	3,4
			t_{RAC} = 70 ns		1 120		
			t_{RAC} = 80 ns		1 000		
			t_{RAC} = 100 ns		880		
Input leakage current	$I_{I(L)}$	V_I = 0 to 5.5 V all other pins not under test = 0 V		−10	+10	μA	
Output leakage current	$I_{O(L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		−10	+10	μA	
High level output voltage	V_{OH}	I_O = −5.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +4.2 mA			0.4	V	

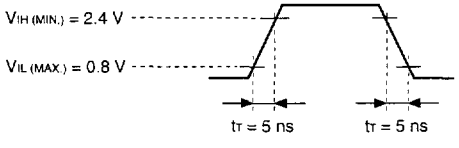
AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 8, 9

Parameter		Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		t_{RAC} = 100 ns		Unit	Notes
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time		t_{RC}	120		140		160		190		ns	
Fast Page Mode Cycle Time		t_{PC}	40		45		50		60		ns	
Access Time from $\overline{RAS}$		t_{RAC}		60		70		80		100	ns	10,11
Access Time from $\overline{CAS}$	MC-421000A32	t_{CAC}		15		20		20		25	ns	10,11
	MC-421000A36			20								
Access Time from Column Address		t_{AA}		30		35		40		50	ns	10,11
Access Time from $\overline{CAS}$ Precharge		t_{ACP}		35		40		45		55	ns	11
$\overline{RAS}$ to Column Address Delay Time		t_{RAD}	15	30	15	35	17	40	17	50	ns	10
$\overline{CAS}$ to Data Setup Time		t_{CLZ}	0		0		0		0		ns	11
Output Buffer Turn-off Delay Time from $\overline{CAS}$		t_{OFF}	0	15	0	15	0	20	0	25	ns	12
Transition Time (Rise and Fall)		t_T	3	50	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time		t_{RP}	50		60		70		80		ns	
$\overline{RAS}$ Pulse Width		t_{RAS}	60	10 000	70	10 000	80	10 000	100	10 000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)		t_{RASP}	60	125 000	70	125 000	80	125 000	100	125 000	ns	
$\overline{RAS}$ Hold Time		t_{RSH}	20		20		20		25		ns	
$\overline{CAS}$ Pulse Width		t_{CAS}	20	10 000	20	10 000	20	10 000	25	10 000	ns	
$\overline{CAS}$ Hold Time		t_{CSH}	60		70		80		100		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time		t_{RCD}	20	40	20	50	25	60	25	75	ns	10
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	10		10		10		10		ns	13
$\overline{CAS}$ Precharge Time		t_{CPN}	10		10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)		t_{CP}	10		10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time		t_{RPC}	10		10		10		10		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge		t_{RHCP}	35		40		45		55		ns	
Row Address Setup Time		t_{ASR}	0		0		0		0		ns	
Row Address Hold Time		t_{RAH}	10		10		12		12		ns	
Column Address Setup Time		t_{ASC}	0		0		0		0		ns	
Column Address Hold Time	MC-421000A32	t_{CAH}	15		15		15		20		ns	
	MC-421000A36				17		20					
Column Address Lead Time Referenced to $\overline{RAS}$		t_{RAL}	30		35		40		50		ns	
Read Command Setup Time		t_{RCS}	0		0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$		t_{RRH}	10		10		10		10		ns	14
Read Command Hold Time Referenced to $\overline{CAS}$		t_{RCH}	0		0		0		0		ns	14
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$		t_{WCH}	15		15		15		20		ns	15
Data-in Setup Time		t_{DS}	0		0		0		0		ns	16
Data-in Hold Time	MC-421000A32	t_{DH}	15		15		15		20		ns	16
	MC-421000A36						20					
Write Command Setup Time		t_{WCS}	0		0		0		0		ns	17
$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)		t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)		t_{CHR}	15		15		15		20		ns	
$\overline{WE}$ Setup Time		t_{WSR}	10		10		10		10		ns	
$\overline{WE}$ Hold Time		t_{WHR}	15		15		15		20		ns	
Refresh Time		t_{REF}		16		16		16		16	ms	

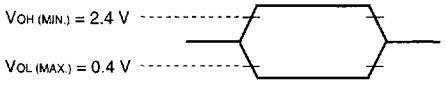
Notes

1. All voltages are referenced to GND.
2. After power up, wait more than 100 μs and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.
3. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycles rates (t_{RC} and t_{PC}).
4. Specified values are obtained with outputs unloaded.
5. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
6. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
7. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leqq V_{IL\,(MAX.)}$ and $\overline{CAS} \geqq V_{IH\,(MIN.)}$.
8. AC measurements assume t_T = 5 ns.
9. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



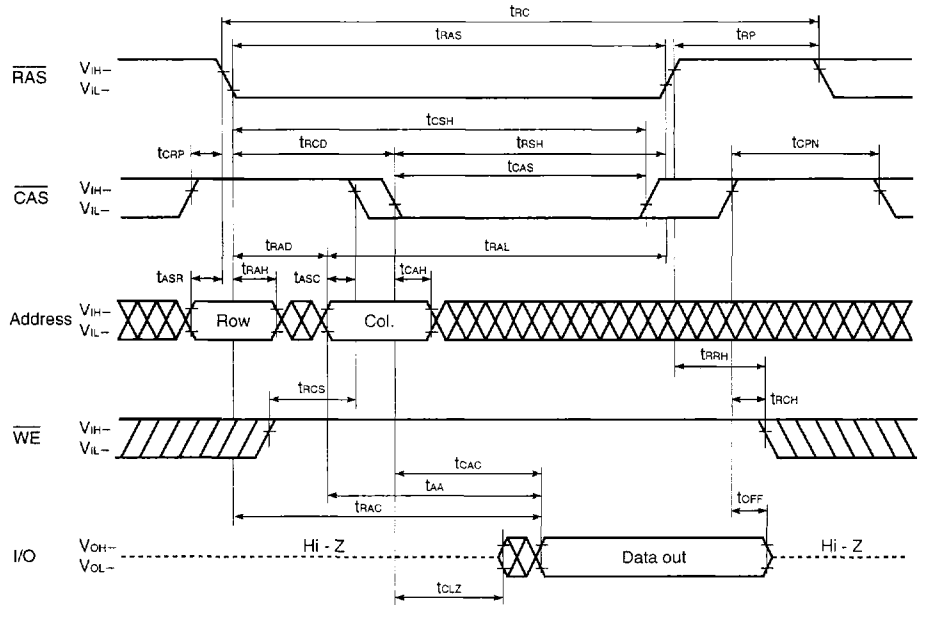
10. For read cycles, access time is defined as follows :

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leqq t_{RAD\,(MAX.)}$ and $t_{RCD} \leqq t_{RCD\,(MAX.)}$	$t_{RAC\,(MAX.)}$	$t_{RAC\,(MAX.)}$
$t_{RAD} > t_{RAD\,(MAX.)}$ and $t_{RCD} \leqq t_{RCD\,(MAX.)}$	$t_{AA\,(MAX.)}$	$t_{RAD} + t_{AA\,(MAX.)}$
$t_{RCD} > t_{RCD\,(MAX.)}$	$t_{CAC\,(MAX.)}$	$t_{RCD} + t_{CAC\,(MAX.)}$

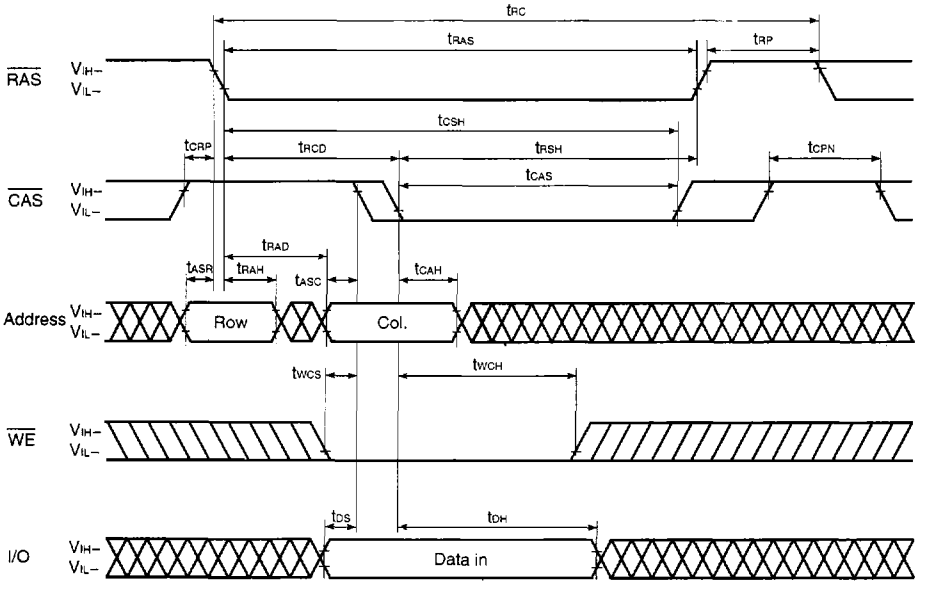
$t_{RAD\,(MAX.)}$ and $t_{RCD\,(MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geqq t_{RAD\,(MAX.)}$ and $t_{RCD} \geqq t_{RCD\,(MAX.)}$ will not cause any operation problems.

11. Loading conditions are 2 TTLs and 100 pF.
12. $t_{OFF\,(MAX.)}$ defines the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL}.
13. $t_{CRP\,(MIN.)}$ requirement should be applied to $\overline{RAS}$, $\overline{CAS}$ cycles preceded by any cycles.
14. Either $t_{RCH\,(MIN.)}$ or $t_{RRH\,(MIN.)}$ should be met in read cycles.
15. In early write cycles, $t_{WCH\,(MIN.)}$ should be met.
16. $t_{DS\,(MIN.)}$ and $t_{DH\,(MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles.
17. If $t_{WCS} \geqq t_{WCS\,(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

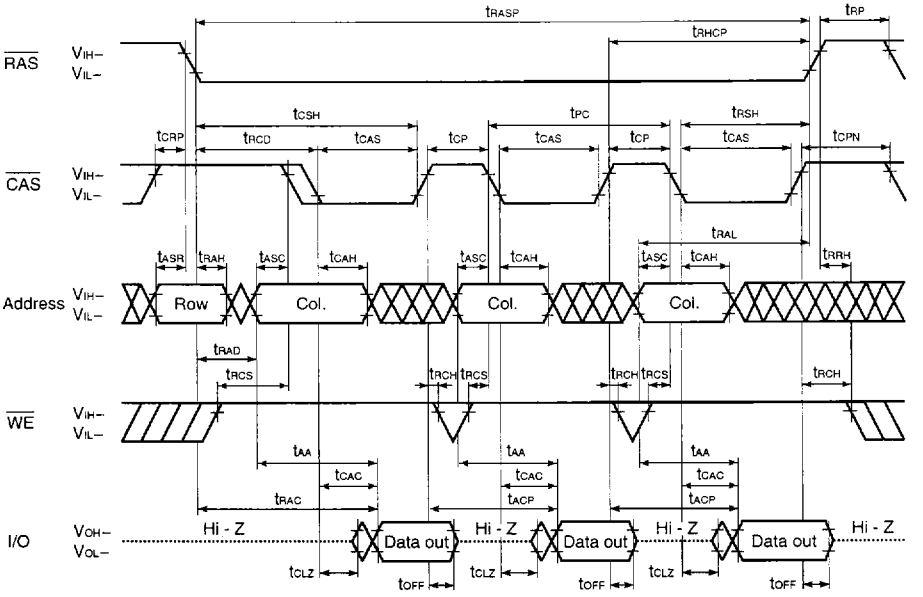
Read Cycle



Early Write Cycle

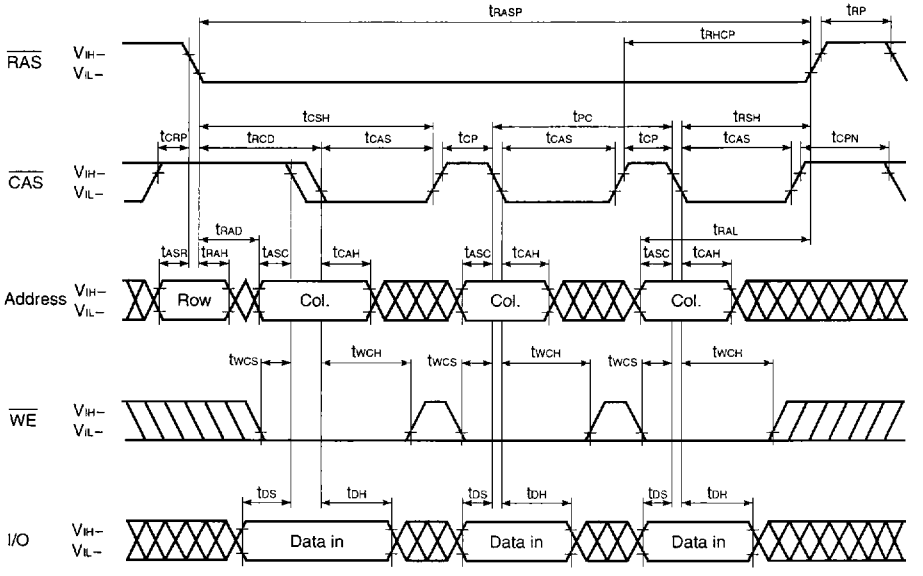


Fast Page Mode Read Cycle



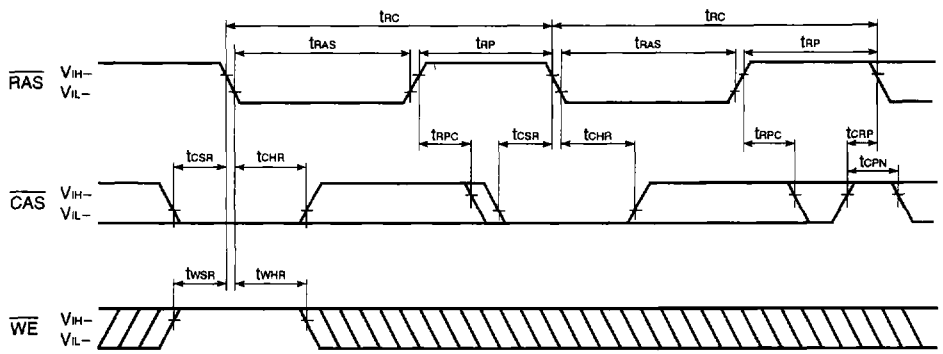
Remark In the fast page mode, read and write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Fast Page Mode Early Write Cycle



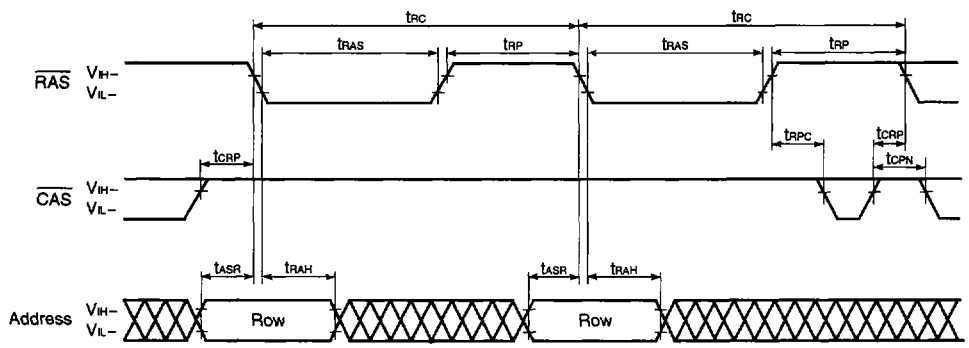
Remark In the fast page mode, read and write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



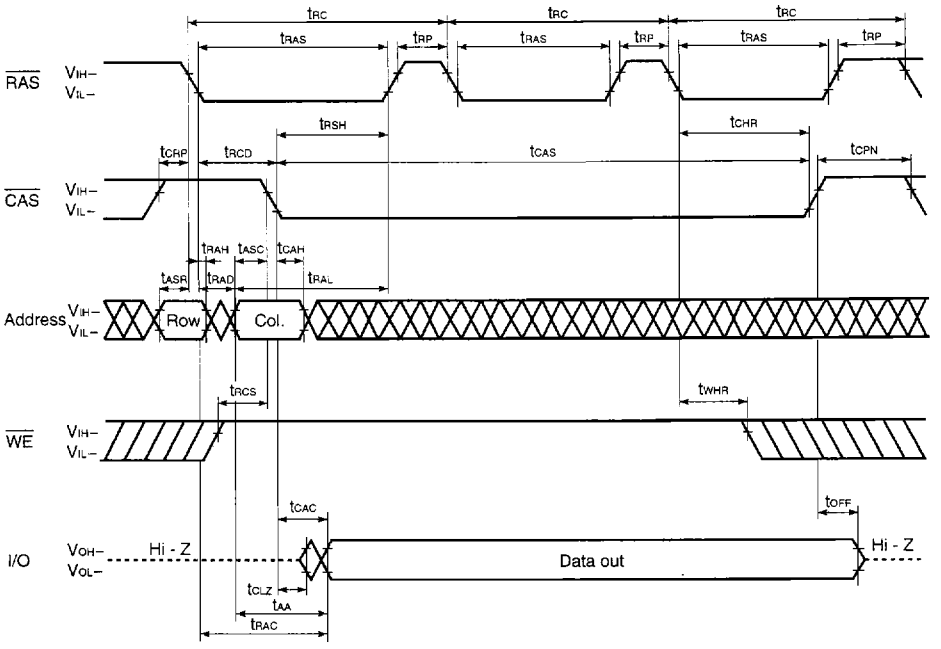
Remark Address = Don't care I/O = Hi - Z

$\overline{RAS}$ Only Refresh Cycle



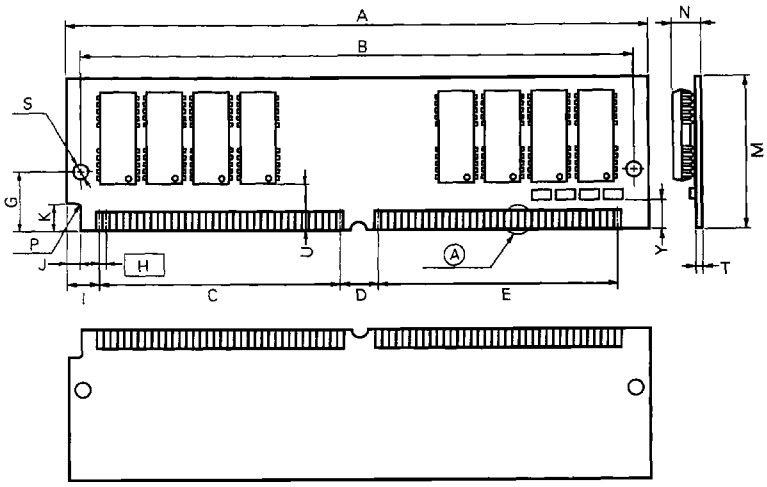
Remark $\overline{WE}$ = Don't care I/O = Hi - Z

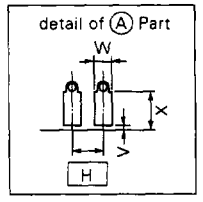
Hidden Refresh Cycle



Package Drawings

MC-421000A32B, 421000A32F
72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)

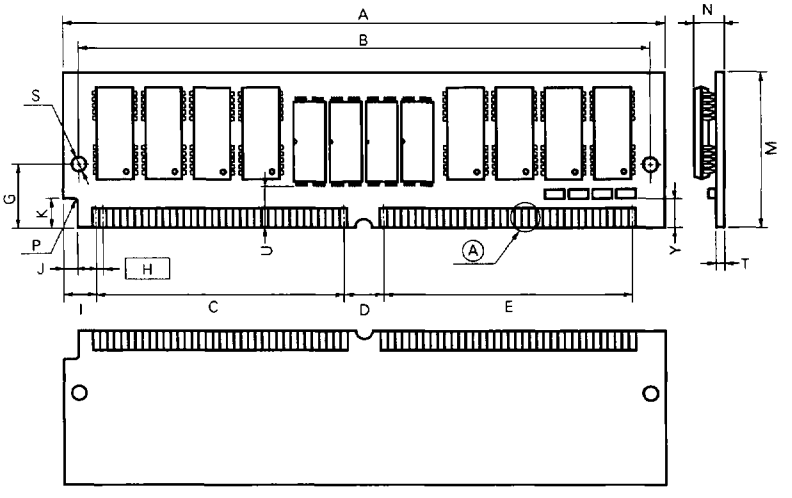


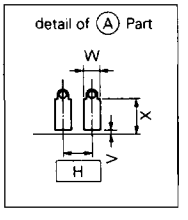


M72B-50A21-1

ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19	3.984
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	25.4	1.000
N	5.08 MAX.	0.200 MAX.
P	R 2.0	R 0.079
S	φ3.18	φ0.125
T	$1.27^{+0.1}_{-0.08}$	0.050±0.004
U	6.5 MIN.	0.255 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.
Y	3.75 MIN.	0.147 MIN.

MC-421000A36B, 421000A36F
72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)



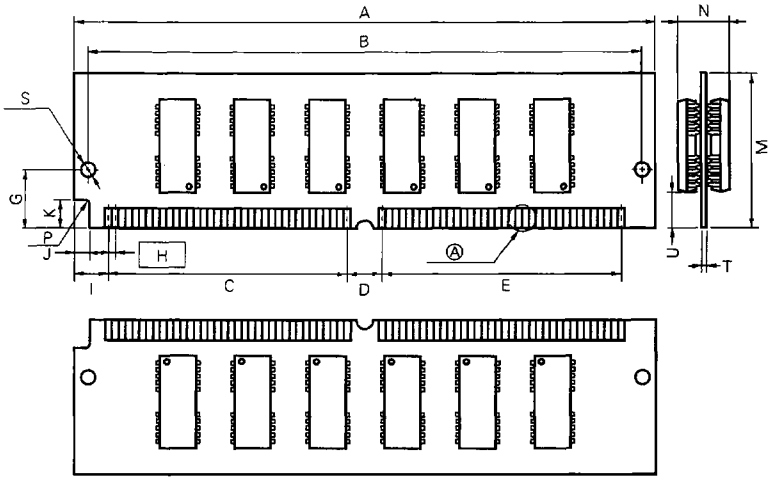


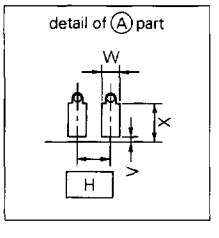
M72B-50A19-1

ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19	3.984
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	25.4	1.000
N	5.08 MAX.	0.200 MAX.
P	R 2.0	R 0.079
S	ϕ3.18	ϕ0.125
T	$1.27^{+0.1}_{-0.08}$	0.050±0.004
U	5.32 MIN.	0.209 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.
Y	3.75 MIN.	0.147 MIN.

MC-421000A36BE, 421000A36FE

72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)

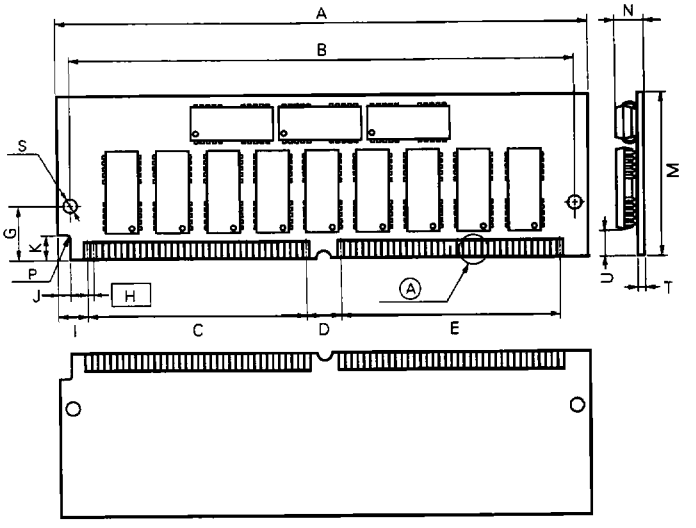


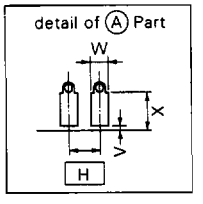


M72B-50A33-1

ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19	3.984
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	25.4	1.000
N	9.0 MAX.	0.355 MAX.
P	R 1.57	R 0.062
S	ϕ3.18	ϕ0.125
T	$1.27^{+0.1}_{-0.08}$	0.050±0.004
U	6.0 MIN.	0.236 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.

MC-421000A36BJ, 421000A36FJ
72 PIN SINGLE IN-LINE MODULE (SOCKET TYPE)





M72B-50A23-2

ITEM	MILLIMETERS	INCHES
A	107.95±0.13	4.250±0.006
B	101.19	3.984
C	44.45	1.750
D	6.35	0.250
E	44.45	1.750
G	10.16	0.400
H	1.27 (T.P.)	0.050 (T.P.)
I	6.35	0.250
J	2.03	0.080
K	6.35	0.250
M	31.75	1.250
N	5.08 MAX.	0.200 MAX.
P	R 2.0	R 0.079
S	ϕ3.18	ϕ0.125
T	$1.27^{+0.1}_{-0.08}$	0.050±0.004
U	3.78 MIN.	0.148 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.04±0.05	0.041±0.002
X	2.54 MIN.	0.100 MIN.