WD1100-04 CRC Generator/Checker

DESCRIPTION

The WD1100-04 CRC Generator / Checker is designed to generate a Cyclic Redundancy Checkword from a serial data stream, and to check a data stream against a known CRC word. Complimentary latched "CRCOK" outputs are provided to indicate CRC errors in check mode. Additional logic has been included to shift the CRC checkword out of the device by signals generated on other WD1100 family devices.

The WD1100-04 is fabricated in NMOS silicon gate technology and is available in a 20 pin dual-in-line package.

FEATURES

- GENERATES / CHECKS CRC
- SINGLE +5V SUPPLY
- LATCHED ERROR OUTPUTS
- $X^{16} + X^{12} + X^5$ 1(CCITT-16)
- AUTOMATIC RESET
- 20 PIN DIP PACKAGE

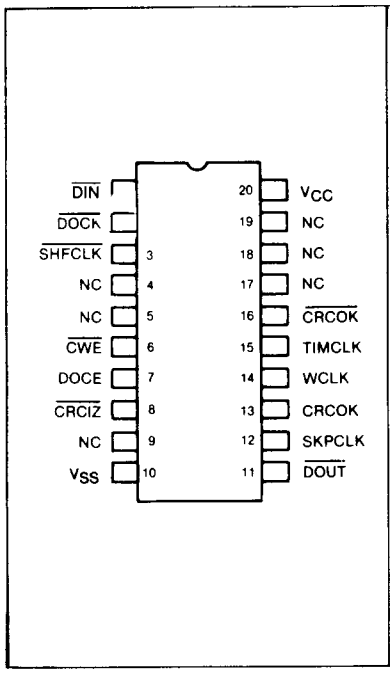

Figure 1.
WD1100-04 Pin Connections

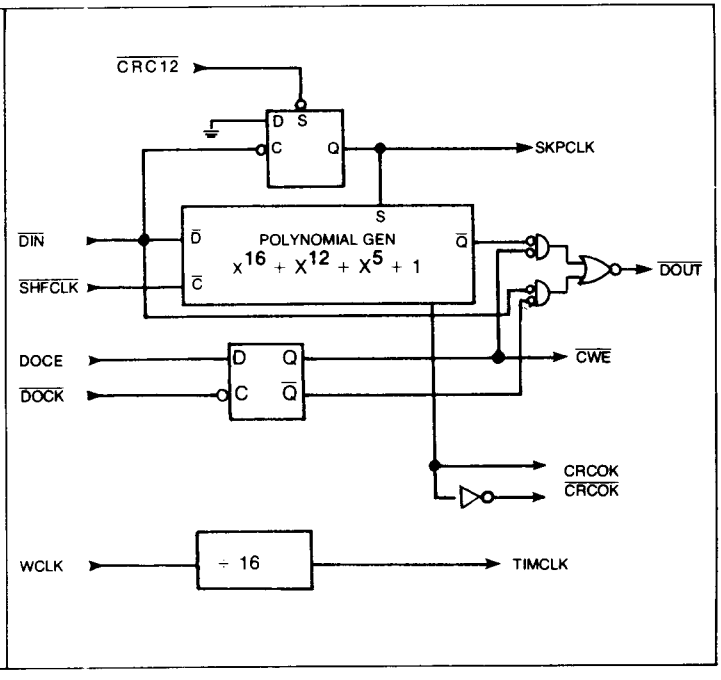

Figure 2.
WD1100-04 Block Diagram

PIN NUMBER	SYMBOL	NAME	FUNCTION
1	$\overline{DIN}$	$\overline{DATA\ INPUT}$	Active low serial input data stream is used to generate/check the 2 byte CRC word.
2	$\overline{DOCK}$	$\overline{DATA\ OR\ CRC\ WORD\ CLOCK}$	After a byte of data has been transferred in, this input signal is used to latch the state of DOCE in an internal D flop with a high to low transition.
3	$\overline{SHFCLK}$	$\overline{SHIFT\ CLOCK}$	The falling edge shifts data bits into the CRC generator/checker. It also transfers the CRC check word to DOUT in the write mode (DDCE = LOW). The rising edge also activates the CRCOK lines in the read mode when no error is found.
4,5	N.C.	NO CONNECTION	
6	$\overline{CWE}$	$\overline{CHECK\ WORD\ ENABLE}$	This active low output indicates that the CRC checkword is being output on the DOUT line. When $\overline{CWE}$ is high, data is being output on DOUT.
7	DOCE	DATA OR CRC ENABLE	Initially, this input line is held high to direct input data (pin 1) to the output data (pin 11). After the next to the last BYTE is transmitted but before the last BYTE occurs DOCE must be low to direct the 2 CRC check bytes to DOUT (pin 11). DOCE must be maintained low for a minimum of 2 byte times. DOCE is used only in the write mode.
8	$\overline{CRCIZ}$	$\overline{CYCLIC\ REDUNDANCY\ CHECK\ INITIALIZE}$	When this line is at a logic 0, the SKPCLK output line is held high and the CRC generator is held preset to hex "FFFF."
9	N.C.	NO CONNECTION	
10	V_{SS}	GROUND	GROUND.
11	$\overline{DOUT}$	$\overline{DATA\ OUTPUT}$	In the write mode, this line outputs the unmodified data stream along with the 2 byte CRC word appended to the end of the stream.
12	SKPCLK	SKIP CLOCK	The first high-to-low transition on $\overline{DIN}$ (pin 1) resets SKPCLK low and enables the CRC to either generate or check the CRC word.
13	CRCOK	CYCLIC REDUNDANCY CHECK OKAY	In the read mode, after the 2 byte CRC word is entered on DIN and no error has been detected, this line is set high to indicate no errors have occurred. This line will then remain high as long as DIN is maintained high.
14	WCLK	WRITE CLOCK	This input clock is divided by 16 to produce TIMCLK (pin 15) and has no effect on the rest of the internal circuitry.
15	TIMCLK	TIMING CLOCK	See WCLK (pin 14).
16	$\overline{CRCOK}$	$\overline{CYCLIC\ REDUNDANCY\ CHECK\ OKAY}$	Complementary output version of CRCOK (pin 13).
17-19	N.C.	NO CONNECTION	
20	V_{CC}	Power Supply	+5v ± 10% power supply.

DEVICE DESCRIPTION

Prior to shifting data through the device (either in the read or write modes) the CRC generator/checker is initialized by strobing the CRCIZ (pin 8) low. This forces the SKPCLK (pin 12) line to the high state. The first low going transition on DIN (pin 1), namely the most significant bit of an address mark, resets the SKPCLK line. The WD1100-04 has now been properly initialized and is ready to generate/check the CRC bytes. The CRCOK and CRCOK lines should be set to their inactive states.

In the write mode, initially the DOCE (pin 7) is held high and pseudo DOCK is produced by supplying a string of zeros before the address mark. This ensures the proper state of the internal D flip flop to gate input data to the output line DOUT (pin 11). As shown in the block diagram the CWE (pin 6) will be set high. Sometime between the next to the last and the last DOCK that indicates the end of the data stream, DOCE (pin 7) is lowered to ensure the smooth transition of the 2 byte CRC checkword to the output line DOUT (pin 11).

DOCE must be maintained low for a minimum of 2 byte times. After the CRC word is generated, DOUT will produce a string of zeroes (i.e., held high). This portion of the circuitry is dormant in the read mode. After proper initialization, input data is entered on DIN (pin 1) along with the 2 byte CRC word for the read mode of operation. At the end of the data stream, if no errors were detected the CRCOK (pin 13) is set high. Accordingly the complimentary output (pin 16) is set low. These output states will be maintained as long as DIN is held high and CRCIZ (pin 8) is not strobed. If the CRCOK lines do not become active, an error has been detected and a retry is in order. If successive re-tries fail, an error flag may be set to determine a further course of action as desired by the user.

WCLK is divided by 16 to produce TIMCLK which may be used as a buffered step clock for SA1000 compatible drives.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias . . . . . 0°C (32°F) to 50°C (122°F)
Voltage on any pin with respect to V_{SS} . . . . . -0.2V to +7.0V
Power Dissipation . . . . . 1 Watt

STORAGE TEMPERATURE
PLASTIC . . . . . -55°C (-67°F) to + 125°C (257°F)
CERAMIC . . . . -55°C (-67°F) to + 150°C (302°F)

NOTE: Maximum ratings indicate operation where permanent device damage may occur. Continuous operations at these limits is not intended and should be limited to those conditions specified in the DC electrical characteristics.

DC Electrical Characteristics T_A = 0°C (32°F) to 50°C (122°F); V_{CC} = +5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITIONS
V_{IL}	Input Low Voltage	-0.2		0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4			V	I_{0H} = -200μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			125	mA	All Outputs Open
I_{IH}	Current Input High			<10	uA	V_{IN} = .4 to V_{CC}
I_{IL}	Current Input Low			<10	uA	V_{IN} = .4 to V_{CC}

AC Electrical Characteristics T_A = 0°C (32°F) to 50°C (122°F); V_{CC} = 5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN.	TYP[1]	MAX.	UNITS	CONDITION
t_{WT}	↑ WCLK to ↓ TIMCLK			140	nsec	
t_{ZS}	CRCIZ ↓ to ↑ SKPCLK			120	nsec	
t_{ZK}	CRCIZ pulse width	90			nsec	
t_{BS}	DOCE set up time w.r.t. ↓ DOCK	20			nsec	
t_{BH}	DOCE hold time w.r.t. ↓ DOCK	40			nsec	
t_{DD}	DIN to DOUT delay			105	nsec	CWE set high

SYMBOL	PARAMETER	MIN.	TYP[1]	MAX.	UNITS	CONDITION
t_{DK}	↓ $\overline{DIN}$ to ↓ SKPCLK			120	nsec	
t_{DW}	$\overline{DIN}$ P.W. to reset SKPCLK	50			nsec	
t_{IC}	↓ $\overline{DOCK}$ to ↑ $\overline{CWE}$			120	nsec	
t_{SD}	$\overline{SHFCLK}$ to $\overline{DOUT}$			150	nsec	
t_{BC}	↓$\overline{DOCK}$ to ↑$\overline{CWE}$			120	nsec	
f_{SC}	$\overline{SHFCLK}$ frequency			5.25	MHz	
t_{SR}	↑ $\overline{SHFCLK}$ to ↑ $\overline{CRCOK}$			85	nsec	
t_{SC}	↑$\overline{SHFCLK}$ to ↓ $\overline{CRCOK}$			90	nsec	
t_{IN}	↓ $\overline{DOCK}$ to ↓ $\overline{DIN}$			90	nsec	

NOTE: 1. Typical Values are for T_A = 25°C (77°F) and V_{CC} = +5.0V

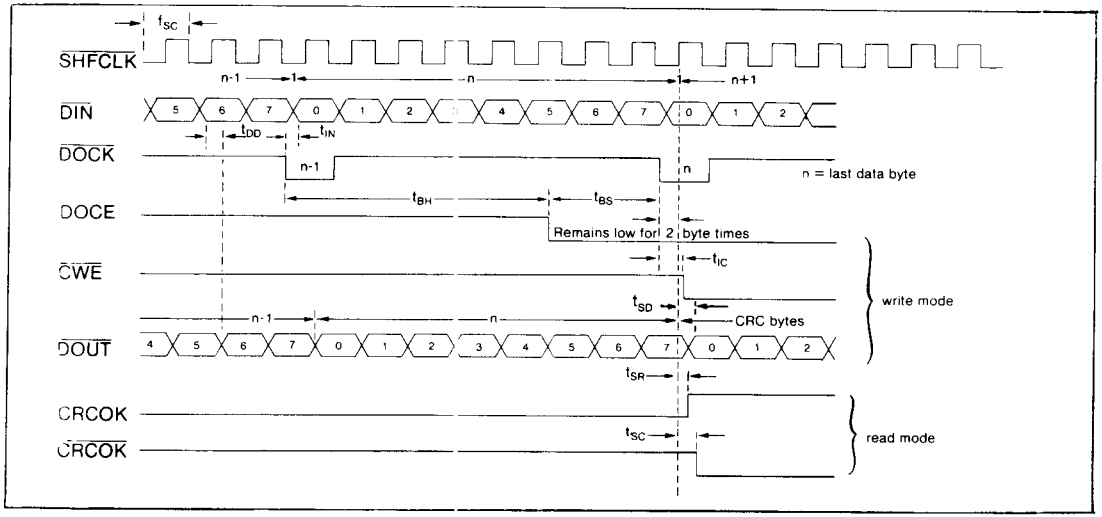

Figure 3.
WD1100-04 Write Mode

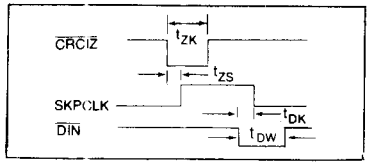

Figure 4.
WD1100-04 Initialize