TM4164FL8, TM4164FM8
65,536 BY 8-BIT DYNAMIC RAM MODULES

NOVEMBER 1983 — REVISED NOVEMBER 1985

- 65,536 X 8 Organization
- Single 5-V Supply (10% Tolerance)
- 30-Pin Single-in-Line Package (SIP)
- Utilizes Eight 64K Dynamic RAMs in Plastic Chip Carrier
- Long Refresh Period . . . 4 ms (256 Cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance Ranges:

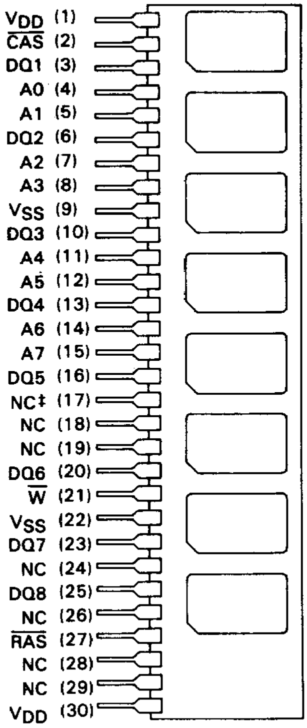
	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)
TM4164__8-12	120 ns	75 ns	230 ns
TM4164__8-15	150 ns	90 ns	260 ns
TM4164__8-20	200 ns	135 ns	326 ns

- Common $\overline{\text{CAS}}$ Control for Eight Common Data-In and Data-Out Lines
- Low Power Dissipation:

	OPERATING (TYP)	STANDBY (TYP)
TM4164__8-12	1600 mW	140 mW
TM4164__8-15	1400 mW	140 mW
TM4164__8-20	1080 mW	140 mW

- Operating Free-Air Temperature . . . 0 °C to 70 °C

TM4164FL8 . . . L SINGLE-IN-LINE PACKAGE[†]
TM4164FM8 . . . M SINGLE-IN-LINE PACKAGE
(TOP VIEW)



[†] TM4164FL8 package is shown.

[‡] Pin 17 of the 256K x 8 SIP is memory address A8.

description

The TM4164__8 series are 512K, dynamic random-access memory modules organized as 65,536 × 8-bits in a 30-pin single-in-line package comprising eight TMS4164FPL, 65,536 × 1-bit dynamic RAM's in 18-lead plastic chip carriers mounted on top of a substrate together with eight 0.1 μF decoupling capacitors mounted beneath the chip carriers. The onboard capacitors eliminate the need for bypassing on the motherboard and offer superior performance over equivalent leaded capacitors due to reduced lead inductance. Also, with 0.3 inch board spacing the TM4164_8 has a density of 8.5 devices per square inch (approximately 3.5X the density of of DIPs). With the elimination of bypass capacitors on the motherboard, reduced PC board size, and fewer plated-through holes, a cost savings can be realized.

PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{\text{CAS}}$	Column-Address Strobe
DQ1-DQ8	Data In/Data Out
NC	No Connection
$\overline{\text{RAS}}$	Row-Address Strobe
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{\text{W}}$	Write Enable

The TM4164__8 features $\overline{\text{RAS}}$ access times of 120 ns, 150 ns, and 200 ns maximum. Power dissipation as low as 1080 mW typical operating and 140 mW typical standby.

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with $\overline{\text{RAS}}$ in order to retain data. $\overline{\text{CAS}}$ can remain high during the refresh sequence to conserve power.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address lines and data in are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TM4164__8 is rated for operation from 0°C to 70°C.

operation

address (A0 through A7)

Sixteen address bits are required to decode 1 of 65,536 storage cell locations on each of the eight chips. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe ($\overline{\text{RAS}}$). Then the eight column-address bits are set up on pins A0 through A7 and latched onto the chip by the column-address strobes. All addresses must be stable on or before the falling edges of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$. $\overline{\text{RAS}}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{\text{CAS}}$ is used as a chip select activating the column decoder and the input and output buffers for M1-M8.

write enable ($\overline{\text{W}}$)

The read or write mode is selected through the write-enable ($\overline{\text{W}}$) input. A logic high on the $\overline{\text{W}}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data inputs are disabled when the read mode is selected. The common I/O feature of the TM4164__8 dictates the use of early write cycles to prevent contention on D and Q. When $\overline{\text{W}}$ goes low prior to $\overline{\text{CAS}}$, the data outs will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data in (DQ1-DQ8)

Data is written during a write cycle. The falling edge of $\overline{\text{CAS}}$ or $\overline{\text{W}}$ strobes data into the on-chip data latches. These latches can be driven from standard TTL circuits without a pull-up resistor. In the early write cycle, $\overline{\text{W}}$ is brought low prior to $\overline{\text{CAS}}$ and the data is strobed in by $\overline{\text{CAS}}$ with setup and hold times referenced to this signal.

data out (DQ1-DQ8)

The three-state output buffers provide direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads for each output. Data out is the same polarity as data in. In a read cycle the outputs go active after the access time interval t_a(C) that begins with the negative transition of $\overline{\text{CAS}}$ as long as t_a(R) is satisfied. The outputs become valid after the access time has elapsed and remains valid while $\overline{\text{CAS}}$ is low; $\overline{\text{CAS}}$ going high returns it to a high-impedance state. In the early write cycle, the outputs are always in the high-impedance state, a necessity due to the common I/O feature of the TM4164_8.

refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffers are in the high-impedance state unless $\overline{\text{CAS}}$ is applied, the $\overline{\text{RAS}}$-only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with $\overline{\text{RAS}}$ causes all bits in each row to be refreshed. $\overline{\text{CAS}}$ can remain high (inactive) for this refresh sequence to conserve power.

page mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the module. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. To extend beyond the 256 column locations on M1-M8, the row address and $\overline{\text{RAS}}$ are applied to multiple modules. $\overline{\text{CAS}}$ is then decoded to select the proper module.

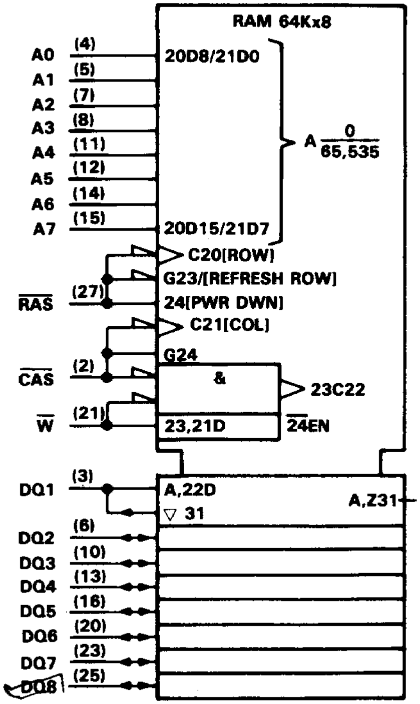
power up

After power up, the power supply must remain at its steady-state value for 1 ms. In addition, $\overline{\text{RAS}}$ must remain high for 100 µs immediately prior to initialization. Initialization consists of performing eight $\overline{\text{RAS}}$ cycles before proper device operation is achieved.

single-in-line package and components

PC substrate: 0,79 mm (0.031 inch) minimum thickness
Bypass capacitors: Multilayer ceramic
Leads: Tin/lead solder coated over phosphor-bronze
Contact area for socketable devices: Nickel plate and solder plate on top of copper

logic symbol†



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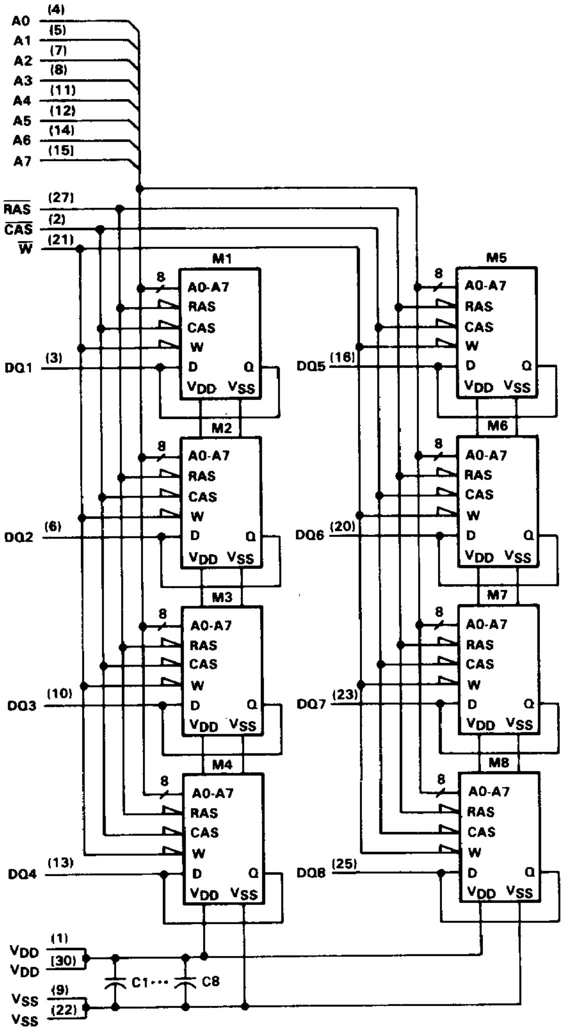
† This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin except V_{DD} and data out (see Note 1) . . . . -1.5 V to 10 V
Voltage range on V_{DD} supply and data out with respect to V_{SS} . . . . -1 V to 6 V
Short circuit output current for any output . . . . 50 mA
Power dissipation . . . . 8 W
Operating free-air temperature range . . . . 0°C to 70°C
Storage temperature range . . . . -65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		4.5	5	5.5	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage	V_{DD} = 4.5 V	2.4		4.8	V
		V_{DD} = 5.5 V	2.4		6	
V_{IL}	Low-level input voltage (see Notes 2 and 3)		-0.6		0.8	V
T_A	Operating free-air temperature		0		70	°C

NOTES: 2. The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

3. Due to input protection circuitry, the applied voltage may begin to clamp at -0.6 V. Test conditions should comprehend this occurrence. See application report entitled "TMS4164A and TMS4416 Input Protection Diode" on page 9-5.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TM4164__8-12			TM4164__8-15			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	$I_{OH} = -5$ mA	2.4			2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5 V, All other pins = 0 V			±10			±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V, $\overline{\text{CAS}}$ high			±10			±10	μA
I_{DD1}‡	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open		320	384		280	360	mA
I_{DD2}‡	Standby current	After 1 memory cycle, $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ high, All outputs open		28	40		28	40	mA
I_{DD3}‡	Average refresh current	t_c = minimum cycle, $\overline{\text{CAS}}$ high and $\overline{\text{RAS}}$ cycling, All outputs open		224	320		200	296	mA
I_{DD4}‡	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{\text{RAS}}$ low and $\overline{\text{CAS}}$ cycling, All outputs open		224	320		200	296	mA

† All typical values are at T_A = 25°C and nominal supply voltages.

‡ I_{DD1}-I_{DD4} are measured with M1-M8 in the same mode (i.e., operating, standby, refresh or page mode).

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TM4164__8-20			UNIT
			MIN	TYP[†]	MAX	
V_{OH}	High-level output voltage	$I_{OH} = -5$ mA	2.4			V
V_{OL}	Low-level output voltage	$I_{OL} = 4.2$ mA			0.4	V
I_I	Input current (leakage)	$V_I = 0$ V to 5.8 V, $V_{DD} = 5$ V, All other pins = 0 V			± 10	μA
I_O	Output current (leakage)	$V_O = 0.4$ V to 5.5 V, $V_{DD} = 5$ V, $\overline{CAS}$ high			± 10	μA
I_{DD1}[‡]	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open		216	296	mA
I_{DD2}[‡]	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		28	40	mA
I_{DD3}[‡]	Average refresh current	t_c = minimum cycle, $\overline{CAS}$ high and $\overline{RAS}$ cycling, All outputs open		160	256	mA
I_{DD4}[‡]	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, All outputs open		160	256	mA

[†] All typical values are at $T_A = 25°C$ and nominal supply voltages.

[‡] I_{DD1}-I_{DD4} are measured with M1-M8 in the same mode (i.e., operating, standby, refresh or page mode).

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs	40	pF
$C_{i(DQ)}$	Input capacitance, data inputs	11	pF
$C_{i(RAS)}$	Input capacitance, $\overline{RAS}$ input	64	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$ input	64	pF
$C_{i(CAS)}$	Input capacitance, $\overline{CAS}$ input	64	pF

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TM4164__8-12		TM4164__8-15		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	$C_L = 100$ pF, Load = 2 Series 74 TTL gates	t_{CAC}		75		90	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, Load = 2 Series 74 TTL gates	t_{RAC}		120		150	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	$C_L = 100$ pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	40	0	40	ns

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TM4164__8-20		UNIT
				MIN	MAX	
$t_{a(C)}$	Access time from $\overline{\text{CAS}}$	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		135	ns
$t_{a(R)}$	Access time from $\overline{\text{RAS}}$	t_{RLCL} = MAX, Load = 2 Series 74 TTL gates	t_{RAC}		200	ns
$t_{dis(CH)}$	Output disable time after $\overline{\text{CAS}}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	50	ns

timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TM4164__8-12		TM4164__8-15		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page-mode cycle time	t_{PC}	130		160		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	230		260		ns
$t_{c(W)}$	Write cycle time	t_{WC}	230		260		ns
$t_{w(CH)}$	Pulse duration, $\overline{\text{CAS}}$ high (precharge time)‡	t_{CP}	50		50		ns
$t_{w(CL)}$	Pulse duration, $\overline{\text{CAS}}$ low	t_{CAS}	75	10,000	90	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{\text{RAS}}$ high (precharge time)	t_{RP}	80		100		ns
$t_{w(RL)}$	Pulse duration, $\overline{\text{RAS}}$ low	t_{RAS}	120	10,000	150	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	40		45		ns
t_t	Transition times (rise and fall) for $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ †	t_T	10	50	10	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{\text{CAS}}$ high	t_{CWL}	50		50		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{\text{RAS}}$ high	t_{RWL}	50		50		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{\text{CAS}}$ low	t_{CAH}	40		45		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	20		25		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{\text{RAS}}$ low	t_{AR}	85		100		ns
$t_{h(CLD)}$	Data hold time after $\overline{\text{CAS}}$ low	t_{DHC}	45		50		ns
$t_{h(RLD)}$	Data hold time after $\overline{\text{RAS}}$ low	t_{DHR}	90		100		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{\text{CAS}}$ high	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{\text{RAS}}$ high	t_{RRH}	5		5		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{\text{CAS}}$ low	t_{WCH}	45		50		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{\text{RAS}}$ low	t_{WCR}	90		100		ns
t_{RLCH}	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ high	t_{CSH}	120		150		ns
t_{CHRL}	Delay time, $\overline{\text{CAS}}$ high to $\overline{\text{RAS}}$ low	t_{CRP}	0		0		ns
t_{CLRH}	Delay time, $\overline{\text{CAS}}$ low to $\overline{\text{RAS}}$ high	t_{RSH}	60		100		ns
t_{RLCL}	Delay, time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ low (maximum value specified only to guarantee access time)	t_{RCD}	25	45	30	60	ns
t_{WLCL}	Delay time, $\overline{\text{W}}$ low to $\overline{\text{CAS}}$ low (early write cycle)	t_{WCS}	0		0		ns
t_{rf}	Refresh time interval	t_{REF}		4		4	ms

NOTE 4: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

†All cycle times assume t_t = 5 ns. The specified t_t = is due to testing limitations. Transition times may be as little as 3 ns in system use.

‡Page mode only.

timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TM4164__8-20		UNIT
			MIN	MAX	
$t_{c(P)}$	Page-mode cycle time	t_{PC}	206		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	326		ns
$t_{c(W)}$	Write cycle time	t_{WC}	326		ns
$t_{w(CH)}$	Pulse duration, $\overline{\text{CAS}}$ high (precharge time)‡	t_{CP}	80		ns
$t_{w(CL)}$	Pulse duration, $\overline{\text{CAS}}$ low	t_{CAS}	135	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{\text{RAS}}$ high (precharge time)	t_{RP}	120		ns
$t_{w(RL)}$	Pulse duration, $\overline{\text{RAS}}$ low	t_{RAS}	200	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	55		ns
t_t	Transition times (rise and fall) for $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$†	t_T	10	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{\text{CAS}}$ high	t_{CWL}	60		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{\text{RAS}}$ high	t_{RWL}	60		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{\text{CAS}}$ low	t_{CAH}	55		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	30		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{\text{RAS}}$ low	t_{AR}	125		ns
$t_{h(CLD)}$	Data hold time after $\overline{\text{CAS}}$ low	t_{DHC}	60		ns
$t_{h(RLD)}$	Data hold time after $\overline{\text{RAS}}$ low	t_{DHR}	145		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{\text{CAS}}$ high	t_{RCH}	0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{\text{RAS}}$ high	t_{RRH}	5		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{\text{CAS}}$ low	t_{WCH}	60		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{\text{RAS}}$ low	t_{WCR}	145		ns
t_{RLCH}	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ high	t_{CSH}	200		ns
t_{CHRL}	Delay time, $\overline{\text{CAS}}$ high to $\overline{\text{RAS}}$ low	t_{CRP}	0		ns
t_{CLRH}	Delay time, $\overline{\text{CAS}}$ low to $\overline{\text{RAS}}$ high	t_{RSH}	135		ns
t_{RLCL}	Delay, time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ low (maximum value specified only to guarantee access time)	t_{RCD}	35	65	ns
t_{WLCL}	Delay time, $\overline{\text{W}}$ low to $\overline{\text{CAS}}$ low (early write cycle)	t_{WCS}	0		ns
t_{rf}	Refresh time interval	t_{REF}		4	ms

NOTE 4: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

† All cycle times assume t_t = 5 ns. The specified t_t = is due to testing limitations. Transition times may be as little as 3 ns in system use.

‡ Page mode only.

PARAMETER MEASUREMENT INFORMATION

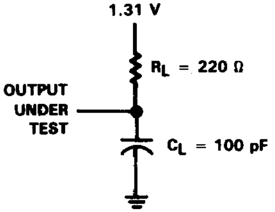
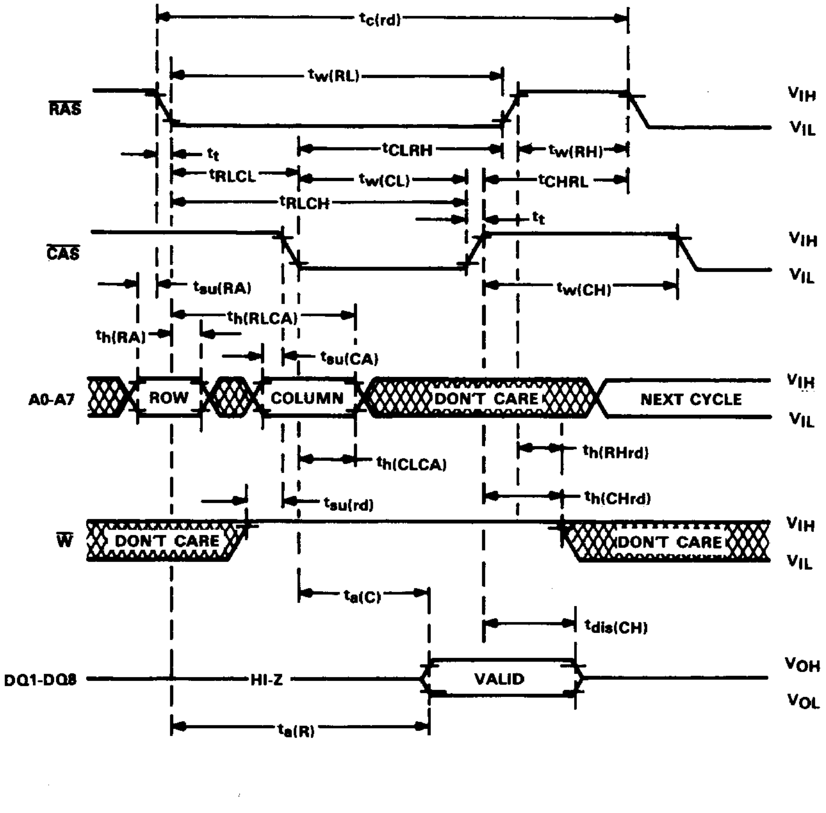
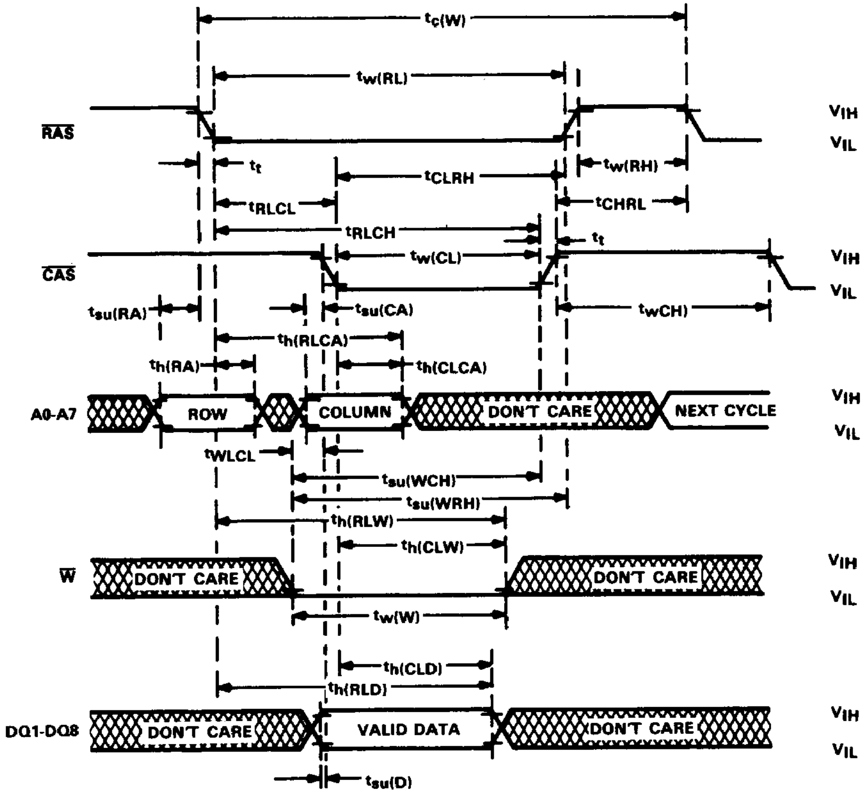


FIGURE 1. LOAD CIRCUIT

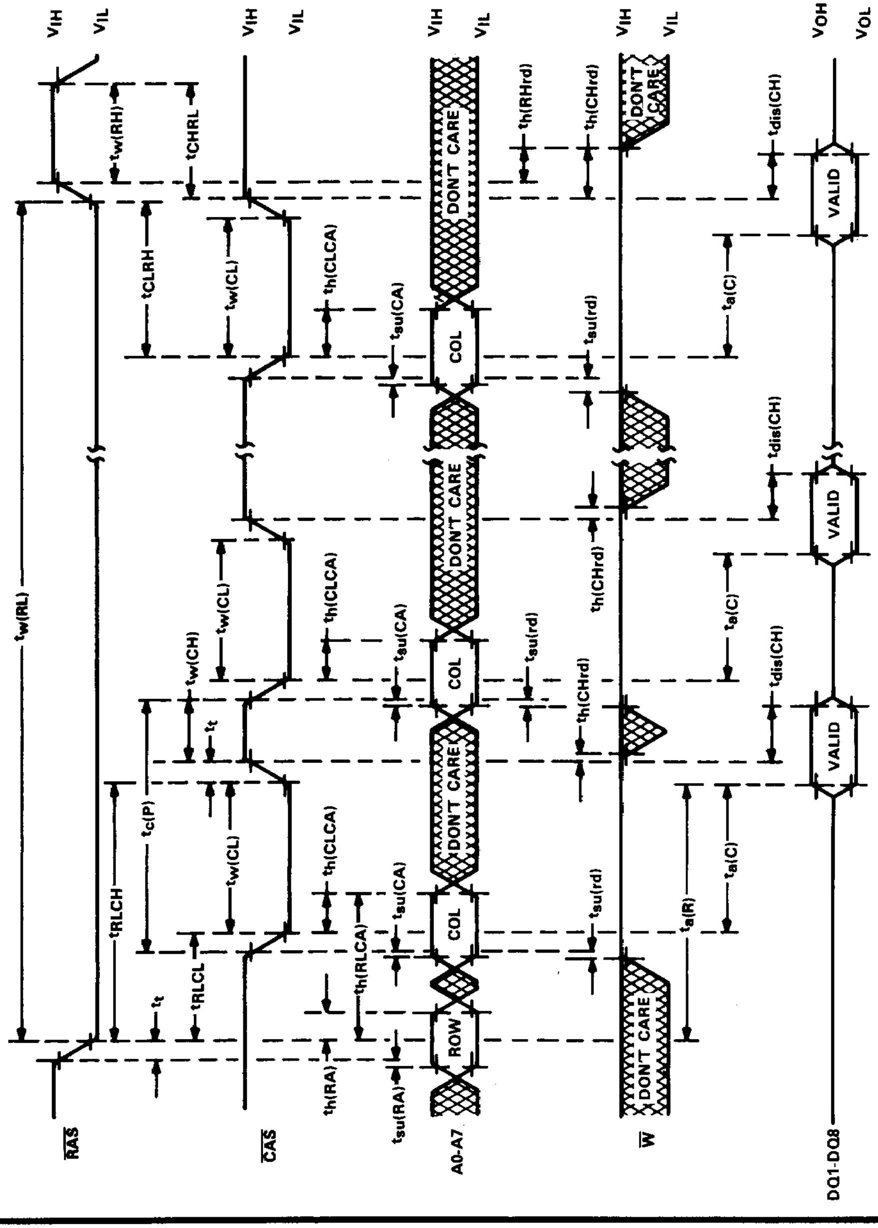
read cycle timing



early write cycle timing

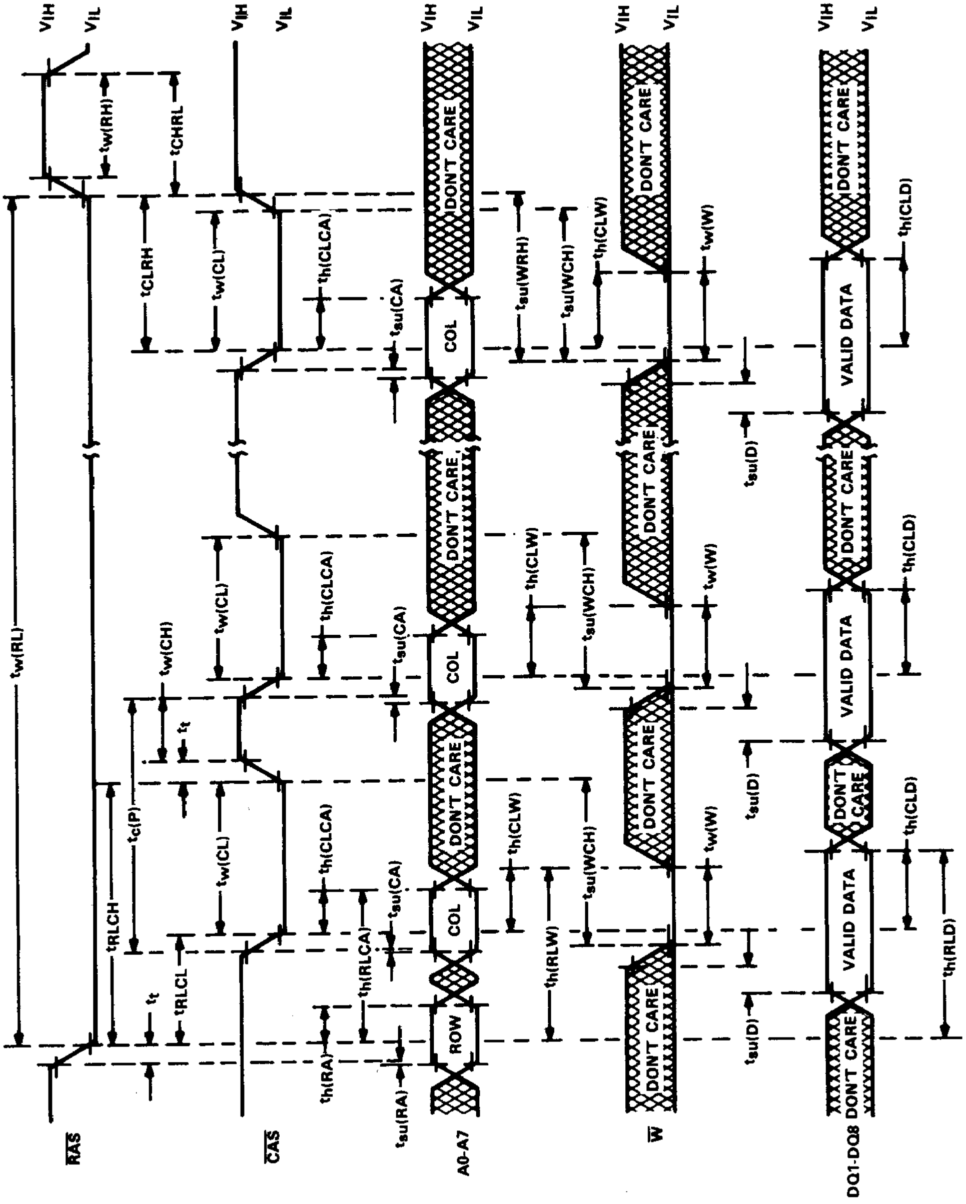


page-mode read cycle timing



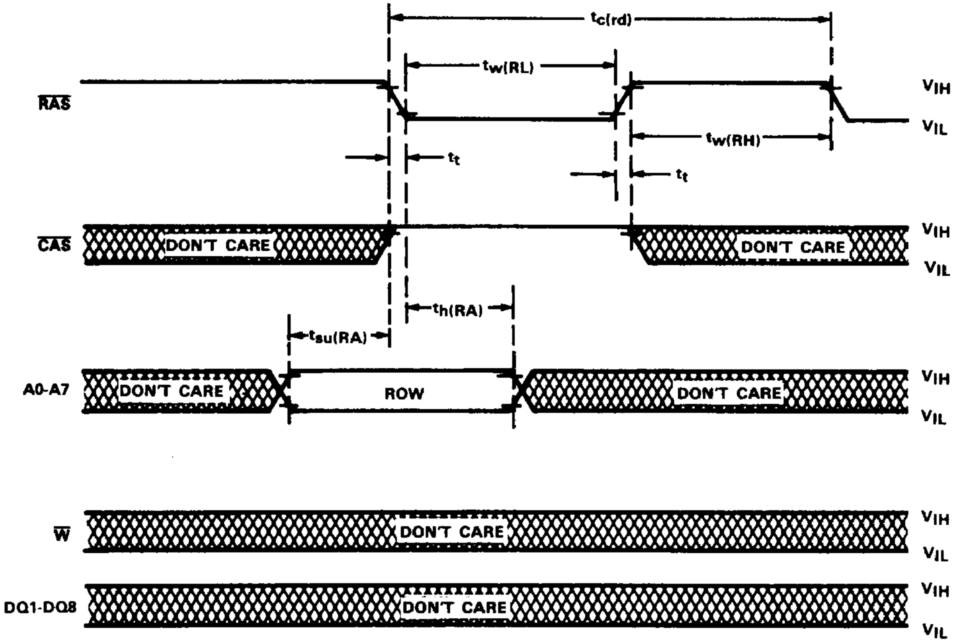
NOTE 5: A write cycle or a read-modify-write cycle can be intermixed with read cycles as long as the write and read-modify-write timing specifications are not violated.

page-mode write cycle timing

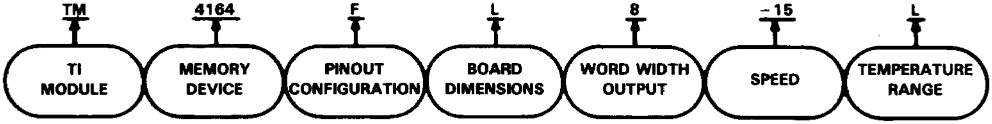


NOTE 6: A read cycle or a read-modify-write can be intermixed with write cycles as long as the read and read-modify-write timing specifications are not violated.

$\overline{\text{RAS}}$-only refresh timing



TI single-in-line package nomenclature



L Package
(76,2 x 16,5 mm)
(3.1 x 0.65 inches)
M Package
(88,9 x 15,24 mm)
(3.5 x 0.60 inches)

Max Access
−12 120 ns
−15 150 ns
−20 200 ns

L 0°C to 70°C