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The S-2812A and the S-2817A are low power 2Kx8-bit parallel E<sup>2</sup>PROMs. The S-2812A features wide operating voltage range, and the S-2817A features 5-V single power supply. Since provided with 32-byte page write function, they can perform fast programming operation.

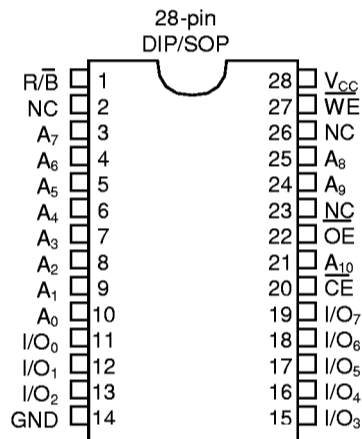
■ Features

- Access time: 150 ns  
(V<sub>CC</sub>=5 V±10%, T<sub>a</sub>=0°C to 70°C)
- Low power consumption  
Operating: 30 mA max. (V<sub>CC</sub>=5 V±10%)  
Standby: 1 μA max. (V<sub>CC</sub>=5 V±10%)
- Operating voltage range  

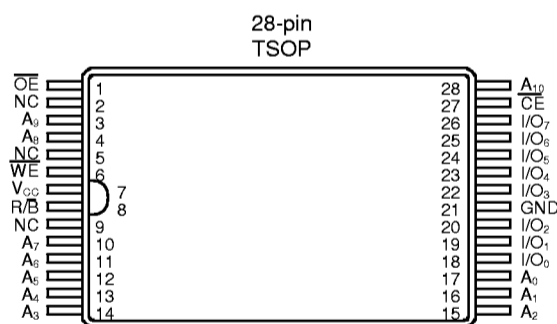
<u>S-2812A</u>	<u>S-2817A</u>
Read: 1.8 to 5.5 V	5 V±10%
Write: 2.7 to 5.5 V	5 V±10%
- Write inhibition  

S-2812A:	2.1 V typ.
S-2817A:	3.5 V typ.
- Data polling
- With Ready/Busy pin
- Page write for 32 bytes
- Rewritings: 10<sup>5</sup> times
- Data retention: 10 years
- Program noise immunity
- Package: 28-pin DIP/SOP/TSOP
- Supply in bare chip is also available

■ Pin Assignment



Pin name	Function
A <sub>0</sub> to A <sub>10</sub>	Address input
I/O <sub>0</sub> to I/O <sub>7</sub>	Data input / output
<u>CE</u>	Chip Enable
<u>OE</u>	Output Enable
<u>WE</u>	Write Enable
R/ <u>B</u>	Ready/Busy (opendrain output)
V <sub>CC</sub>	Power supply voltage
GND	Ground (0 V)



Figure

**CMOS 16K-bit PARALLEL E<sup>2</sup>PROM  
S-2812A/2817A**

■ **Block Diagram**

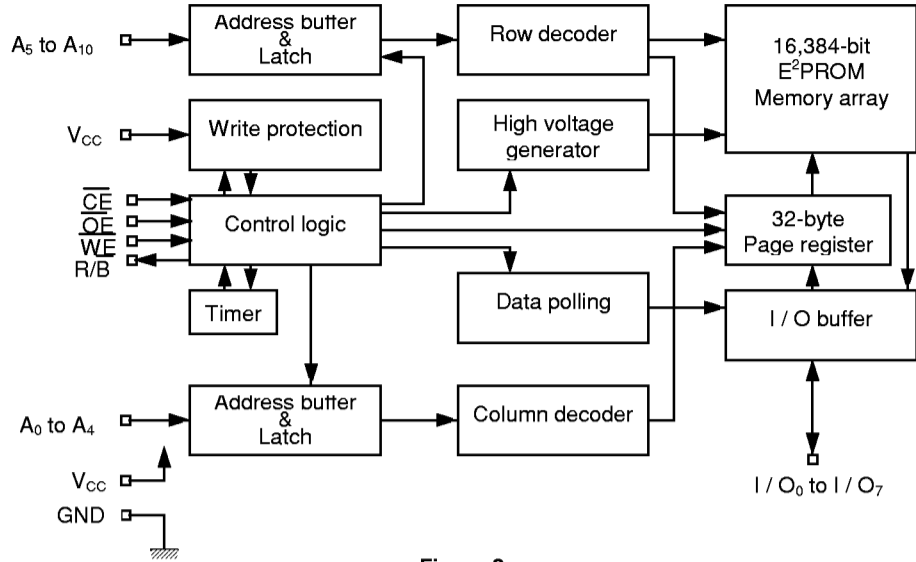


Figure 2

■ **Operation Mode**

Table 1

Mode	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	I/O
Read	L	L	H	Data output
Write	L	H	L	Data input
Write inhibition	x	x	H	—
	x	L	x	—
Standby	H	x	x	High-Z

■ **Absolute Maximum Ratings**

Table 2

Parameter	Symbol	Ratings	Unit
Power supply voltage	V <sub>CC</sub>	-0.3 to +7.0	V
Input voltage	V <sub>IN</sub>	-0.3 to V <sub>CC</sub> +0.3	V
Output voltage	V <sub>OUT</sub>	-0.3 to V <sub>CC</sub>	V
Storage temperature under bias	T <sub>bias</sub>	-50 to +95	°C
Storage temperature	T <sub>stg</sub>	-65 to +150	°C

■ **Recommended Operating Conditions**

Table 3

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
Power supply voltage	V <sub>CC</sub>	S-2812A	Read	1.8	—	5.5	V
			Write	2.7	—	5.5	V
		S-2817A		4.5	5.0	5.5	V
High level input voltage	V <sub>IH</sub>	V <sub>CC</sub> =2.7 to 5.5 V	2.2	—	V <sub>CC</sub> +0.3	V	
		V <sub>CC</sub> =1.8 to 2.7 V	0.8×V <sub>CC</sub>	—	V <sub>CC</sub> +0.3	V	
Low level input voltage	V <sub>IL</sub>	V <sub>CC</sub> =5 V ±10%	-0.3	—	0.8	V	
		V <sub>CC</sub> =2.7 to 4.5 V	-0.3	—	0.4	V	
		V <sub>CC</sub> =1.8 to 2.7 V	-0.3	—	0.2×V <sub>CC</sub>	V	
Operating temperature	T <sub>opr</sub>		-40	—	85	°C	

■ DC Electrical Characteristics

1. S-2812A

Table 4

(Ta=-40°C to 85°C)

Parameter	Symbol	Conditions	5 V±10%			3 V±10%			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Current consumption (Read)	I <sub>CC1</sub>	$\overline{CE} \leq V_{IL}, V_{IN} \leq V_{IL} \text{ or } V_{IN} \geq V_{IH}$ I <sub>OUT</sub> =0 mA, f=1/t <sub>RC</sub>	—	—	30	—	—	15	mA
	I <sub>CC2</sub>	$\overline{CE} \leq 0.2 \text{ V}, V_{IN} \leq 0.2 \text{ V or } V_{IN} \geq V_{CC} - 0.2 \text{ V}$ I <sub>OUT</sub> =0 mA, f=1/t <sub>RC</sub>	—	—	25	—	—	10	mA
Current consumption (Program)	I <sub>CC3</sub>	$\overline{CE} \leq V_{IL}, V_{IN} \leq V_{IL} \text{ or } V_{IN} \geq V_{IH}$	—	—	30	—	—	15	mA
	I <sub>CC4</sub>	$\overline{CE} \leq 0.2 \text{ V}, V_{IN} \leq 0.2 \text{ V or } V_{IN} \geq V_{CC} - 0.2 \text{ V}$	—	—	25	—	—	10	mA
Standby current	I <sub>SB1</sub>	$\overline{CE} \geq V_{IH}$	—	—	1	—	—	0.5	mA
	I <sub>SB2</sub>	$\overline{CE} \geq V_{CC} - 0.2 \text{ V}$	—	—	1.0	—	—	1.0	μA
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> =GND to V <sub>CC</sub>	—	—	1.0	—	—	1.0	μA
Output leakage current	I <sub>LO</sub>	V <sub>I/O</sub> =GND to V <sub>CC</sub>	—	—	1.0	—	—	1.0	μA
High level output voltage	V <sub>OH</sub>	5-V operation: I <sub>OH</sub> =-400 μA 3-V operation: I <sub>OH</sub> =-100 μA	2.4	—	—	2.4	—	—	V
Low level output voltage	V <sub>OL</sub>	5-V operation: I <sub>OL</sub> =2.1 mA 3-V operation: I <sub>OL</sub> =400 μA	—	—	0.4	—	—	0.4	V

2. S-2817A

Table 5

(Ta=-40°C to 85°C, V<sub>CC</sub>=5 V±10%)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consumption (Read)	I <sub>CC1</sub>	$\overline{CE} \leq V_{IL}, V_{IN} \leq V_{IL} \text{ or } V_{IN} \geq V_{IH}$ I <sub>OUT</sub> =0 mA, f=1/t <sub>RC</sub>	—	—	30	mA
	I <sub>CC2</sub>	$\overline{CE} \leq 0.2 \text{ V}, V_{IN} \leq 0.2 \text{ V or } V_{IN} \geq V_{CC} - 0.2 \text{ V}$ I <sub>OUT</sub> =0 mA, f=1/t <sub>RC</sub>	—	—	25	mA
Current consumption (Program)	I <sub>CC3</sub>	$\overline{CE} \leq V_{IL}, V_{IN} \leq V_{IL} \text{ or } V_{IN} \geq V_{IH}$	—	—	30	mA
	I <sub>CC4</sub>	$\overline{CE} \leq 0.2 \text{ V}, V_{IN} \leq 0.2 \text{ V or } V_{IN} \geq V_{CC} - 0.2 \text{ V}$	—	—	25	mA
Standby current	I <sub>SB1</sub>	$\overline{CE} \geq V_{IH}$	—	—	1	mA
	I <sub>SB2</sub>	$\overline{CE} \geq V_{CC} - 0.2 \text{ V}$	—	—	1.0	μA
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> =GND to V <sub>CC</sub>	—	—	1.0	μA
Output leakage current	I <sub>LO</sub>	V <sub>I/O</sub> =GND to V <sub>CC</sub>	—	—	1.0	μA
High level output voltage	V <sub>OH</sub>	I <sub>OH</sub> =-400 μA	2.4	—	—	V
Low level output voltage	V <sub>OL</sub>	I <sub>OL</sub> =2.1 mA	—	—	0.4	V

■ Rewriting Times

Table 6

Parameter	Symbol	Min.	Typ.	Max.	Unit
Rewriting times	N <sub>W</sub>	10 <sup>5</sup>	—	—	times/byte

■ Pin Capacitance

Table 7

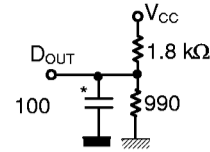
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0 V	—	—	10	pF
Input / output capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> =0 V	—	—	10	pF

**CMOS 16K-bit PARALLEL E<sup>2</sup>PROM  
S-2812A/2817A**

■ **AC Electrical Characteristics**

**Table 8 Measuring conditions**

Parameter	S-2812A	S-2817A
Input pulse levels	V <sub>IL</sub> =0.2 V V <sub>IH</sub> =2.4 V	V <sub>IL</sub> =0.4 V V <sub>IH</sub> =2.4 V
Input rise and fall time	10 ns	10 ns
I/O reference level	1.5 V	1.5 V
Output load	See Figure 3	See Figure 3



\* (When measuring t<sub>CLZ</sub>, t<sub>OLZ</sub>, t<sub>CHZ</sub>, t<sub>OHZ</sub>, t<sub>WHZ</sub>, t<sub>WLZ</sub>) : 5pF

**Figure 3 Output load measuring circuit**

1. Read Cycle

(1) 5-V operation

**Table 9**

(V<sub>CC</sub>=5 V±10%)

Parameter	Symbol	0°C to 70°C		-40°C to 85°C		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	t <sub>RC</sub>	150	—	200	—	ns
CE access time	t <sub>CE</sub>	—	150	—	200	ns
Address access time	t <sub>AA</sub>	—	150	—	200	ns
OE access time	t <sub>OE</sub>	—	70	—	90	ns
Output enable time ( $\overline{\text{CE}}$ )	t <sub>CLZ</sub>	10	—	10	—	ns
Output enable time ( $\overline{\text{OE}}$ )	t <sub>OLZ</sub>	10	—	10	—	ns
Output disable time ( $\overline{\text{CE}}$ )	t <sub>CHZ</sub>	10	70	10	90	ns
Output disable time ( $\overline{\text{OE}}$ )	t <sub>OHZ</sub>	10	70	10	90	ns
Output data hold time	t <sub>OH</sub>	5	—	5	—	ns

(2) 3-V operation (S-2812A only)

**Table 10**

(V<sub>CC</sub>=3 V±10%)

Parameter	Symbol	0°C to 70°C		-40°C to 85°C		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	t <sub>RC</sub>	400	—	500	—	ns
CE access time	t <sub>CE</sub>	—	400	—	500	ns
Address access time	t <sub>AA</sub>	—	400	—	500	ns
OE access time	t <sub>OE</sub>	—	200	—	250	ns
Output enable time ( $\overline{\text{CE}}$ )	t <sub>CLZ</sub>	25	—	30	—	ns
Output enable time ( $\overline{\text{OE}}$ )	t <sub>OLZ</sub>	25	—	30	—	ns
Output disable time ( $\overline{\text{CE}}$ )	t <sub>CHZ</sub>	25	200	30	250	ns
Output disable time ( $\overline{\text{OE}}$ )	t <sub>OHZ</sub>	25	200	30	250	ns
Output data hold time	t <sub>OH</sub>	10	—	15	—	ns

2. Write Cycle

(1) 5-V operation

**Table 11**

(V<sub>CC</sub>=5 V±10%)

Parameter	Symbol	0°C to 70°C		-40°C to 85°C		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	t <sub>WC</sub>	—	10	—	10	ms
Address setup time	t <sub>AS</sub>	0	—	0	—	ns
Address hold time	t <sub>AH</sub>	120	—	150	—	ns
Write setup time	t <sub>CS</sub>	0	—	0	—	ns
Write hold time	t <sub>CH</sub>	0	—	0	—	ns
$\overline{\text{CE}}$ pulse width	t <sub>CW</sub>	120	—	150	—	ns
$\overline{\text{OE}}$ setup time	t <sub>OES</sub>	15	—	20	—	ns
$\overline{\text{OE}}$ hold time	t <sub>OEH</sub>	15	—	20	—	ns
$\overline{\text{WE}}$ pulse width	t <sub>WP</sub>	120	—	150	—	ns
Data setup time	t <sub>DS</sub>	85	—	100	—	ns
Data hold time	t <sub>DH</sub>	0	—	0	—	ns
Page load time (page data setting time)	t <sub>PL</sub>	0.3	30	0.3	30	μs
Page load time (page data write start time)	t <sub>PDL</sub>	100	—	100	—	μs
Time to device busy	t <sub>DB</sub>	110	—	140	—	ns

(2) 3-V operation (S-2812A only)

**Table 12**

(V<sub>CC</sub>=3 V±10%)

Parameter	Symbol	0°C to 70°C		-40°C to 85°C		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	t <sub>WC</sub>	—	10	—	10	ms
Address setup time	t <sub>AS</sub>	0	—	0	—	ns
Address hold time	t <sub>AH</sub>	300	—	350	—	ns
Write setup time	t <sub>CS</sub>	0	—	0	—	ns
Write hold time	t <sub>CH</sub>	0	—	0	—	ns
$\overline{\text{CE}}$ pulse width	t <sub>CW</sub>	300	—	350	—	ns
$\overline{\text{OE}}$ setup time	t <sub>OES</sub>	30	—	35	—	ns
$\overline{\text{OE}}$ hold time	t <sub>OEH</sub>	30	—	35	—	ns
$\overline{\text{WE}}$ pulse width	t <sub>WP</sub>	300	—	350	—	ns
Data setup time	t <sub>DS</sub>	180	—	210	—	ns
Data hold time	t <sub>DH</sub>	0	—	0	—	ns
Page load time (page data setting time)	t <sub>PL</sub>	0.3	30	0.3	30	μs
Page load time (page data write start time)	t <sub>PDL</sub>	100	—	100	—	μs
Time to device busy	t <sub>DB</sub>	250	—	300	—	ns

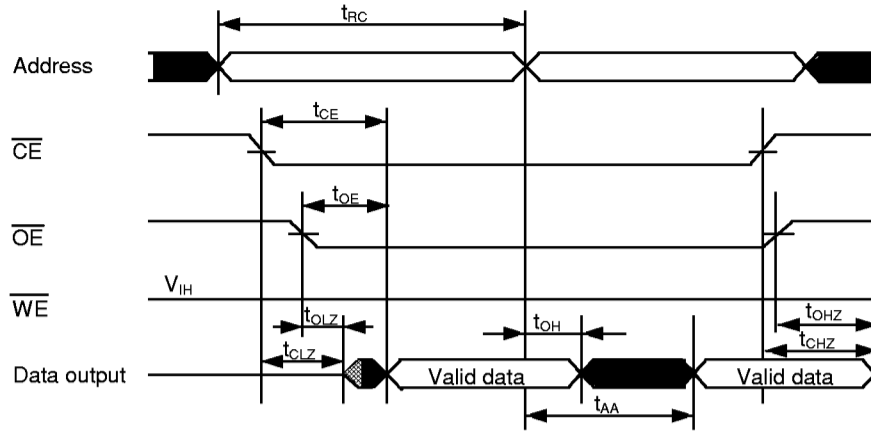


Figure 4 Read cycle

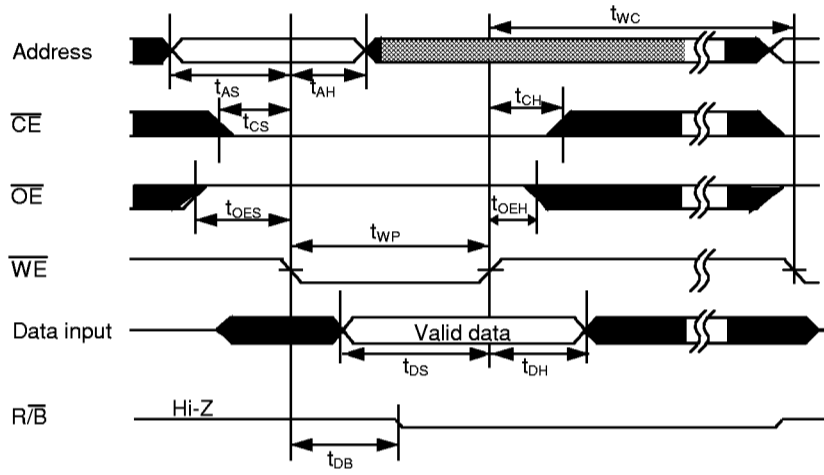


Figure 5  $\overline{WE}$  controlled write cycle

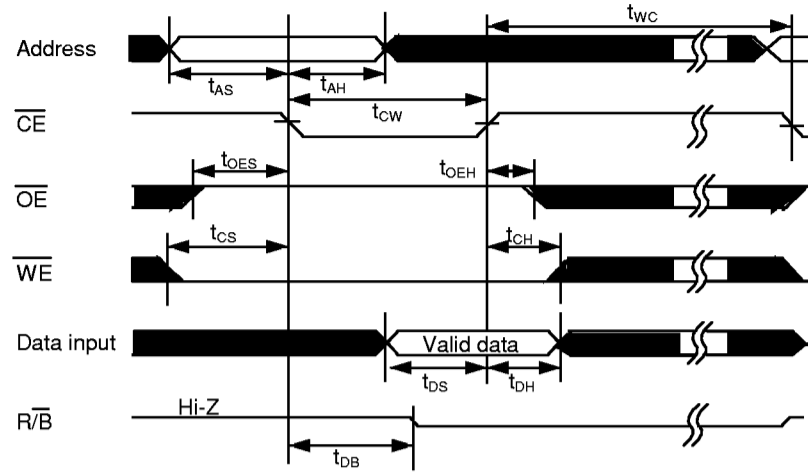


Figure 6  $\overline{CE}$  controlled write cycle

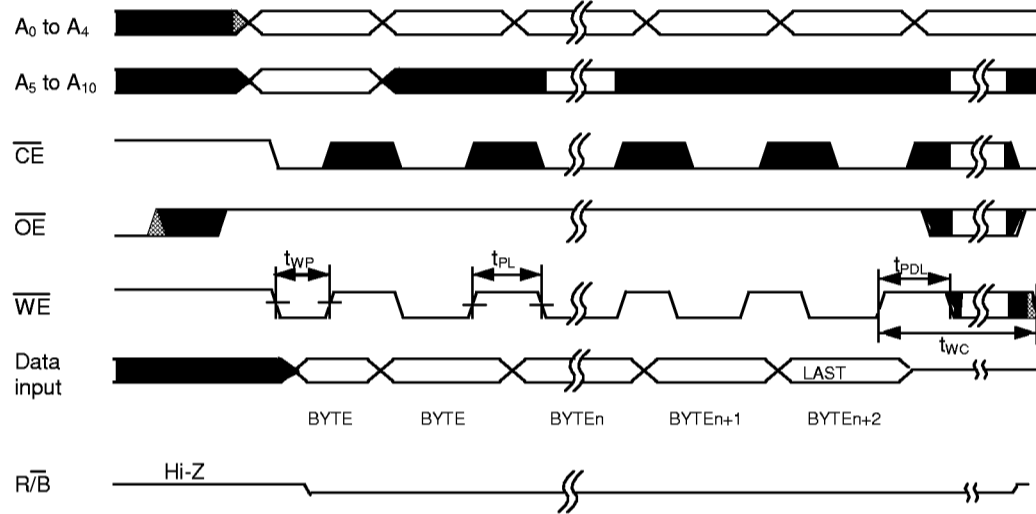


Figure 7 Page write cycle

# CMOS 16K-bit PARALLEL E<sup>2</sup>PROM

## S-2812A/2817A

### ■ Operation

(1) Read mode

This mode outputs data to I/O<sub>0</sub> to I/O<sub>7</sub> when both  $\overline{CE}$  and  $\overline{OE}$  are low and when  $\overline{WE}$  is high. The data bus is high impedance when either  $\overline{CE}$  or  $\overline{OE}$  is high.

(2) Byte write mode

A byte write cycle starts when both  $\overline{CE}$  and  $\overline{WE}$  are low and  $\overline{OE}$  is high.  $\overline{CE}$ - and  $\overline{WE}$ -controlled write cycles are available. The address is latched at the falling of  $\overline{CE}$  or  $\overline{WE}$  whichever occurs last, and the data is latched at the rising of  $\overline{CE}$  or  $\overline{WE}$  whichever occurs first.

(3) Page write mode

In this mode, 1 page program operation of 32 bytes is completed in 10 ms, and all memory area is written within a second because the device organization is 64-page × 32-byte. When starting this mode, first, addresses A<sub>5</sub> to A<sub>10</sub> assign the page, then A<sub>0</sub> to A<sub>4</sub> assign the address to each byte within the page sequentially or at random. Less than 32 bytes of program is available. This address assignment is performed while  $0.3 \mu\text{s} \leq t_{PL} \leq 30 \mu\text{s}$ , and the program operation starts when  $t_{PD1} \geq 100 \mu\text{s}$ .

(4) Data polling

This function is to output the complement data written last on I/O<sub>7</sub> and to output low to I/O<sub>0</sub> to I/O<sub>6</sub>. This operation is performed by read operation during write cycle.  $R/\overline{B}$  outputs low during write cycle; it is in high impedance in other modes.

(5) Erase all mode

All data is erased when  $\overline{OE}$  is 13 V and both  $\overline{CE}$  and  $\overline{WE}$  are low. During erase all mode, A<sub>0</sub> to A<sub>10</sub> and I/O<sub>0</sub> to I/O<sub>7</sub> must be fixed to either high or low.

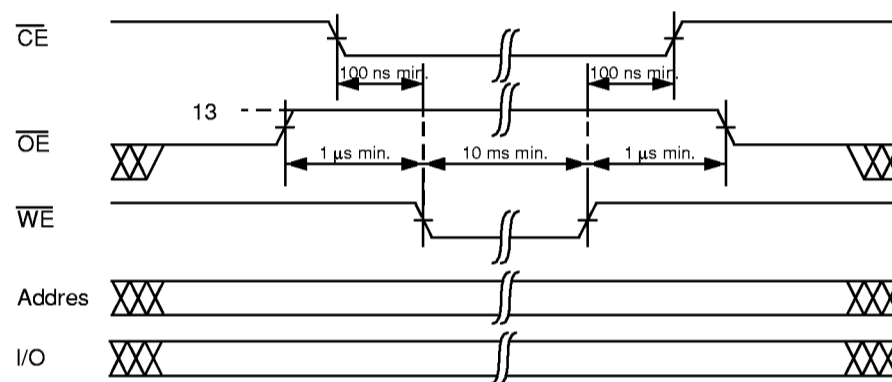


Figure 8

(6) Write inhibition

Write operation is inhibited in the following cases :

- When power supply voltage is under write inhibit voltage ( $V_{WI}$ ).  
S-2817A :  $V_{WI}=3.5 \text{ V typ.}$   
S-2812A :  $V_{WI}=2.1 \text{ V typ.}$
- When  $\overline{OE}$  is low, or  $\overline{WE}$  is high.

(7) Program noise immunity

$\overline{CE}$ ,  $\overline{OE}$  and  $\overline{WE}$  are noise protected for preventing erroneous write operation at power on and off. Less than 20 ns write pulse will not activate a write cycle at 5-V operation, and less than 50 ns at 3-V operation. See Figure 9.

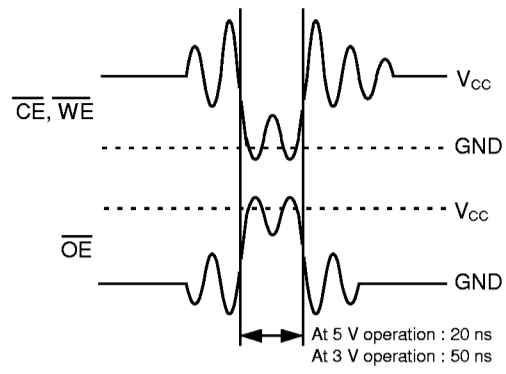


Figure 9

■ Dimensions (Unit : mm)

1. 28-pin DIP

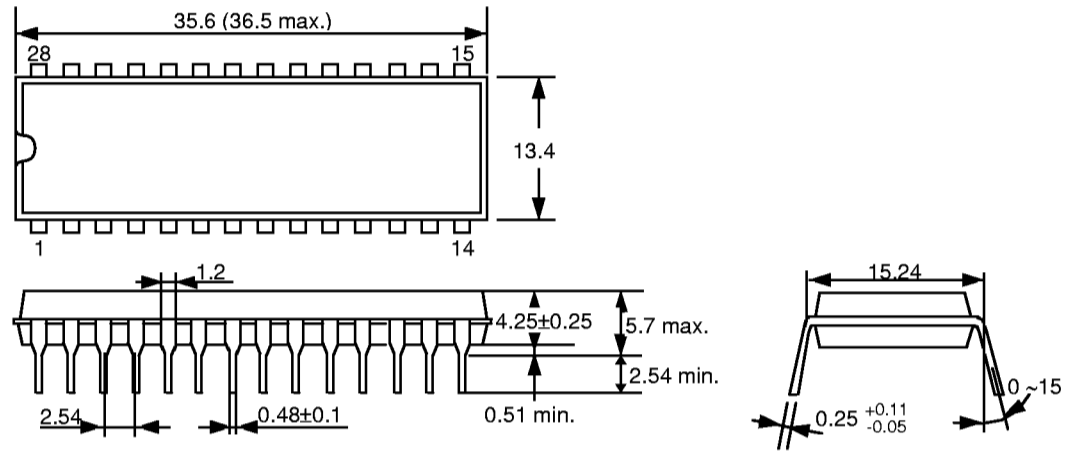


Figure 10

2. 28-pin SOP

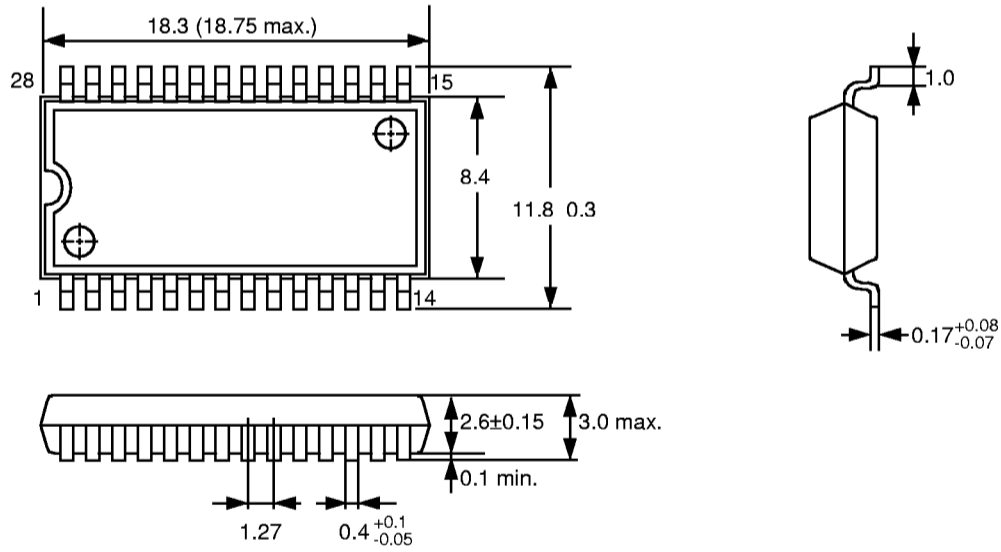


Figure 11

**CMOS 16K-bit PARALLEL E<sup>2</sup>PROM  
S-2812A/2817A**

3. 28-pin TSOP

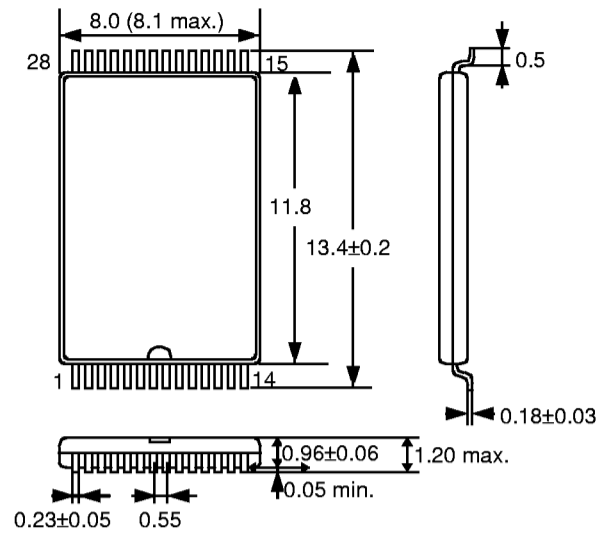
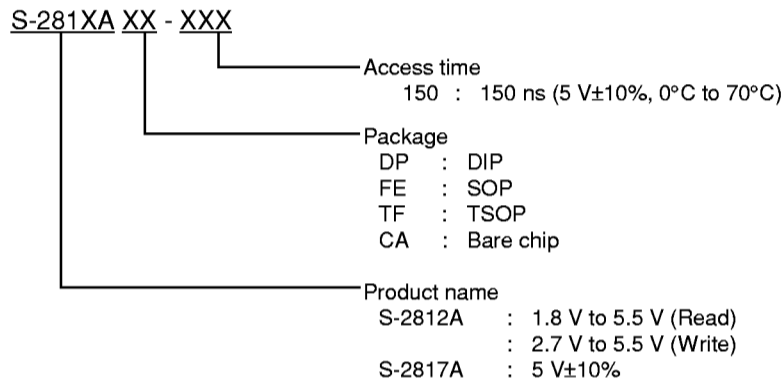


Figure 12

■ Ordering Information

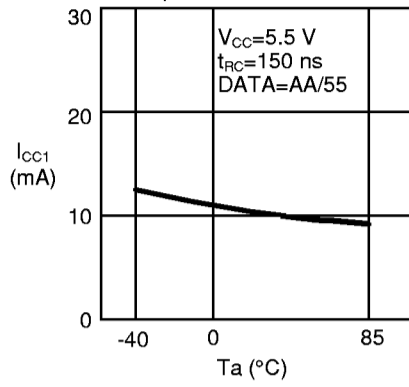


Note: Each bit is set to 1 before delivery (except bare chip)

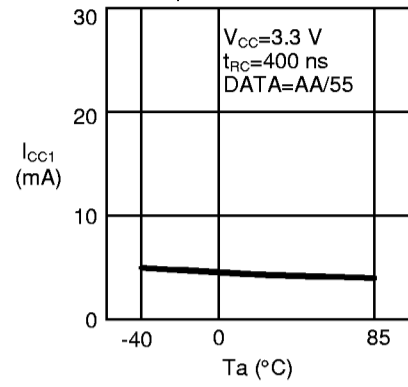
■ Characteristics

1. DC characteristics

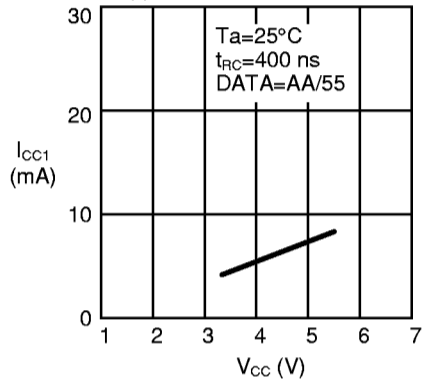
1.1 Current consumption (READ)  $I_{CC1}$  -  
Ambient temperature  $T_a$



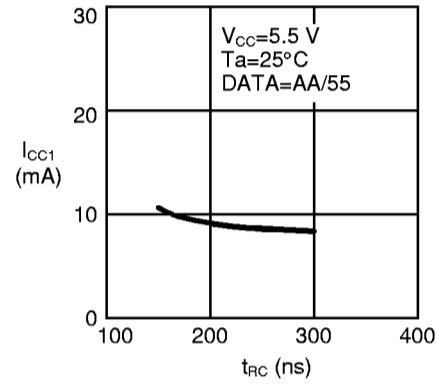
1.2 Current consumption (READ)  $I_{CC1}$  -  
Ambient temperature  $T_a$



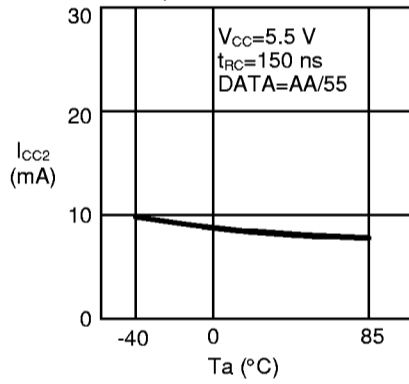
1.3 Current consumption (READ)  $I_{CC1}$  -  
Power supply voltage  $V_{CC}$



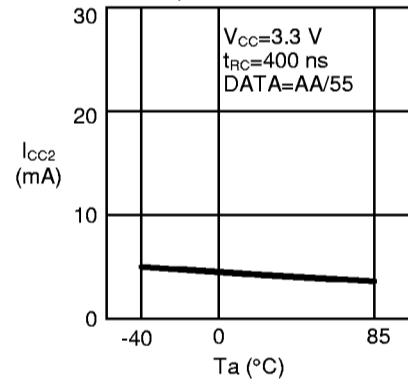
1.4 Current consumption (READ)  $I_{CC1}$  -  
Read cycle time  $t_{RC}$



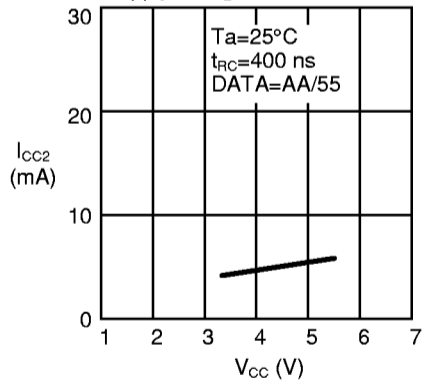
1.5 Current consumption (READ)  $I_{CC2}$  -  
Ambient temperature  $T_a$



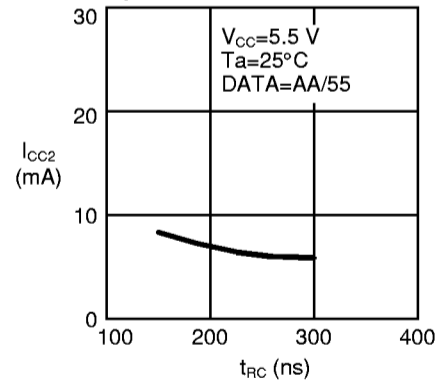
1.6 Current consumption (READ)  $I_{CC2}$  -  
Ambient temperature  $T_a$



1.7 Current consumption (READ)  $I_{CC2}$  -  
Power supply voltage  $V_{CC}$

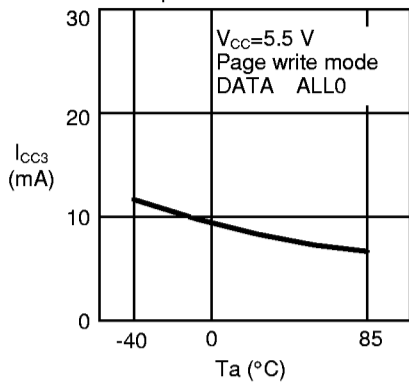


1.8 Current consumption (READ)  $I_{CC2}$  -  
Read cycle time  $t_{RC}$

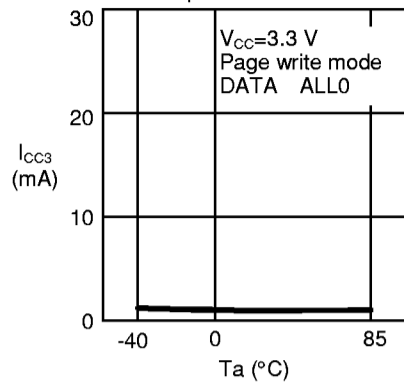


**CMOS 16K-bit PARALLEL E<sup>2</sup>PROM  
S-2812A/2817A**

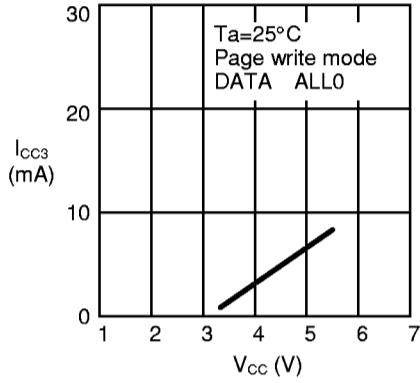
1.9 Current consumption (PROGRAM)  $I_{CC3}$  .  
Ambient temperature  $T_a$



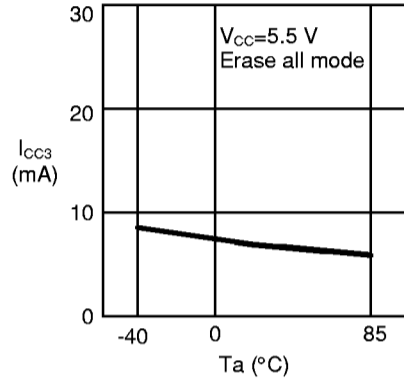
1.10 Current consumption (PROGRAM)  $I_{CC3}$  .  
Ambient temperature  $T_a$



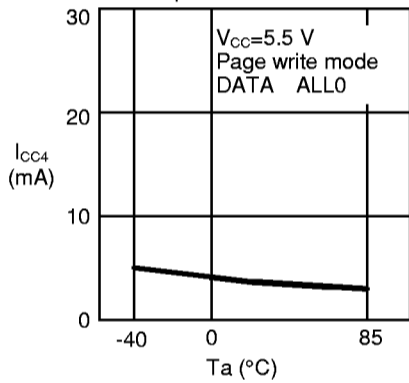
1.11 Current consumption (PROGRAM)  $I_{CC3}$  .  
Power Supply Voltage  $V_{CC}$



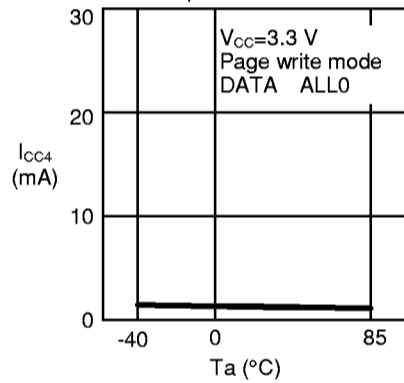
1.12 Current consumption (PROGRAM)  $I_{CC3}$  .  
Ambient temperature  $T_a$



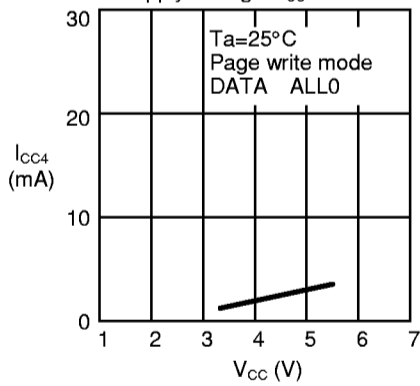
1.13 Current consumption (PROGRAM)  $I_{CC4}$  .  
Ambient temperature  $T_a$



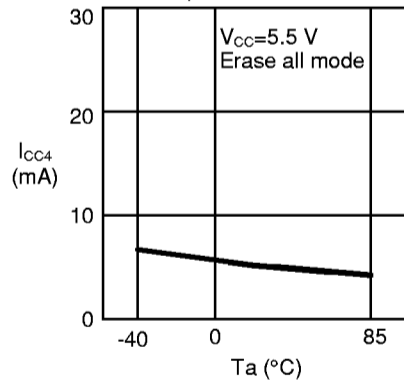
1.14 Current consumption (PROGRAM)  $I_{CC4}$  .  
Ambient temperature  $T_a$



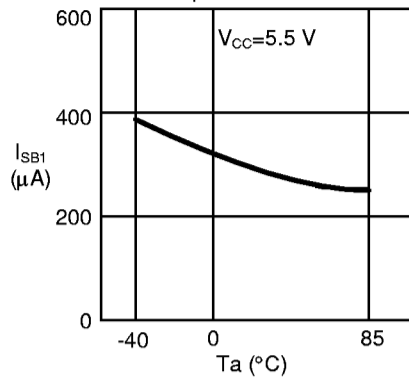
1.15 Current consumption (PROGRAM)  $I_{CC4}$  .  
Power Supply Voltage  $V_{CC}$



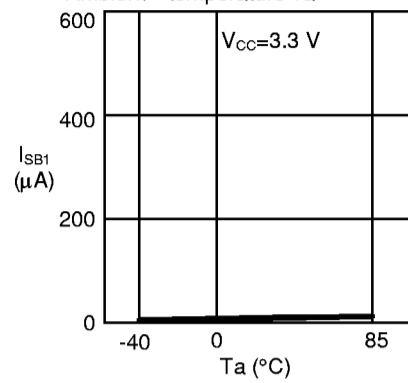
1.16 Current consumption (PROGRAM)  $I_{CC4}$  .  
Ambient temperature  $T_a$



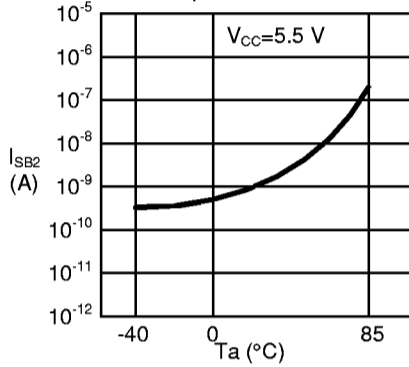
1.17 Standby current  $I_{SB1}$  -  
Ambient temperature  $T_a$



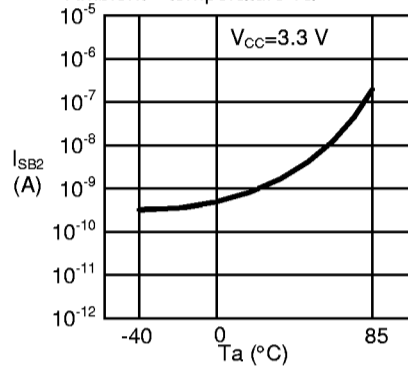
1.18 Standby current  $I_{SB1}$  -  
Ambient temperature  $T_a$



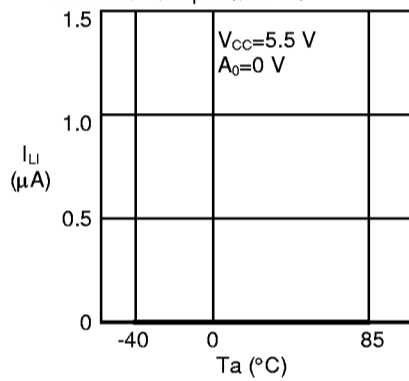
1.19 Standby current  $I_{SB2}$  -  
Ambient temperature  $T_a$



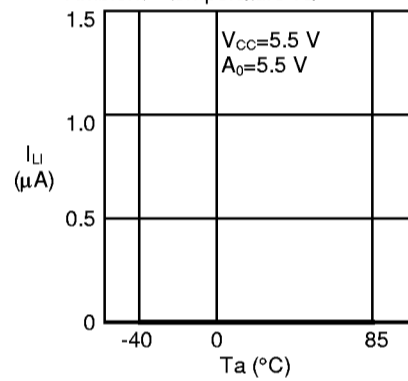
1.20 Standby current  $I_{SB2}$  -  
Ambient temperature  $T_a$



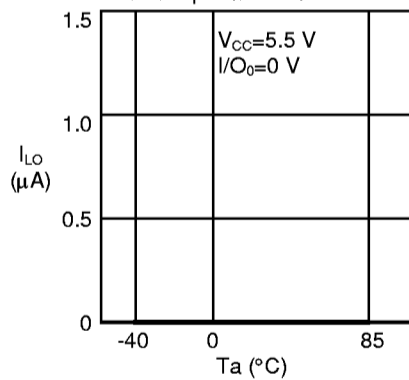
1.21 Input leakage current  $I_{LI}$  -  
Ambient temperature  $T_a$



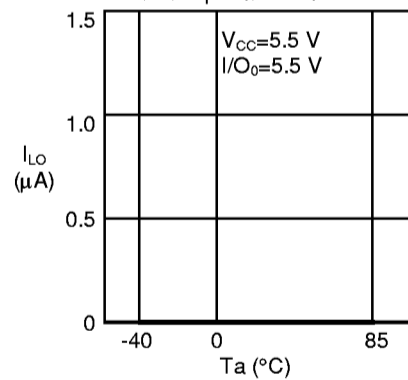
1.22 Input leakage current  $I_{LI}$  -  
Ambient temperature  $T_a$



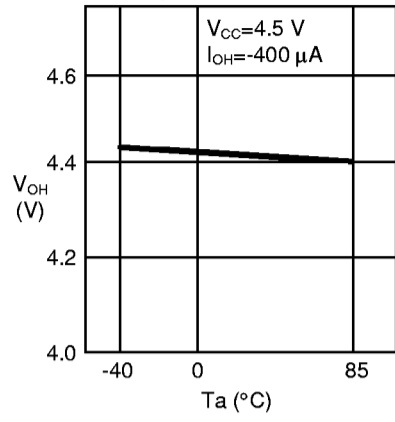
1.23 Output leakage current  $I_{LO}$  -  
Ambient temperature  $T_a$



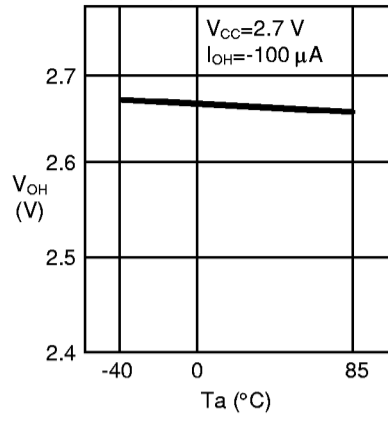
1.24 Output leakage current  $I_{LO}$  -  
Ambient temperature  $T_a$



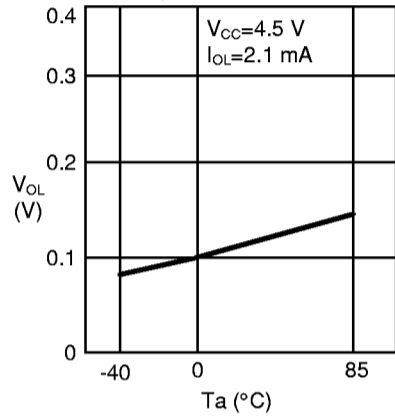
1.25 High level output voltage  $V_{OH}$  - Ambient temperature  $T_a$



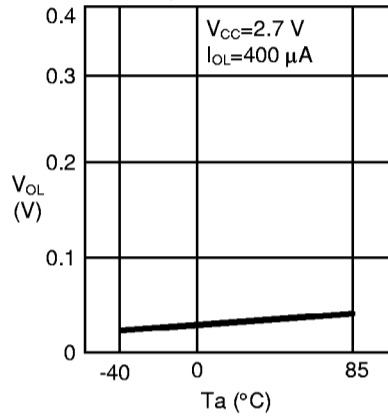
1.26 High level output voltage  $V_{OH}$  - Ambient temperature  $T_a$



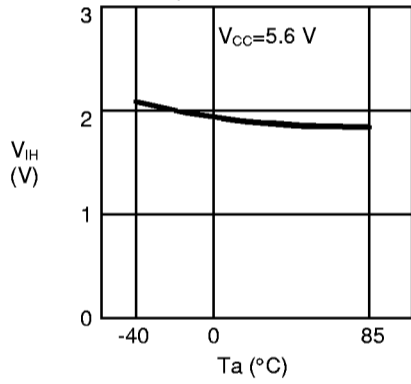
1.27 Low level output voltage  $V_{OL}$  - Ambient temperature  $T_a$



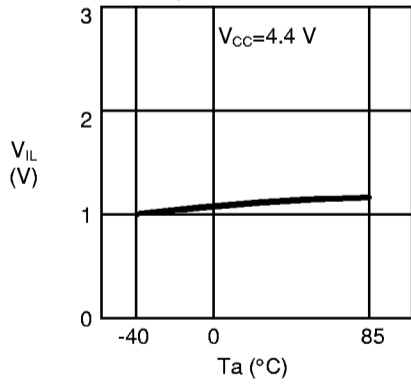
1.28 Low level output voltage  $V_{OL}$  - Ambient temperature  $T_a$



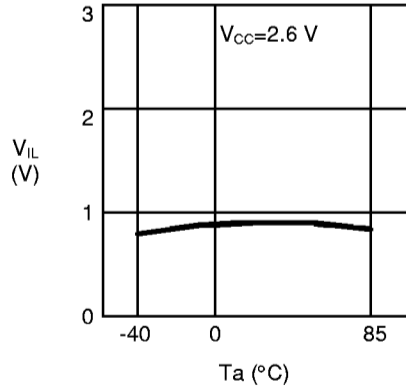
1.29 High level input voltage  $V_{IH}$  - Ambient temperature  $T_a$



1.30 Low level input voltage  $V_{IL}$  - Ambient temperature  $T_a$

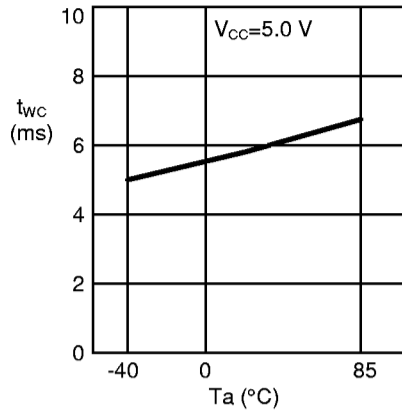


1.31 Low level input voltage  $V_{IL}$  - Ambient temperature  $T_a$

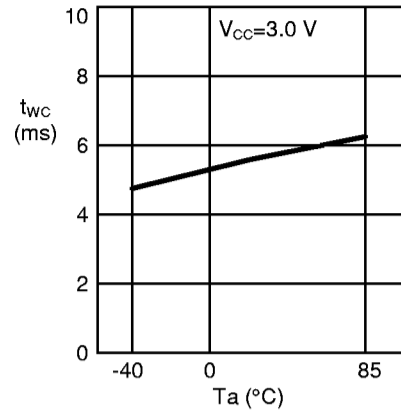


2. AC characteristics

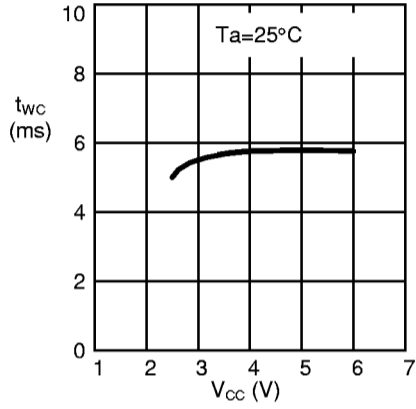
2.1 Write cycle time  $t_{WC}$  . Ambient temperature  $T_a$



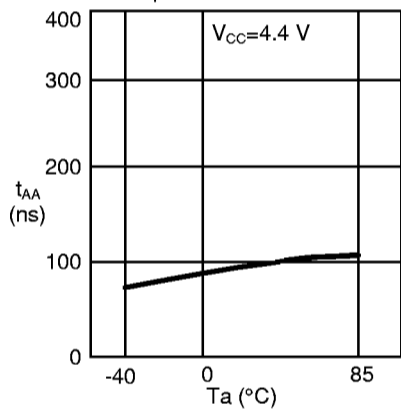
2.2 Write cycle time  $t_{WC}$  . Ambient temperature  $T_a$



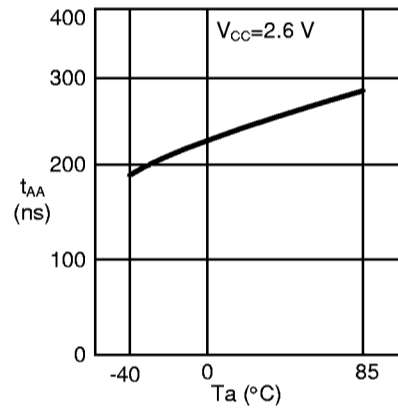
2.3 Write cycle time  $t_{WC}$  . Power supply voltage  $V_{CC}$



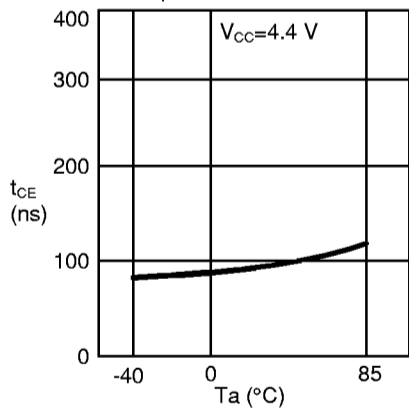
2.4 Address access time  $t_{AA}$  . Ambient temperature  $T_a$



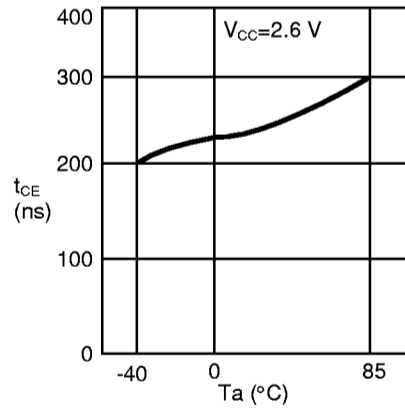
2.5 Address access time  $t_{AA}$  . Ambient temperature  $T_a$



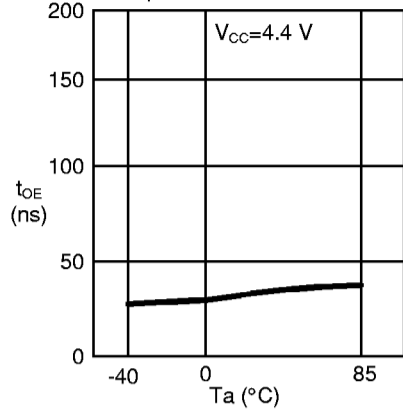
2.6  $\overline{CE}$  access time  $t_{CE}$  . Ambient temperature  $T_a$



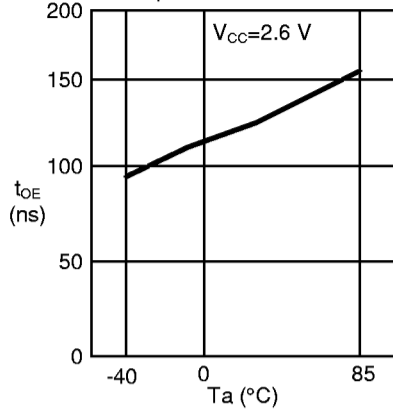
2.7  $\overline{CE}$  access time  $t_{CE}$  . Ambient temperature  $T_a$



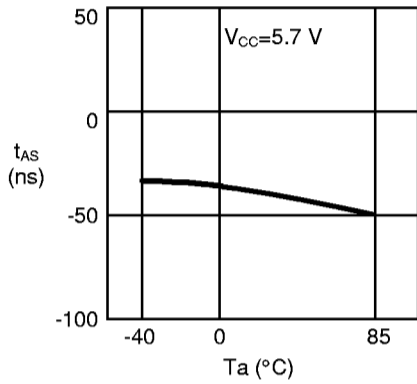
2.8  $\overline{OE}$  access time  $t_{OE}$  -  
Ambient temperature  $T_a$



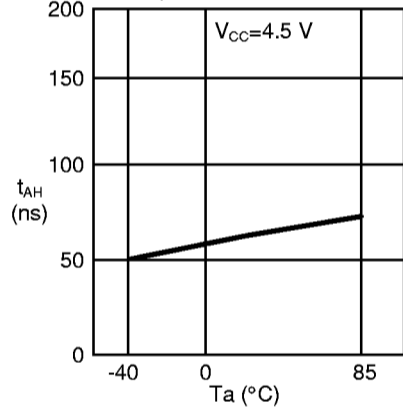
2.9  $\overline{OE}$  access time  $t_{OE}$  -  
Ambient temperature  $T_a$



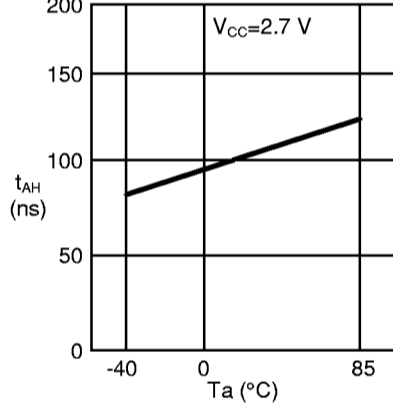
2.10 Address setup time  $t_{AS}$  -  
Ambient temperature  $T_a$



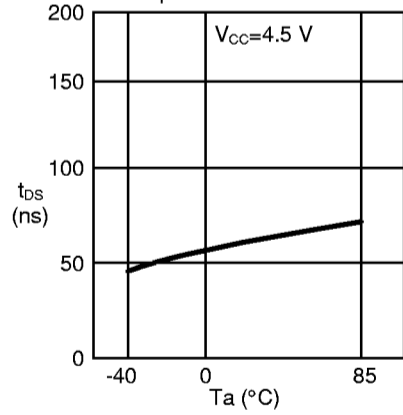
2.11 Address hold time  $t_{AH}$  -  
Ambient temperature  $T_a$



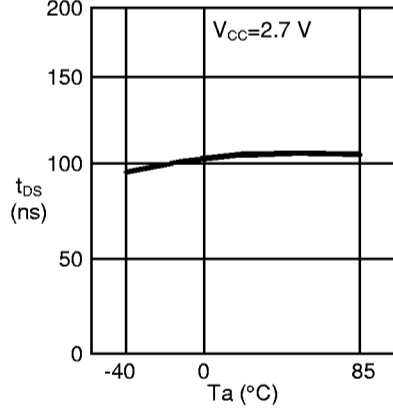
2.12 Address hold time  $t_{AH}$  -  
Ambient temperature  $T_a$



2.13 Data setup time  $t_{DS}$  -  
Ambient temperature  $T_a$



2.14 Data setup time  $t_{DS}$  -  
Ambient temperature  $T_a$



2.15 Data hold time  $t_{DH}$  -  
Ambient temperature  $T_a$

