Hex Buffer with Enable

ELECTRICALLY TESTED PER:
5962-8750901

The 10H588 is a Hex Buffer with a common Enable input. When Enable is in the high state, all outputs are in the low-state. When Enable is in the low-state, the outputs take the same state as the inputs.

This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay and no increase in power-supply current.

- Propagation Delay, 1.3 ns Typical
- 250 mW Max/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
A_{OUT}	2	6	3	51 Ω to V_{TT}
B_{OUT}	3	7	4	51 Ω to V_{TT}
C_{OUT}	4	8	5	51 Ω to V_{TT}
A_{IN}	5	9	7	GND
B_{IN}	6	10	8	GND
C_{IN}	7	11	9	GND
V_{EE}	8	12	10	V_{EE}
Common	9	13	12	OPEN
D_{IN}	10	14	13	GND
E_{IN}	11	15	14	GND
F_{IN}	12	16	15	GND
D_{OUT}	13	1	17	51 Ω to V_{TT}
E_{OUT}	14	2	18	51 Ω to V_{TT}
F_{OUT}	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

TRUTH TABLE		
Inputs		Output
X	Y	OUT
L	L	L
L	H	H
H	L	L
H	H	L

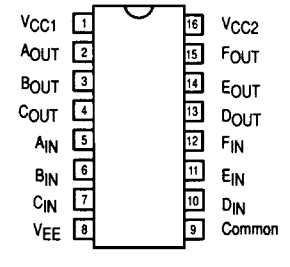
Military 10H588

AVAILABLE AS

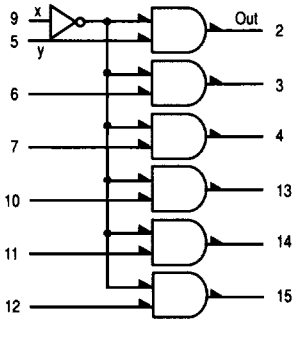
1) JAN: N/A
2) SMD: 5962-8750901
3) 883: 10H588/BXAJC
X = CASE OUTLINE AS FOLLOWS:

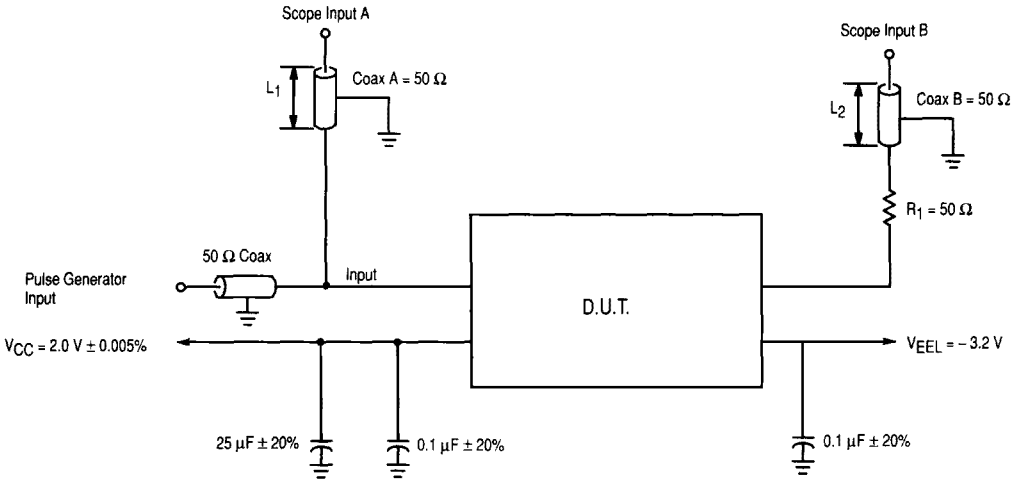
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



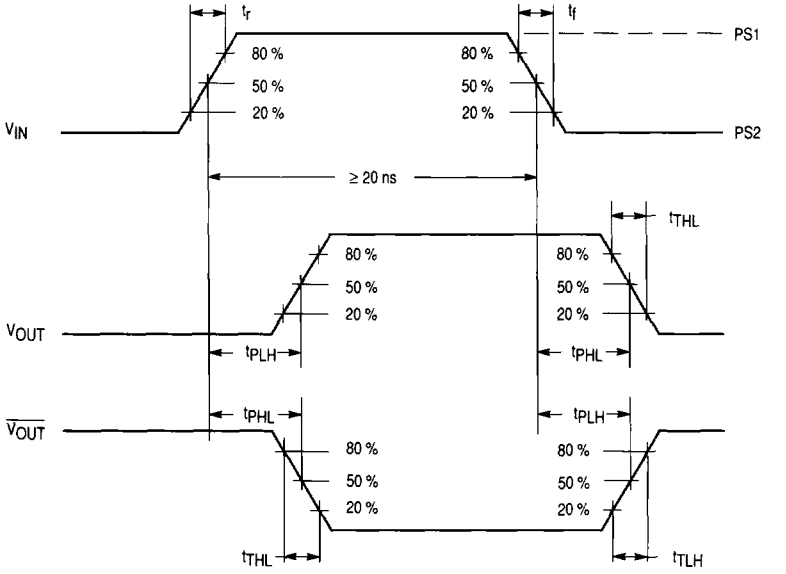
LOGIC DIAGRAM





NOTES

1. Pulse generator must be capable of rise and fall time of 1.0 ns ± 0.1 ms
2. Unused outputs connected to 100 Ω resistor to ground
3. 2:1 divider may be used
4. L1 = L2: matched for equal time delay



NOTES

1. R_1 = 50 Ω in series with a 50 Ω coax constituting the 100 Ω load.
2. $t_r = t_f$ = 1.0 ns ± 0.1 ns.
3. PW ≥ 20 ns
4. f = 1.0 MHz.

Figure 1. Switching Test Circuit and Waveforms

10H588
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}
T_A = 25 °C	-0.78	-1.95	-1.10	-1.480	+1.11	+0.31	-5.46	-4.94
T_A = 125°C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to – 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE}	V_{EE2}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	– 1.01	– 0.78	– 0.86	– 0.65	– 1.06	– 0.84	V	5 - 7 10 - 12		5 - 7 10 - 12	9	8		1, 16	2 - 4, 13 - 15
V_{OL}	Low Output Voltage	– 1.95	– 1.58	– 1.95	– 1.565	– 1.95	– 1.61	V				9	8		1, 16	2 - 4, 13 - 15
V_{OH1}	High Output Voltage	– 1.01	– 0.78	– 0.86	– 0.65	– 1.06	– 0.84	V	5 - 7 10 - 12			5 - 7 9 - 12	8	8	1, 16	2 - 4, 13 - 15
V_{OL1}	Low Output Voltage	– 1.95	– 1.58	– 1.95	– 1.565	– 1.95	– 1.61	V	5 - 7 10 - 12		9	5 - 7 10 - 12	8	8	1, 16	2 - 4, 13 - 15
I_{EE}	Power Supply Current	– 42		– 46		– 46		mA					8		1, 16	8
I_{IH}	Input Current High		310		495		495	μA	5 - 7 9 - 12				8		1, 16	5 - 7, 9 - 12
I_{IL}	Input Current	0.5		0.3		0.5		μA		5 - 7 9 - 12				8	1, 16	5 - 7, 9 - 12

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		Subgroup 1		Subgroup 2		Subgroup 3							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P. U. T.
t_{TLH}	Rise Time	0.7	2.2	0.7	2.4	0.7	2.2	ns	5 - 7, 9 - 12	2 - 4, 13 - 15	1, 16	8	2 - 4, 13 - 15
t_{THL}	Fall Time	0.7	2.2	0.7	2.4	0.7	2.2	ns	5 - 7, 9 - 12	2 - 4, 13 - 15	1, 16	8	2 - 4, 13 - 15
t_{PHL} t_{PLH}	Propagation Delay Data	0.7	1.7	0.7	1.9	0.7	1.7	ns	5 - 7, 9 - 12	2 - 4, 13 - 15	1, 16	8	2 - 4, 13 - 15
t_{PLH} t_{PHL}	Propagation Delay Enable	0.7	2.6	0.7	2.8	0.7	2.5	ns	5 - 7, 9 - 12	2 - 4, 13 - 15	1, 16	8	2 - 4, 13 - 15