National Semiconductor

CGS2536V
Commercial Quad 1 to 4 Clock Drivers
CGS2536TV
Industrial Quad 1 to 4 Clock Drivers

General Description

These Clock Generation and Support clock drivers are specifically designed for driving memory arrays requiring large fanouts while operating at high speeds.

This device meets the rise and fall time requirements of the 90 MHz and 100 MHz Pentium™ procrssors.

The CGS2536 I/O structures are CMOS. The outputs are separated into two banks of eight. One bank consists of divide by two outputs, the other, straight-through buffers. Within each bank, half the outputs are inverting, the other half non-inverting.

The CGS2536 specification guarantees part-to-part skew variation.

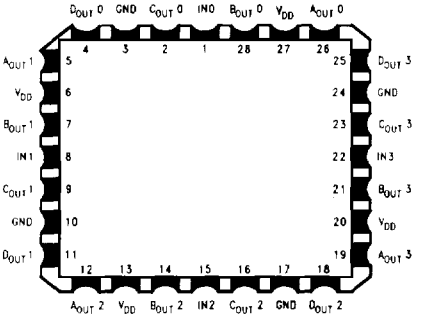
Features

- Guaranteed:
  - 1.0 ns rise and fall times while driving 12 inches of 50Ω microstrip terminated with 25 pF
  - 350 ps pin-to-pin skew (t_{OSLH} and t_{OSHL})
- 650 ps part-to-part variation on positive or negative transition
- Operates with either 3.3V or 5.0V supply
- Inputs 5V tolerant with V_{CC} in 3.3V range
- Symmetric output current drive: 24 mA I_{OH}/I_{OL}
- Industrial temperature of −40°C to +85°C
- Symmetric package orientation
- Large fanout for memory driving applications
- Guaranteed 2 kV ESD protection
- Implemented on National's ABT family process
- 28-pin PLCC for optimum skew performance

Ordering Code: See Section 10

Connection Diagrams

Pin Assignment for 28-Pin PLCC



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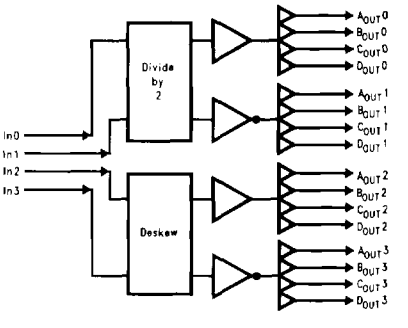
Truth Table

Input	Output
In 0	ABCD Out (0) ÷ 2
In 1	$\overline{ABCD}$ Out (1) ÷ 2
In 2	ABCD Out (2)
In 3	$\overline{ABCD}$ Out (3)

CGS2536



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Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	7.0V
Input Voltage (V_I)	7.0V
Input Current	−30 mA
Current Applied to Output (High/Low)	Twice the Rated IOH/IOL
Operating Temperature	
Industrial Grade	−40°C to +85°C
Commercial grade	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Airflow	Typical θ_{JA}
0 LFM	62°C/W
225 LFM	43°C/W
500 LFM	34°C/W
900 LFM	27°C/W

Recommended Operating Conditions

Supply Voltage	V_{CC} 4.5V to 5.5V
	V_{CC} 3.0V to 3.6V
Maximum Input Rise/Fall Time (0.8V to 2.0V)	5 ns
Free Air Operating Temperature	
Commercial	0°C to +70°C
Industrial	−40°C to +85°C

Note: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the DC and AC Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The Recommended Operating Conditions will define the conditions for actual device operation.

DC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Typ	Max	Units
V_{IH}	Input High Level Voltage		3.0	2.1			V
			4.5	3.15			
			5.5	3.85			
V_{IL}	Input Low Level Voltage		3.0			0.9	V
			4.5			1.35	
			5.5			1.65	
V_{IK}	Input Clamp Voltage	I_I = −18 mA	4.5			−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −50 μA	3.0	2.9			V
			4.5	4.4			
			5.5	5.4			
		I_{OH} = −24 mA	3.0	2.46			V
			4.5	3.76			
			5.5	4.76			
V_{OL}	Low Level Output Voltage	I_{OL} = 50 μA	3.0			0.1	V
			4.5			0.1	
			5.5			0.1	
		I_{OL} = 24 mA	3.0			0.44	V
			4.5			0.44	
			5.5			0.44	
I_I	Input Current @ Max Input Voltage	V_{IH} = 7V	5.5			7	μA
		V_{IH} = V_{CC}	3.6			1	
I_{IH}	High Level Input Current	V_{IH} = V_{CC}	5.5			5	μA
I_{IL}	Low Level Input Current	V_{IL} = 0V	5.5	−5			μA
I_{OLD}	Minimum Dynamic Output Current*	V_{OLD} = 1.65V (max)	5.5	75			mA
		V_{OLD} = 0.9V (max)	3.0**	36			
I_{OHD}	Minimum Dynamic Output Current*	V_{OHD} = 3.85V (min)	5.5	−75			mA
		V_{OHD} = 2.1V (min)	3.0**	−25			
I_{CC}	Supply Current		3.6			75	μA
			5.5			235	
C_{IN}	Input Capacitance		5.0		5		pF

*Maximum test duration 2.0 ms, one output loaded at a time.

**At V_{CC} = 3.3V, I_{OLD} = 55 mA min; @ V_{CC} = 3.6V, I_{OLD} = 64 mA min
At V_{CC} = 3.3V, I_{OHD} = −58 mA min; @ V_{CC} = 3.6V, I_{OHD} = −66 mA min

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AC Electrical Characteristics (Notes 1, 2, and 3)

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	V_{CC} (V) (Note 8)	CGS2536						Units
			T_A = +25°C, C_L = 50 pF, R_L = 500Ω			T_A = −40°C to +85°C (Note 4), C_L = 50 pF, R_L = 500Ω			
			Min	Typ	Max	Min	Typ	Max	
f_{max}	Frequency Maximum	3.0					100		MHz
		5.0					125		
t_{PLH}	Low-to-High Propagation Delay CK to O_n	3.3			7.25			7.25	ns
		5.0			5.0			5.0	
t_{PHL}	High-to-Low Propagation Delay CK to O_n	3.3			5.5			5.5	ns
		5.0			4.5			4.5	
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation (Notes 1, 3)	3.3		150	350		300	350	ps
		5.0		150	350		300	350	
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation (Notes 1, 3)	3.3		150	350		300	350	ps
		5.0		150	350		300	350	
t_{rise}, t_{fall}	Rise/Fall Time (from 0.8V/2.0V to 2.0V/0.8V) (Note 5)	3.3			4.5			4.5	ns
		5.0			3.5			3.5	
t_{rise}, t_{fall}	Rise/Fall Time (from 0.8V/2.0V to 2.0V/0.8V) (Note 6)	3.3			0.8			1.0	ns
		5.0			0.4			0.6	
t_{rise}, t_{fall}	Rise/Fall Time (from 0.8V/2.0V to 2.0V/0.8V) (Note 7)	3.3			1.0			1.0	ns
		5.0			0.7			0.9	
t_{High}	Pulse Width Duration High (Notes 2, 3)	3.3	4.0			4.0			ns
		5.0	4.0			4.0			
t_{Low}	Pulse Width Duration Low (Notes 2, 3)	3.3	4.0			4.0			
		5.0	4.0			4.0			
t_{PVLH}	Part-to-Part Variation of Low-to-High Transitions	3.3			650			650	ps
		5.0			650			650	
t_{PVHL}	Part-to-Part Variation of High-to-Low Transitions	3.3			650			650	
		5.0			650			650	

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either LOW to HIGH (t_{OSLH}) or HIGH to LOW (t_{OSHL}).

Note 2: Time high is measured with outputs at 2.0V or above. Time low is measured with outputs at 0.8V or below. Input waveform characteristics for t_{High}, t_{Low} measurement: f = 66.67 MHz, duty cycle = 50%.

Note 3: The input waveform has a rise and fall time transition time of 2.5 ns (10% to 90%).

Note 4: Industrial range (−40°C to +85°C) limits apply to the commercial temperature range (0°C to +70°C).

Note 5: These Rise and Fall times are measured with C_L = 50 pF, R_L = 500Ω (see *Figure 3*).

Note 6: These Rise and Fall times are measured with C_L = 25 pF, R_L = 500Ω (see *Figure 3*), and are guaranteed by design.

Note 7: These Rise and Fall times are measured driving 12 inches of 50Ω microstrip terminated with equivalent C_L = 25 pF (see *Figure 4*), and are guaranteed by design.

Note 8: Voltage Range 5.0 is 5.0V ± 0.5V, 3.3 is 3.3V ± 0.3V.

Note 9: For increased output drive, output pins may be connected together when the corresponding input pins are connected together.

Timing Information

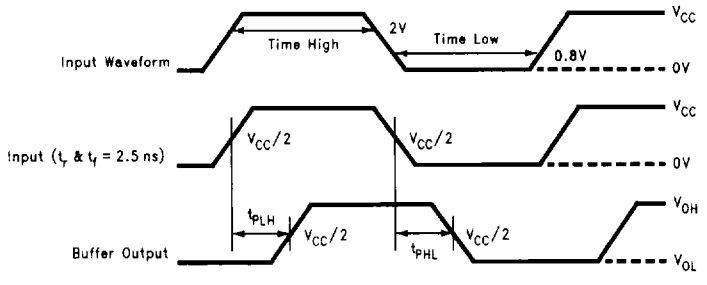

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FIGURE 1. Buffer Waveforms

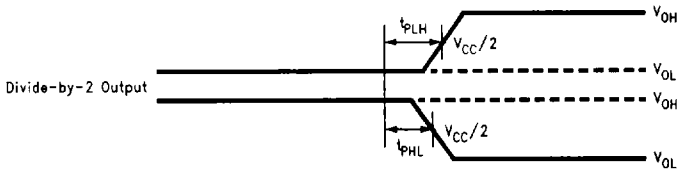

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FIGURE 2. Divide by 2 Waveforms

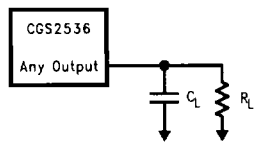

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FIGURE 3. A.C. Load (Reference Notes 5, 6)
C_L = Total Load Including Probes

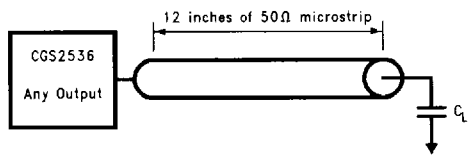

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FIGURE 4. A.C. Load (Reference Note 7)
C_L = Total Load Including Probes

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Power On Requirements

DETAILED DESCRIPTION

The divide by two block of the CGS2536 is accomplished using two negative-edge-triggered flip-flops. During power-on, the inverting flip-flop causes outputs Aout1 through Dout1 to be High. The non-inverting flip-flop causes outputs Aout0 through Dout0 to be Low. Two flip-flops are used to achieve minimum skew between the non-inverting and inverting outputs.

To guarantee that the flip-flops power-up out of phase, the IN0 and IN1 pins must be held low while power is applied to V_{CC}. IN0 and IN1 must remain low until $V_{CC} \geq 3V$.

Application Hints

In a typical user environment IN0 and IN1 inputs may be connected common. Power is applied simultaneously to the crystal oscillator and the CGS2536. If the oscillator output does not deliver a clean first negative-going-edge to the IN0 and IN1 inputs, only one flip-flop may toggle.

Even if the user delays application of V_{CC} to the CGS2536, a false trigger may occur. Simply gating the oscillator to the IN0 and IN1 inputs will not guarantee correct operation, since a "runt" pulse may propagate through the gate and toggle only one of the flip-flops.

Figure 1 shows a circuit that delivers "runt-free" negative-going-edges to the IN0 and IN1 inputs. This circuit ensures that the first clocking pulse seen by the IN0 and IN1 inputs consists of a full positive half-cycle of the crystal oscillator. *Figure 2* shows the waveforms from the synchronizing circuit.

The propagation delay of the 74AC00 gates and the toggle frequency of the 74VHC164 limit the maximum frequency of operation. Equivalent logic elements that have faster propagation delays can be substituted for the NAND gates and shift register. For example, a generic GAL22V10-5 could be programmed as the NAND gates that drive the CGS2536.

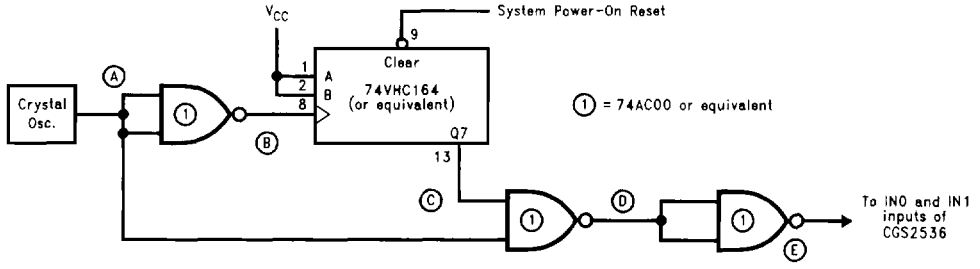
***Figure 1* CIRCUIT DESCRIPTION**

Assumptions:

1. V_{CC} is applied simultaneously to the crystal oscillator, CGS2536, 74AC00, and 74VHC164.
2. A system power-on reset is "Low" long enough for V_{CC} and the crystal oscillator to stabilize.

At power-on, assertion (low) of the system power-on reset clears the outputs of the 74VHC164 serial to parallel converter.

As a result, nodes C and E are low ensuring power-on requirements for the CGS2536 are met. When the system power-on reset is de-asserted, the eighth positive-going-edge received by the 74VHC164 causes node C to go high. Node C remains high as long as power is applied. However, node D still remains high due to the oscillator output (A) being low. Node E stays low until the next positive-going-edge of the oscillator. Thus, a full positive half-cycle of the oscillator is seen by the IN1 and IN0 inputs, which ensures that both flip-flops of the divide by two toggle.



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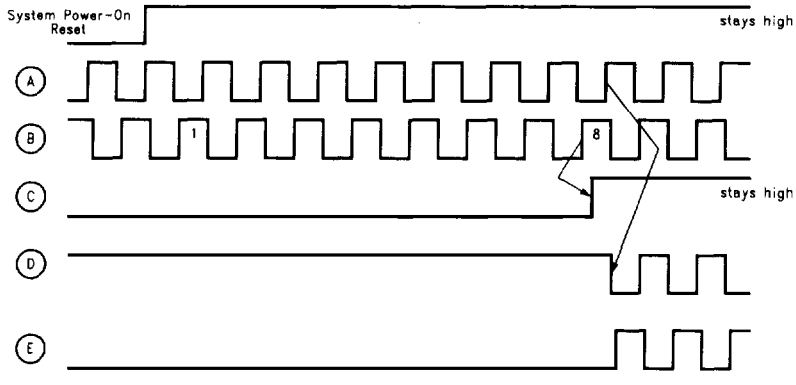

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Memory Array Driving

In order to minimize the total load on the address bus, quite often memory arrays are driven by buffers while having the inputs of the buffers tied together. Although this practice was feasible in the conventional memory designs, in today's high speed, large buswidth designs which require address fetching at higher speeds, this technique produces many undesired results such as cross-talk and over/undershoot.

CGS2534/35/36/37 Quad 1 to 4 clock drivers were designed specifically to address these application issues on high speed, large memory arrays systems.

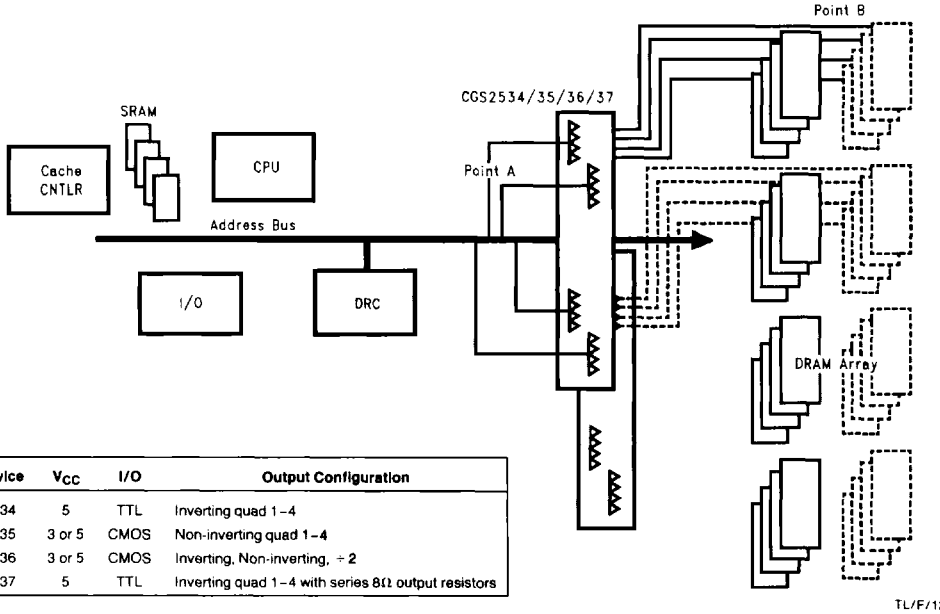
These drivers are optimized to drive large loads, with 3.5 ns propagation delays. These drivers produce less noise while reducing the total capacitive loading on the address bus by having only four inputs tied together (see the diagram below, point A). This helps to minimize the overshoot and undershoot by having only four outputs being switched simultaneously.

Also this larger fan-out helps to save board space since for every one of these drivers, two conventional buffers were typically being used.

Another feature associated with these clock drivers is a 350 ps pin-to-pin skew specification. The minimum skew specification allows high speed memory system designers to optimize the performance of their memory sub-system by operating at higher frequencies without having concerns about output-to-output (bank-to-bank) synchronization problem which are associated with driving high capacitive loads (Point B).

The diagram below depicts a "2534/35/36/37" a memory subsystem operating at high speed with large memory capacity. The address bus is common to both the memory and the CPU and I/Os.

These drivers can operate beyond 125 MHz, and are also available in 3V–5V TTL/CMOS versions with large current drive .



Device	V_{CC}	I/O	Output Configuration
2534	5	TTL	Inverting quad 1–4
2535	3 or 5	CMOS	Non-inverting quad 1–4
2536	3 or 5	CMOS	Inverting, Non-inverting, ÷2
2537	5	TTL	Inverting quad 1–4 with series 8Ω output resistors

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