DS3164-1.0

8.5 MBIT PCM SIGNALLING CIRCUIT

MV1448

HDB3 ENCODER/DECODER

This 8.544MBit PCM Signalling Circuit will perform the signalling and error detection functions for a 8.544MBit PCM transmission link operating to the appropriate CCITT recommendations. The circuit is fabricated in CMOS and operates from a single 5V supply with TTL compatible inputs and outputs.

The MV1448 is an encoder/deocder for the pseudo-ternary transmission code, HDB3 (CCITT Orange Book Vol. III.2 Annex to Rec. G703). The device encodes and decodes simultaneously and asynchronously. Error monitoring functions are provided to detect violations of HDB3 coding, all ones detection and loss of input (all zeros detection). In addition a loop back function is provided for terminal testing.

FEATURES

- HDB3 Encoding and Decoding to CCITT rec. G703
- Asynchronous Operation
- Simultaneous Encoding and Decoding
- Clock Recovery Signal Allows Clock Regeneration from Incoming HDB3 Data
- Loop Back Control
- HDB3 Error Monitor
- 'All Ones' Error Monitor
- Loss of Input Alarm (All Zeros Detector)
- Decoded Data in NRZ Form
- Low Power Operation
- 2.048MHz or 8.544MHz Operation

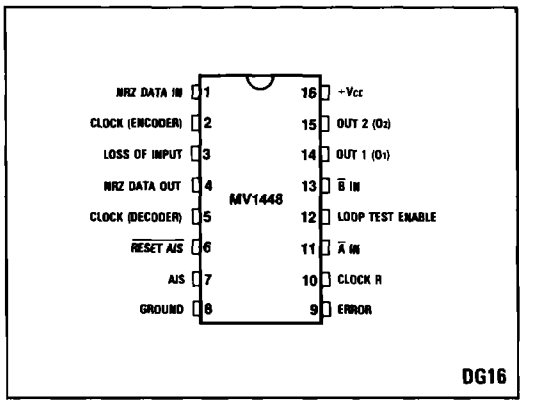

Fig.1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

Electrical Ratings

+Vcc	-0.5V to +7V
Inputs	Vcc+0.5V to GND -0.3V
Outputs	Vcc to GND -0.3V

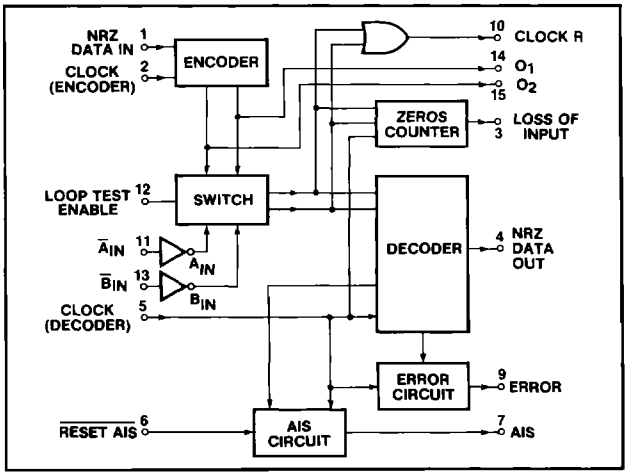

Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage V_{CC} = 5V ± 0.5V Ambient temperature T_{amb} = 0°C to +70°C

Static characteristics

Characteristic	Symbol	Pins	Value			Units	Conditions
			Min.	Typ.	Max.		
Low level input voltage	V_{IL}	All inputs	-0.3		0.8	V	
Low level input current	I_{IL}				50	μA	V_{IL} = 0V
High level input voltage	V_{IH}		2.0		V_{CC}	V	
High level input current	I_{IH}				50	μA	V_{IH} = 5V
Low level output voltage	V_{OL}	All outputs			0.4	V	Isink = 2.0mA
High level output voltage	V_{OH}		2.8			V	Isource = 2mA } both
			V_{CC}-0.75			V	Isource = 1mA } apply
Supply current	I_{CC}			2	4	mA	All inputs to 0V All outputs open circuit

Dynamic characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Max. clock (encoder) frequency	$Fmax_{enc}$	10			MHz	Figs. 10, 15
Max. clock (decoder) frequency	$Fmax_{dec}$	10			MHz	Figs. 11, 15
Propagation delay clock encoder to O_1, O_2	tpd1A/B		50		ns	Figs. 8, 10, 15 See Note 1
Rise and fall times O_1, O_2				20	ns	Figs. 10, 15
tpd1A - tpd1B difference				20	ns	Figs. 10, 15
Propagation delay clock to clock regenerate (clock R)	tpd3		50		ns	Loop test enable = '1', Figs. 10, 15
Setup time of NRZ data in to clock (encoder)	ts3		40		ns	Figs. 7, 10, 15
Hold time of NRZ data in	th3		40		ns	Figs. 7, 10, 15
Propagation delay A_{IN}, B_{IN} to clock regenerate	tpd2 low-high			76	ns	Loop test enable = '0',
	high-low			50		Figs. 13, 15
Propagation delay clock (decoder) to error	tpd4			50	ns	Figs. 12, 15
Propagation delay $\overline{\text{Reset AIS}}$ falling edge to AIS output	tpd5		50	44	ns	Loop test enable = '0', Figs. 14, 15
Propagation delay clock (decoder) to NRZ data out	tpd6			50	ns	Figs. 7, 11, 15 See Note 2
Setup time of $\overline{A}_{IN}$, $\overline{B}_{IN}$ to clock (decoder)	ts1	15	40		ns	Figs. 7, 11, 15
Hold time of $\overline{A}_{IN}$, $\overline{B}_{IN}$ to clock (decoder)	th1	4	5		ns	Figs. 7, 11, 15
Hold time of $\overline{\text{Reset AIS}}$ = '0'	th2	9			ns	Figs. 7, 14, 15
Setup time clock (decoder) to $\overline{\text{Reset AIS}}$	ts2		50		ns	Figs. 7, 14, 15
Setup time $\overline{\text{Reset AIS}}$ = '1' to clock (decoder)	ts2	31			ns	Figs. 14, 15
Propagation delay clock (decoder) to LIP			50	87	ns	

High Density Bipolar 3 (HDB3) is a pseudo-ternary signal in which the number of consecutive zeros that may occur is restricted to a maximum number of three. In any sequence of four consecutive binary zeros, the ultimate zero is substituted by a 'mark' (+ or -) of the same polarity as the previous mark, i.e. it violates AMI code (Alternate Mark Inversion) and is termed a 'violation'. To ensure parity between marks of opposite polarity, the first zero is substituted by an additional mark when there would otherwise be an even number of marks between 'violations'. Thus violations alternate in polarity.

FUNCTIONAL DESCRIPTION

Functions listed by pin number

1. NRZ data in

Input data for encoding into ternary form. The data is clocked by the negative going edge of the Clock (Encoder).

2. Clock (Encoder)

Clock for encoding data on pin 1.

3. LIP

Loss if input circuit detects eleven consecutive zeros at the decoder input and then gives an output high. Any logic '1' at the input (A_{IN} or B_{IN} = '0') resets this count.

4. NRZ data out

Decoded binary data from pseudo-ternary inputs A_{IN} and B_{IN}.

5. Clock (Decoder)

Clock for decoding data on A_{IN} and B_{IN}, or O_1 and O_2 in loop test mode.

6,7. $\overline{\text{Reset AIS}}$, AIS

Logic '0' on Reset AIS resets a decoded zero counter and either resets AIS output to '0' provided 3 or more zeros have been decoded in the preceding $\overline{\text{Reset AIS}}$ = 1 period, or sets AIS to '1' if less than 3 zeros have been decoded in the preceding $\overline{\text{Reset AIS}}$ = 1 period to indicate loss of time slot zero. Logic '1' on $\overline{\text{Reset AIS}}$ enables the internal decoded zero counter.

8. Ground

Zero volts.

9. Error

A logic '1' indicates that a violation of the HDB3 encoding law has been detected i.e. 3 '1's of the same polarity.

10. Clock R

OR function of $\overline{A}_{IN}$, $\overline{B}_{IN}$ for clock regeneration when pin 12 = '0', OR function of O_1, O_2 when pin 12 = '1'.

11,13. $\overline{A}_{IN}$, $\overline{B}_{IN}$

Inputs representing the received ternary PCM signal. $\overline{A}_{IN}$ = '0' represents a positive going '1', $\overline{B}_{IN}$ = '0' represents a negative going '1'. $\overline{A}_{IN}$ and $\overline{B}_{IN}$ are sampled by the positive going edge of the clock decoder. $\overline{A}_{IN}$ and $\overline{B}_{IN}$ may be interchanged.

12. Loop test enable

TTL input to select normal or loop back operation. Pin 14 = '0' selects normal operation, encode and decode are independent and asynchronous. When pin 14 = '1' O_1, is connected internally to A_{IN} and O_2 to B_{IN}. Clock R becomes the OR function of O_1, O_2. N.B. A decode clock has to be supplied, or regenerated. The delay from NRZ in (pin 1) to NRZ out (pin 4) is about 6¾ clock periods in loop back.

14,15. O_1, O_2

Outputs representing the ternary encoded PCM HDB3 signal for line transmission. O_1 and O_2 are in Return to zero from and are clocked out on the positive going edge of the encode clock. The length of O_1 and O_2 pulses is set by the positive clock pulse length. Use suitable line drivers from these two outputs such that O_1 gives positive going pulse and O_2 gives negative going pulse.

16. $+V_{CC}$

Positive 5V ± 10% supply.

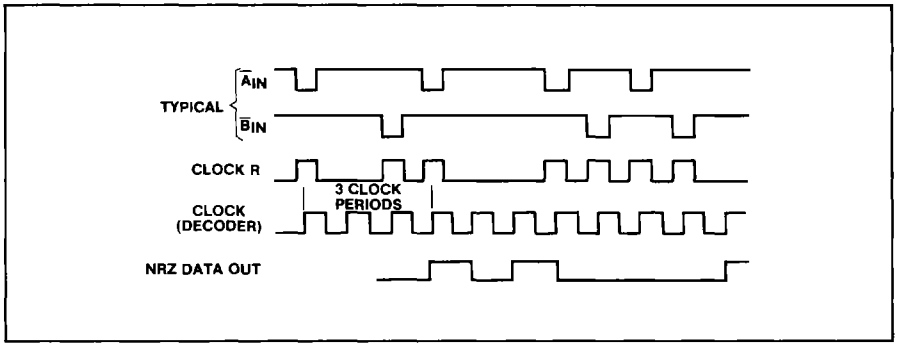

Fig. 3 Decode waveforms

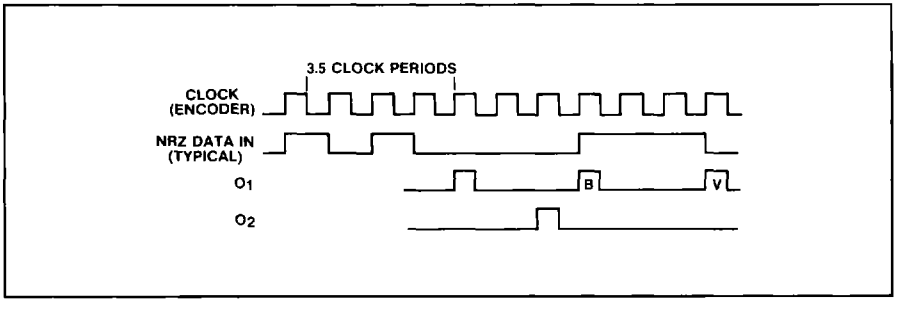

Fig.4 Encode waveforms

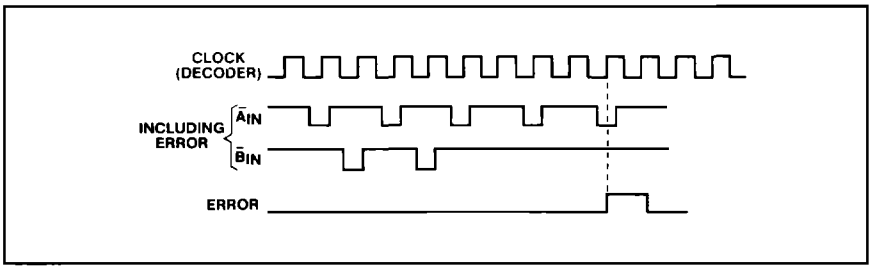

Fig.5 HDB3 error output waveforms

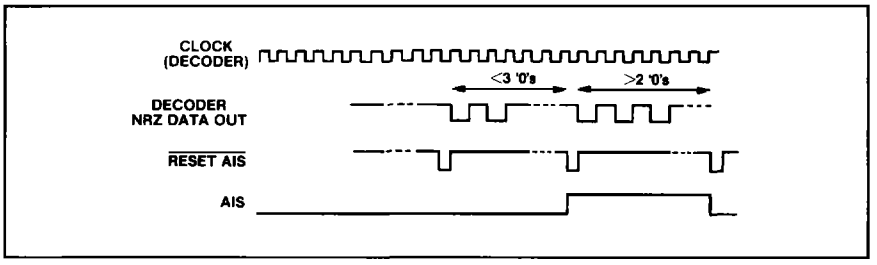

Fig.6 AIS error and Reset waveforms

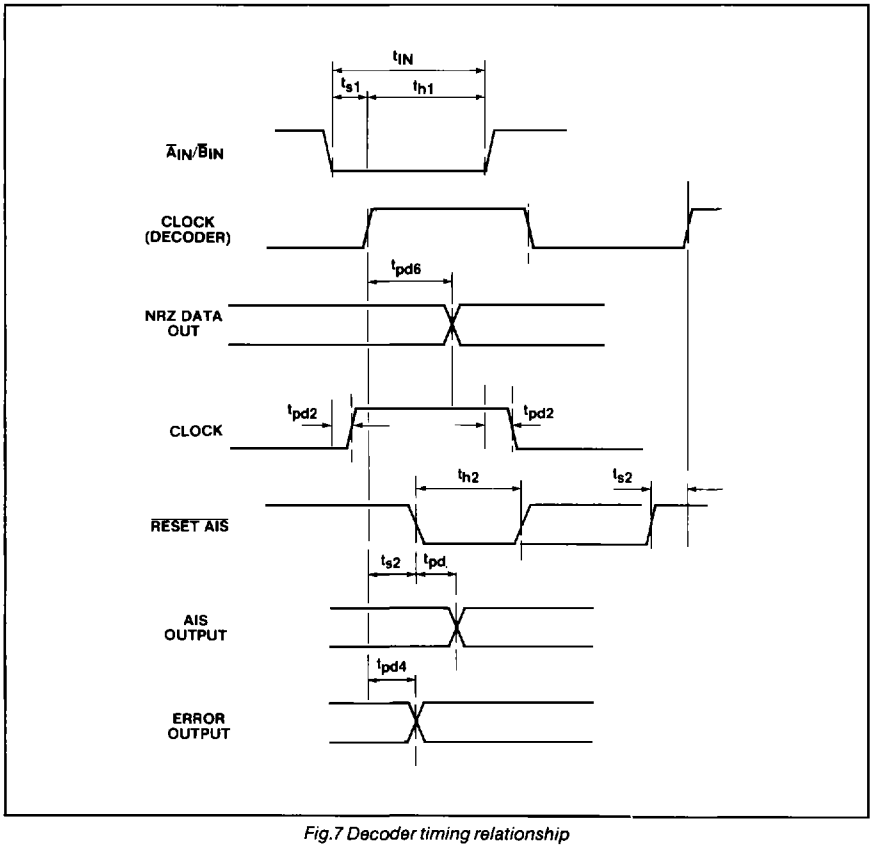

Fig.7 Decoder timing relationship

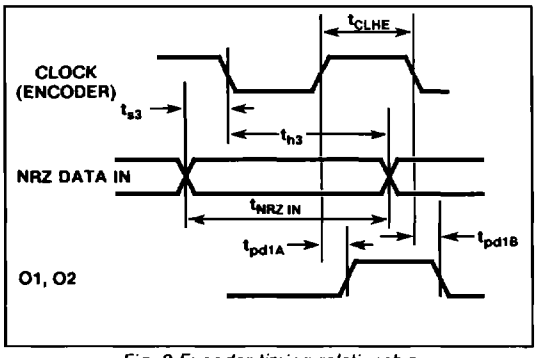

Fig. 8 Encoder timing relationship

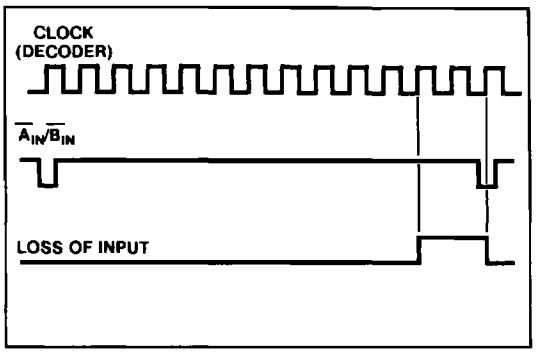

Fig. 9 Loss of input waveforms

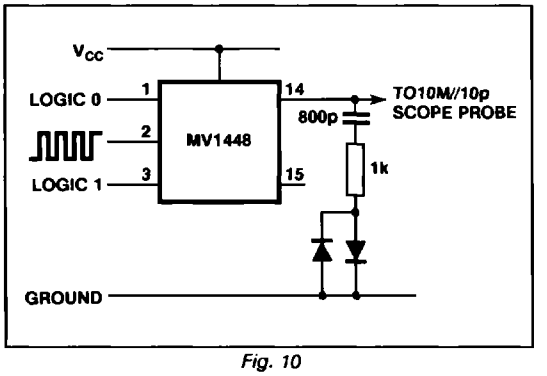

Fig. 10

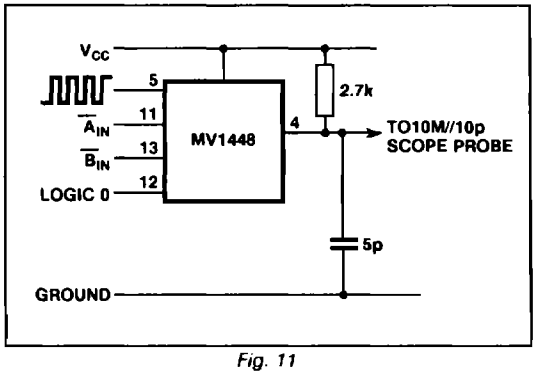

Fig. 11

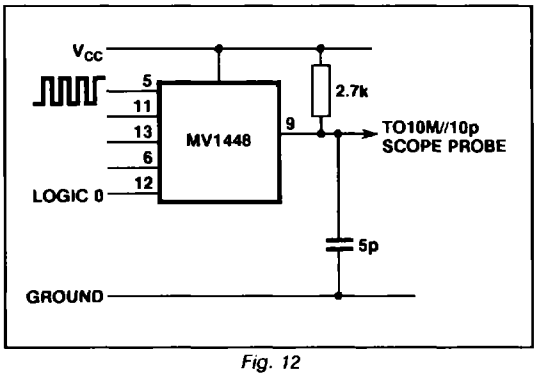

Fig. 12

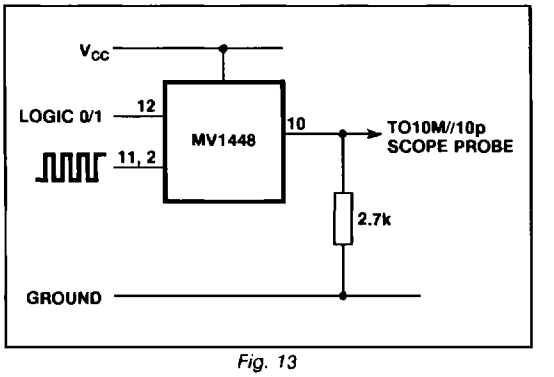

Fig. 13

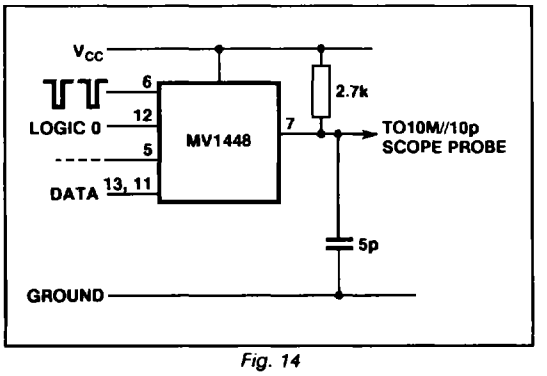

Fig. 14

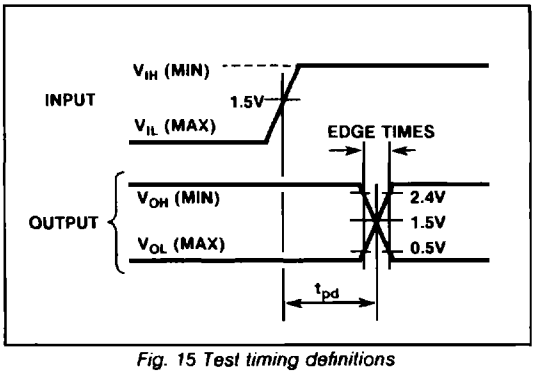

Fig. 15 Test timing definitions