

1x4Mx32bit DRAM Card
2x4Mx32bit DRAM Card
1x4Mx36bit DRAM Card
2x4Mx36bit DRAM Card

MF116M-L17ATXX
MF132M-L17ATXX
MF116M-L27ATXX
MF132M-L27ATXX

Connector Type

Two-piece 88-pin

DESCRIPTION

These DRAM CARDS are developed based on JEIDA DRAM CARD GUIDELINE Ver. 2.0. These cards are made using industry standard 4 M × 4 and 4 M × 1 Dynamic RAM and interface IC's in TSOP.

FEATURES

- All inputs except RAS inputs are buffered.
- Standard card size : 54mm (W) × 85.6mm (L) × 3.3mm (T)
- 88pin 2 piece connector type.
- RAS only refresh mode. CAS before RAS refresh mode and Page mode functions are available.
- Extended refresh is available. (128ms/2048cycle)

APPLICATIONS

Main/expansion memory unit for Personal Computer. Laser-Printer, FAX etc.

PRODUCT LIST

Product No.	Item Type name	Memory capacity	Data Bus width (bits)	Access time (tRAC) (ns)	Connector type	Number of pins	Outline drawing
No. 1	MF116M-L17ATXX	16MB	32	70	Two-piece	88	88P-001
No. 2	MF132M-L17ATXX	32MB	(without parity)				
No. 3	MF116M-L27ATXX	16MB	36				
No. 4	MF132M-L27ATXX	32MB	(with parity)				

DYNAMIC RAM CARDS

PIN ASSIGNMENT

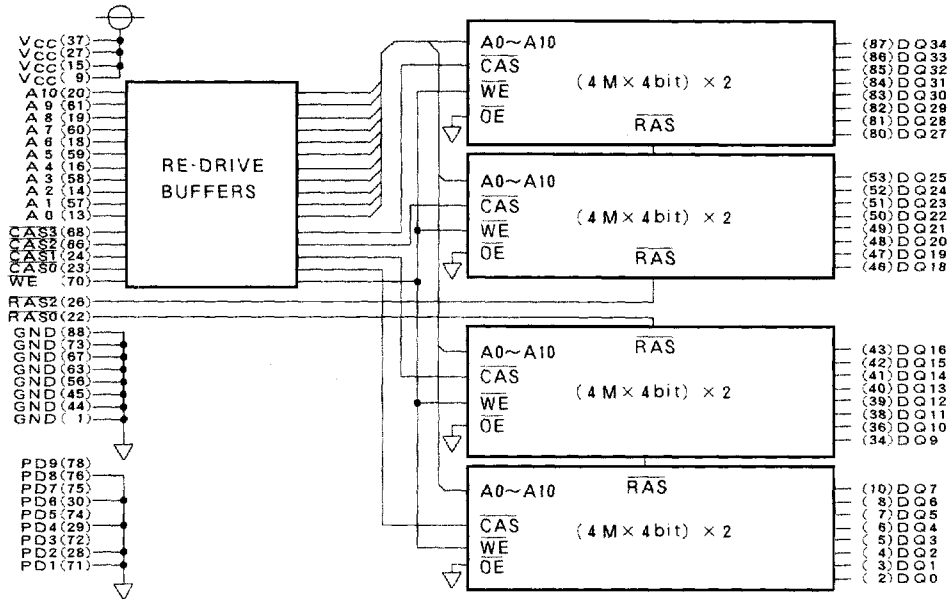
Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	GND	Ground	45	GND	Ground
2	DQ 0	Data I/O	46	DQ18	Data I/O
3	DQ 1		47	DQ19	
4	DQ 2		48	DQ20	
5	DQ 3		49	DQ21	
6	DQ 4		50	DQ22	
7	DQ 5		51	DQ23	
8	DQ 6		52	DQ24	
9	V _{CC}	Power supply voltage	53	DQ25	Data I/O (NC for No. 1, No. 2)
10	DQ7	Data I/O	54	DQ26	
11	NC	No connection	55	NC	No connection
12	DQ 8	Data I/O (NC for No. 1, No. 2)	56	GND	Ground
13	A 0	Address input	57	A 1	Address input
14	A 2		58	A 3	
15	V _{CC}	Power supply voltage	59	A 5	
16	A 4	Address input	60	A 7	No connection
17	NC	No connection	61	A 9	
18	A 6	Address input	62	NC	No connection
19	A 8		63	GND	Ground
20	A10	No connection	64	NC	No connection
21	NC		65	<u>RAS</u> 1	Row address strobe 1 (NC for No. 1, No. 3)
22	<u>RAS</u> 0	Row address strobe 0	66	<u>CAS</u> 2	Column address strobe 2
23	<u>CAS</u> 0	Column address strobe 0	67	GND	Ground
24	<u>CAS</u> 1	Column address strobe 1	68	<u>CAS</u> 3	Column address strobe 3
25	NC	No connection	69	<u>RAS</u> 3	Row address strobe 3 (NC for No. 1, No. 3)
26	<u>RAS</u> 2	Row address strobe 2	70	<u>WE</u>	Write enable
27	V _{CC}	Power supply voltage	71	PD 1	Presence detect 1
28	PD 2	Presence detect 2	72	PD 3	Presence detect 3
29	PD 4	Presence detect 4	73	GND	Ground
30	PD 6	Presence detect 6	74	PD 5	Presence detect 5
31	NC	No connection	75	PD 7	Presence detect 7
32	NC		76	PD 8	Presence detect 8
33	DQ17	Data I/O (NC for No. 1, No. 2)	77	NC	No connection
34	DQ 9	Data I/O	78	PD 9	Presence detect 9
35	NC	No connection	79	DQ35	Data I/O (NC for No. 1, No. 2)
36	DQ10	Data I/O	80	DQ27	Data I/O
37	V _{CC}	Power supply voltage	81	DQ28	
38	DQ11	Data I/O	82	DQ29	
39	DQ12		83	DQ30	
40	DQ13		84	DQ31	
41	DQ14		85	DQ32	
42	DQ15		86	DQ33	
43	DQ16		87	DQ34	
44	GND	Ground	88	GND	Ground

PD Pin Table

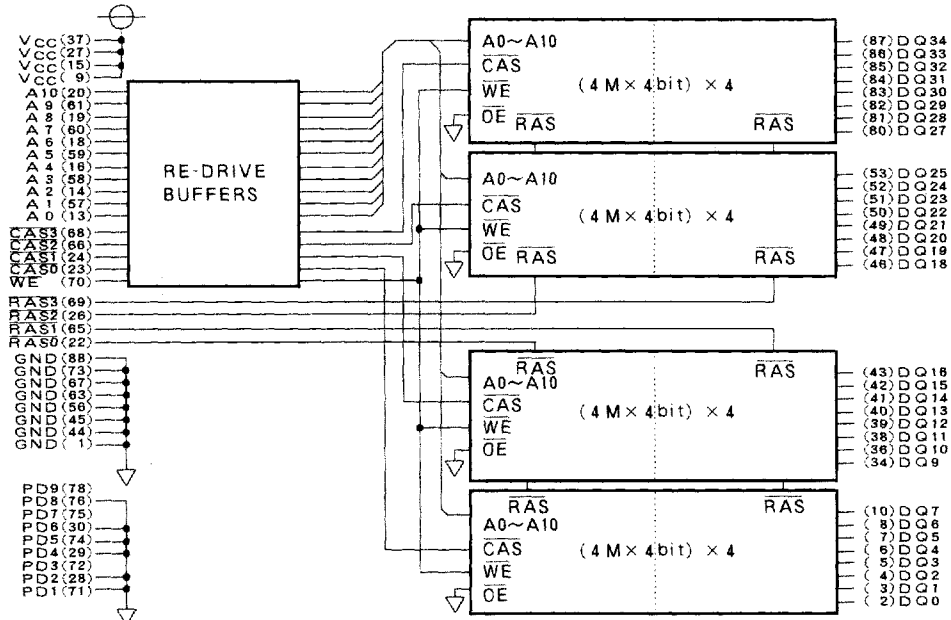
Product No.	PD 1	PD 2	PD 3	PD 4	PD 5	PD 6	PD 7	PD 8	PD 9
No. 1	GND	GND	NC	GND	NC	GND	NC	GND	NC
No. 2	GND	GND	NC	GND	GND	GND	NC	GND	NC
No. 3	GND	GND	NC	GND	NC	GND	NC	GND	NC
No. 4	GND	GND	NC	GND	GND	GND	NC	GND	NC

DYNAMIC RAM CARDS

BLOCK DIAGRAM (No.1)

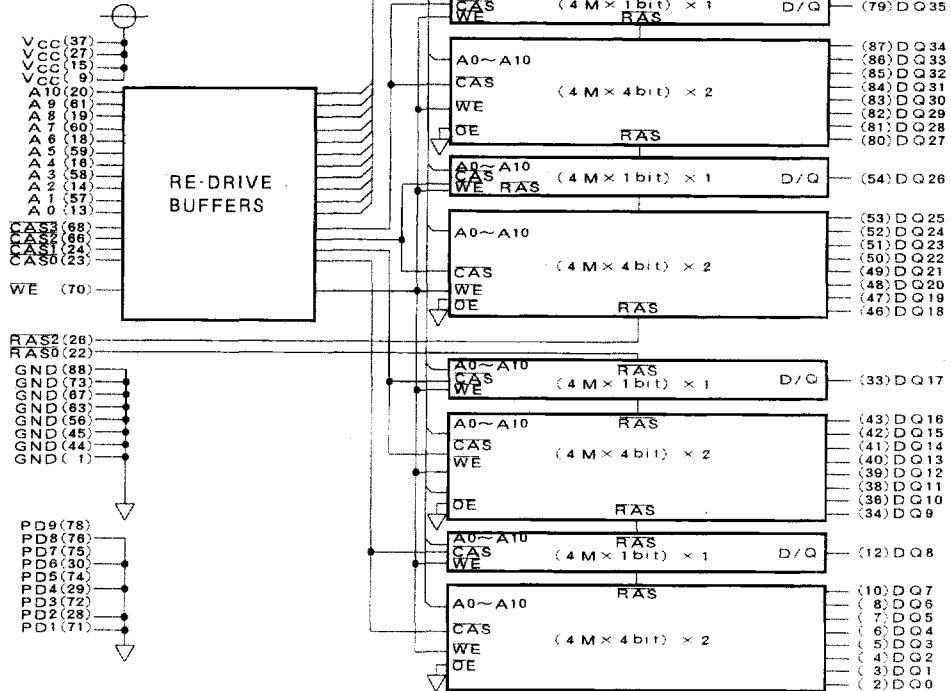


BLOCK DIAGRAM (No.2)

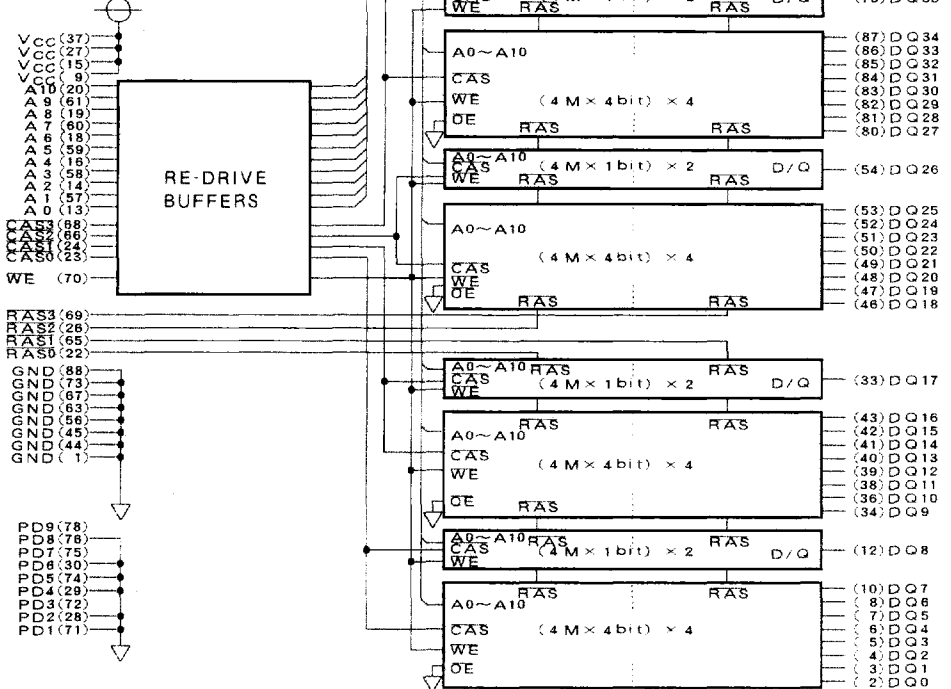


DYNAMIC RAM CARDS

BLOCK DIAGRAM (No.3)



BLOCK DIAGRAM (No.4)



DYNAMIC RAM CARDS

FUNCTION TABLE

Operation	input				input/output		Refresh	Note
	RAS	CAS	WE	Row Address	Column Address	input	output	
Read	ACT	ACT	NAC	APD	APD	OPN	VLD	YES
Early write	ACT	ACT	ACT	APD	APD	VLD	OPN	YES
RAS only refresh	ACT	NAC	DNC	APD	DNC	DNC	OPN	YES
CAS before RAS refresh	ACT	ACT	NAC	DNC	DNC	DNC	OPN	YES
Self refresh	ACT	ACT	NAC	DNC	DNC	DNC	OPN	YES
Standby	NAC	DNC	DNC	DNC	DNC	DNC	OPN	NO

Note 1 : ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, APD : applied, OPN : open
Don't be active the even and odd No. RASs at the same time. (Read/Early write cycle only)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings				Unit
			No. 1	No. 2	No. 3	No. 4	
V _{CC}	Supply voltage	With respect to GND	-1.0~7.0				V
V _I	Input voltage		-1.0~7.0				V
V _O	Output voltage		-1.0~7.0				V
I _O	Output current	T _a = 25°C	50				mA
P _d	Power dissipation		8	16	12	24	W
T _{opr}	Operating temperature		0~55				°C
T _{stg}	Storage temperature		-40~80				°C

RECOMMENDED OPERATING CONDITIONS (T_a = 0 ~ 55°C, unless otherwise noted): (Note 2)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V _{CC}	Supply voltage	4.75	5	5.25	V
GND	Supply voltage	0	0	0	V
V _{IH}	High input voltage	0.7 × V _{CC}		V _{CC}	V
V _{IL}	Low input voltage	0		0.8	V

Note 2 : With respect to GND

DYNAMIC RAM CARDS

ELECTRICAL CHARACTERISTICS ($T_A = 0 \sim 55^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 5\%$, $GND = 0\text{V}$) : (Note 3)

Symbol	Parameter	Test condition	Limits										Unit
			Min.				Typ.	Max.					
			No. 1	No. 2	No. 3	No. 4		No. 1	No. 2	No. 3	No. 4		
V _{OH}	High output voltage	I _{OH} = − 5 mA	2. 4					V _{CC}				V	
V _{OL}	Low output voltage	I _{OL} = 4. 2mA	0					0. 4				V	
I _{OZ}	Off-stage output current	0 V ≤ V _{OUT} ≤ V _{CC}	− 10	− 20	− 10	− 20		10	20	10	20	μ A	
I _I	Input current	0 V ≤ V _{IN} ≤ V _{CC} Other input pins = 0 V	− 40		− 60			40		60		μ A	
I _{CC1(AV)}	Average supply current from V _{CC} , operating (Note 4, 5, 6)	$\overline{RAS}$, $\overline{CAS}$ cycling trc = twc = min, output open						900	920	1250	1280	mA	
I _{CC2(AV)}	Supply current from V _{CC} , standby (Note 7)	$\overline{RAS} = \overline{CAS} \geq V_{CC} - 0.2V$, other input pins ≥ V _{CC} − 0.2V or ≤ 0.2V, output open						3. 2	6. 4	3. 6	7. 2	mA	
I _{CC3(AV)}	Average supply current from V _{CC} , refreshing (Note 4, 6)	$\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$ trc = min, output open						890	1750	1240	2450	mA	
I _{CC4(AV)}	Average supply current from V _{CC} , Page-Mode (Note 4, 5, 6)	$\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling trc = min, output open						530	580	890	970	mA	
I _{CC6(AV)}	Average supply current from V _{CC} , $\overline{CAS}$ before RAS refresh mode (Note 4, 6)	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling trc = min, output open						850	1700	1160	2300	mA	
I _{CC8(AV)}	Average supply current from V _{CC} , Extended refresh mode (Note 7)	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling WE ≥ V _{CC} − 0. 2V other input pins ≥ V _{CC} − 0. 2V or ≤ 0. 2V, output open trc = 62. 5 μ s						5	10	5. 7	11. 4	mA	
I _{CC9(AV)}	Average supply current from V _{CC} , Self refresh mode (Note 7)	$\overline{RAS} = \overline{CAS} \leq 0. 2V$, WE ≥ V _{CC} − 0. 2V output open						5	10	5. 7	11. 4	mA	

Note 3 : Current flowing into a CARD is positive, out is negative.

4 : $I_{CC1(AV)}$, $I_{CC3(AV)}$, $I_{CC4(AV)}$ and $I_{CC6(AV)}$ are dependent on cycle rate.

Specified values are obtained at the fastest cycle rate.

5 : $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading.

Specified values are obtained with the outputs open.

6 : Column Address can be changed once or less while $\overline{RAS} = V_{IL}$ and $\overline{CAS} = V_{IH}$.

DYNAMIC RAM CARDS

SWITCHING CHARACTERISTICS ($T_a = 0 \sim 55^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 5\%$, $GND = 0\text{V}$): (Note 7)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_{CAC}	Access time from $\overline{\text{CAS}}$ (Note 8, 9)		27	ns
t_{RAC}	Access time from $\overline{\text{RAS}}$ (Note 8, 10)		70	ns
t_{CAA}	Column Address access time (Note 8, 11)		42	ns
t_{OFF}	Output disable time after $\overline{\text{CAS}}$ high (Note 12)	0	27	ns

Note 7 : An initial pause of 500 μ sec is required after power-up followed by any 8 $\overline{\text{RAS}}$ or $\overline{\text{RAS}}/\overline{\text{CAS}}$ cycles before proper device operation is achieved. Note that $\overline{\text{RAS}}$ may be cycled during the initial pause. And any 8 $\overline{\text{RAS}}$ or $\overline{\text{RAS}}/\overline{\text{CAS}}$ cycles are required after prolonged periods of $\overline{\text{RAS}}$ inactivity before proper device operation is achieved.

8 : Measured with a load circuit equivalent to 2 TTL loads and 100pF.

9 : Assume that $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$.

10 : Assume that $t_{RCD} \leq t_{RCD(max)}$ and $t_{RAD} \leq t_{RAD(max)}$.

11 : Assume that $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$.

12 : $t_{OFF(max)}$ define the time at which the output achieves the high impedance state ($|I_{out}| \leq 10\text{ }\mu\text{A}$ or $20\text{ }\mu\text{A}$) and are not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

TIMING REQUIREMENTS ($T_a = 0 \sim 55^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 5\%$, $GND = 0\text{V}$): (Note 13, 14)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_{REF}	Refresh cycle time		32	ms
t_{REF}	Refresh cycle time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycling)		128	ms
t_{RP}	$\overline{\text{RAS}}$ high pulse width	50		ns
t_{RCD}	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ low (Note 15)	20	43	ns
t_{CRP}	Delay time, $\overline{\text{CAS}}$ high to $\overline{\text{RAS}}$ low (Note 16)	17		ns
t_{RPC}	Precharge to $\overline{\text{CAS}}$ active time.	0		ns
t_{CPN}	$\overline{\text{CAS}}$ high pulse width	10		ns
t_{RAD}	Column address delay time from $\overline{\text{RAS}}$ low (Note 17)	17	28	ns
t_{ASR}	Row address setup time before $\overline{\text{RAS}}$ low	10		ns
t_{ASC}	Column address setup time before $\overline{\text{CAS}}$ low (Note 18)	5	10	ns
t_{RAH}	Row address hold time after $\overline{\text{RAS}}$ low	10		ns
t_{CAH}	Column address hold time after $\overline{\text{CAS}}$ low	15		ns
t_T	Transition time (Note 19)	3	50	ns

Note 13 : The timing requirements are assumed $t_T = 5\text{ ns}$.

14 : $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.

15 : $t_{RCD(max)}$ is specified as a reference point only.

If $t_{RCD} \geq t_{RCD(max)}$, access time is defined as t_{CAC} and t_{CAA} .

16 : t_{CRP} requirement is applicable for all $\overline{\text{RAS}}/\overline{\text{CAS}}$ cycles.

17 : $t_{RAD(max)}$ is specified as a reference point only.

If $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$, access time is assumed by t_{CAA} for read cycle.

18 : $t_{ASC(max)}$ is specified as a reference point only of address access time.

19 : t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

DYNAMIC RAM CARDS

Read and Refresh Cycles

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t _{RC}	Read cycle time	130		ns
t _{RAS}	RAS low pulse width	70	10000	ns
t _{CAS}	CAS low pulse width	20	10000	ns
t _{CSH}	CAS hold time after RAS low	70		ns
t _{RSH}	RAS hold time after CAS low	27		ns
t _{RSC}	Read setup time before CAS low	5		ns
t _{RCH}	Read hold time after CAS high	0		ns
t _{RRH}	Read hold time after RAS high	10		ns

Write Cycle (Early Write)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t _{WC}	Write cycle time	130		ns
t _{RAS}	RAS low pulse width	70	10000	ns
t _{CAS}	CAS low pulse width	20	10000	ns
t _{CSH}	CAS hold time after RAS low	70		ns
t _{RSH}	RAS hold time after CAS low	27		ns
t _{WCS}	Write setup time before CAS low	5		ns
t _{WCH}	Write hold time after CAS low	15		ns
t _{DS}	Data setup time	10		ns
t _{DH}	Data hold time after CAS low	22		ns

Page Mode Cycle (Read, Early Write)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t _{PC}	Read, Write cycle time	55		ns
t _{CP}	CAS high pulse width	10		ns
t _{RAS}	RAS low pulse width (Note 20)	125	100000	ns

Note 20 : t_{RAS}(min) is specified by the following formula as two cycles of CAS input are executed.

$$t_{RAS}(\text{min}) = t_{CSH}(\text{min}) + t_{PC}(\text{min}).$$

CAS before RAS Refresh Cycle (Note 21)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t _{CSR}	CAS setup time for CAS before RAS refresh	20		ns
t _{CHR}	CAS hold time for CAS before RAS refresh	15		ns

Note 21 : Eight or more CAS before RAS cycles are necessary for proper operation of CAS before RAS refresh mode.

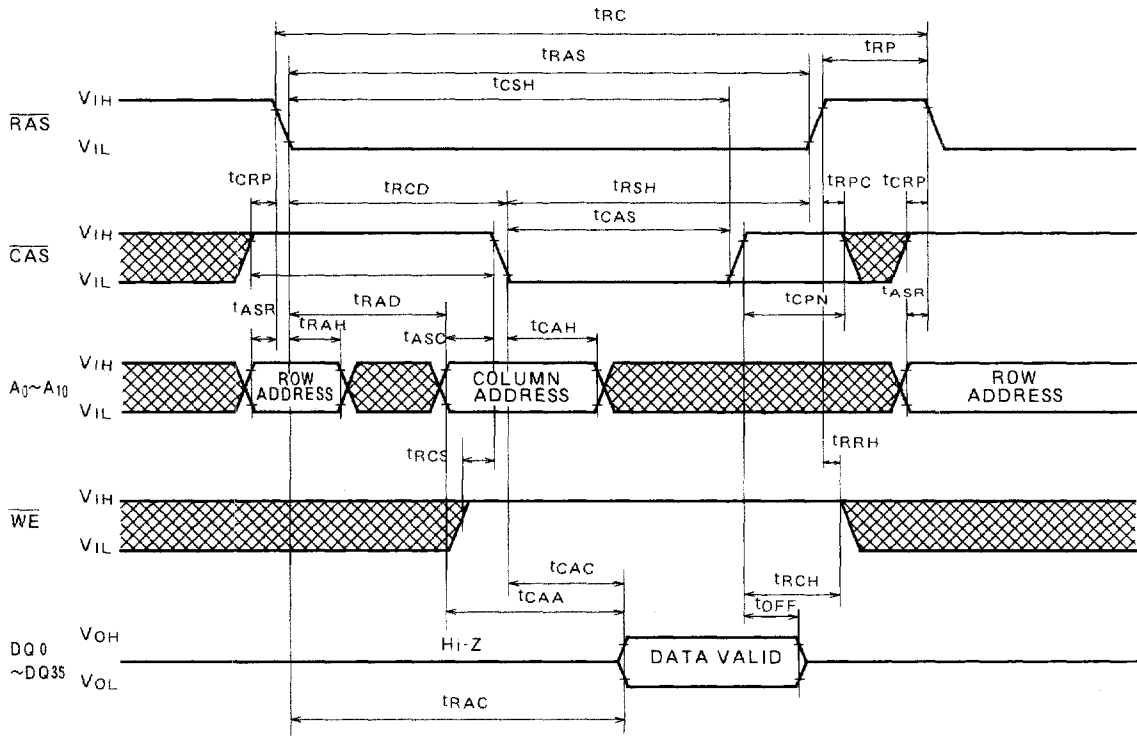
Self Refresh Cycle

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t _{RASS}	RAS low pulse width	100		ns
t _{RPS}	CAS high pulse width	130		ns
t _{CHS}	RAS hold time after RAS high	-50		ns

DYNAMIC RAM CARDS

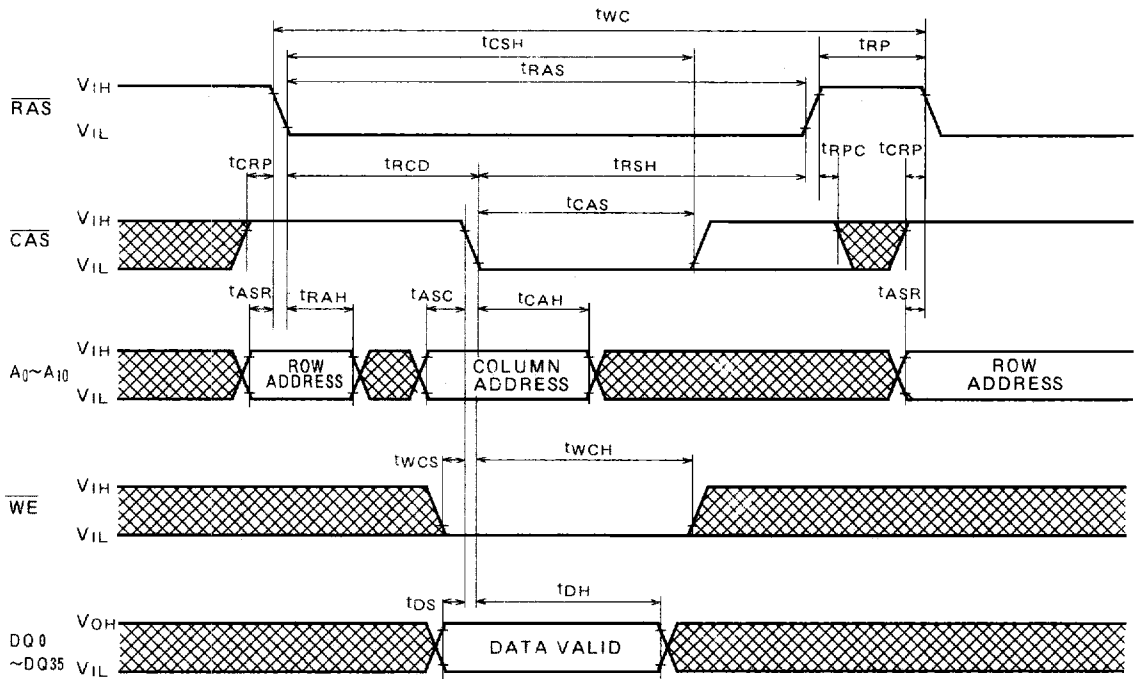
TIMING DIAGRAMS (Note 22)

Read Cycle

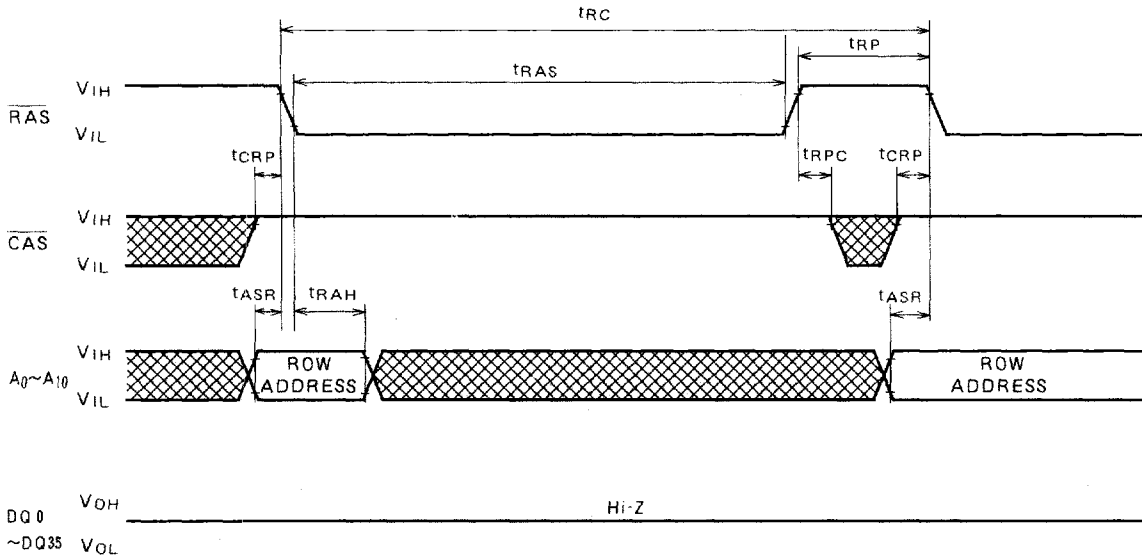
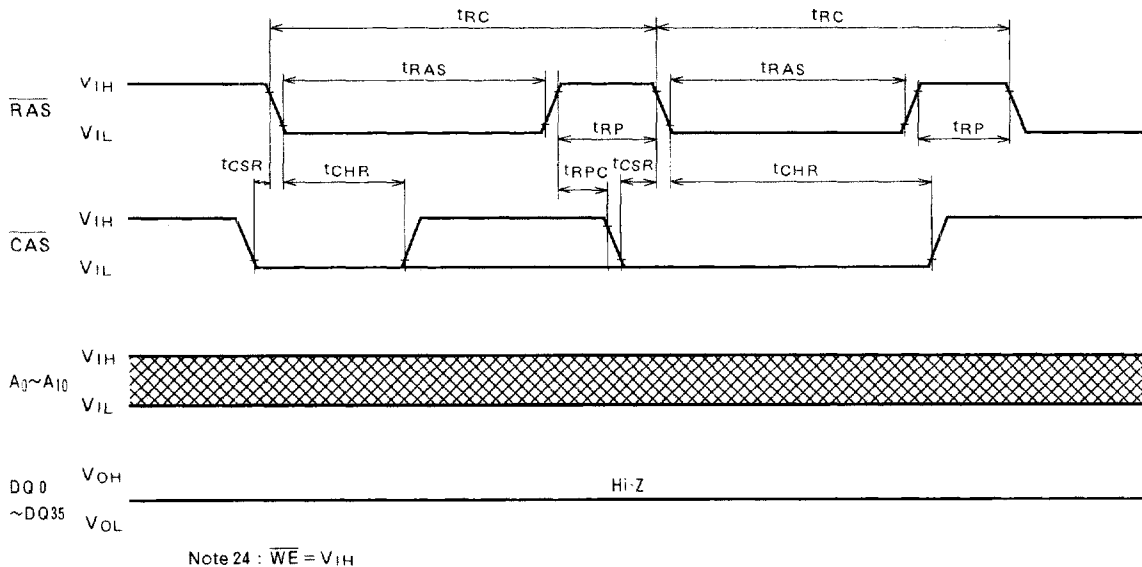


Note 22 :  Indicates the don't care input.

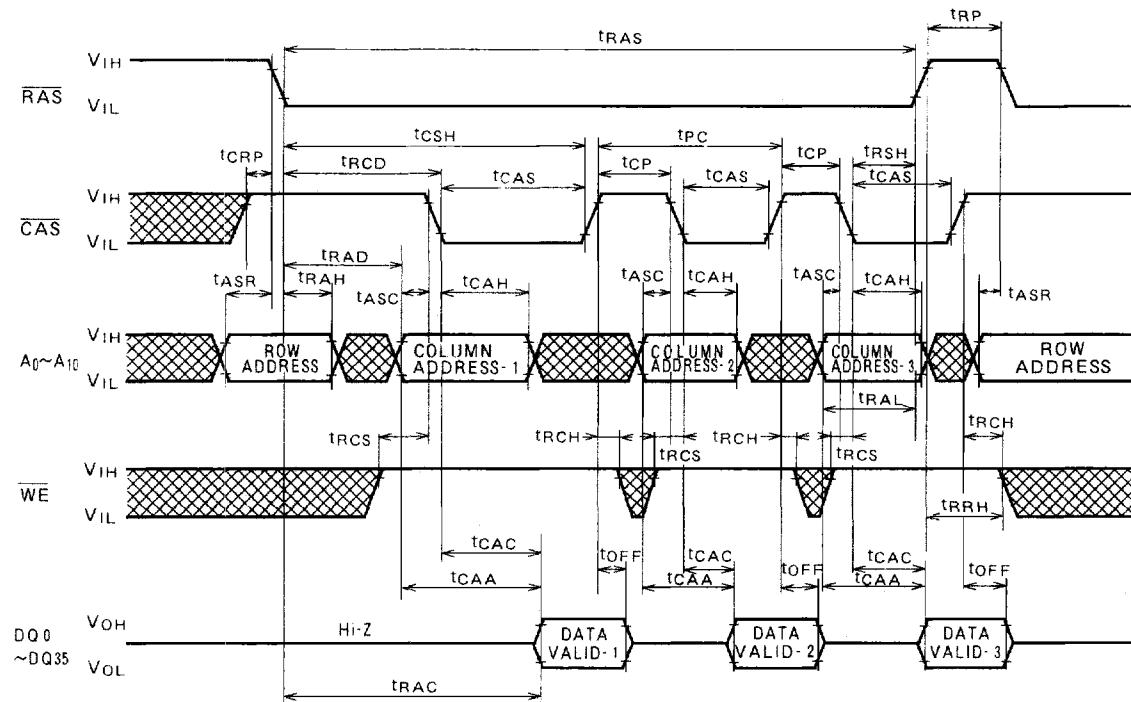
Early Write Cycle



DYNAMIC RAM CARDS

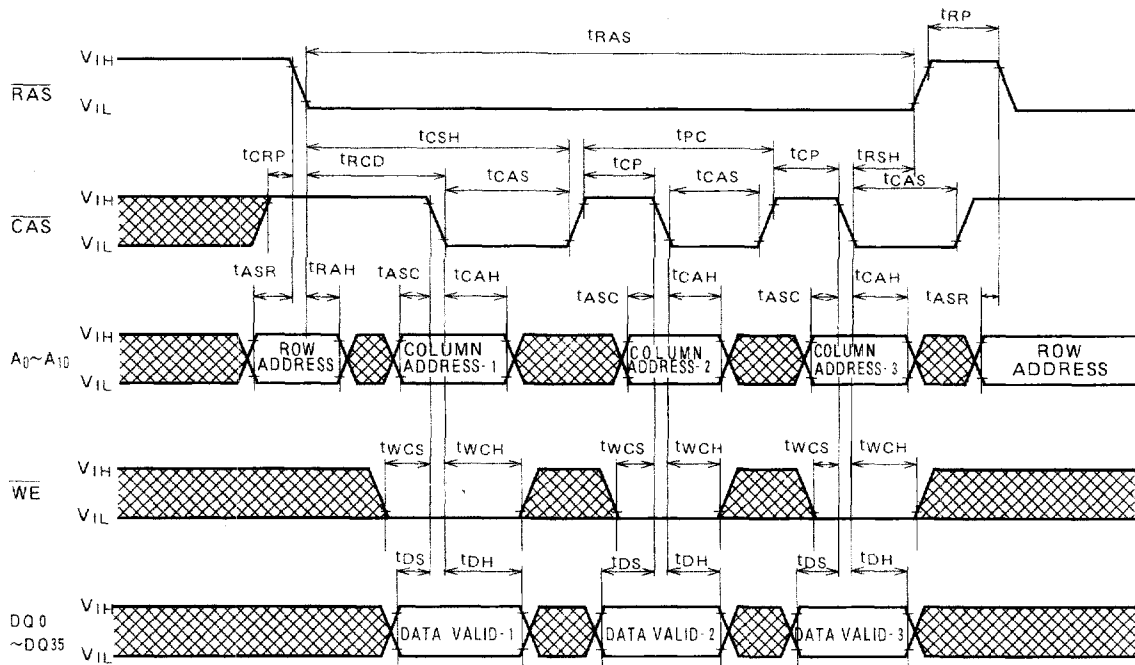
RAS only Refresh Cycle (Note 23)

CAS before RAS Refresh Cycle (Note 24)


Page-Mode Read Cycle



DYNAMIC RAM CARDS

Page-Mode Early Write Cycle



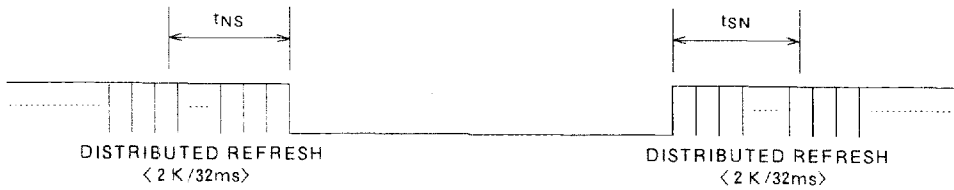
2-88

DYNAMIC RAM CARDS

Note 26 : SELF REFRESH ENTRY & EXIT CONDITIONS

(1) In case of distributed refresh

The last/first full refresh cycles (2 K) must be made within t_{NS}/t_{SN} before/after self refresh, on the condition of $t_{NS} \leq 32\text{ms}$ and $t_{SN} \leq 32\text{ms}$.



(2) In case of burst refresh

The last/first full refresh cycles (2 K) must be made within t_{NS}/t_{SN} before/after self refresh, on the condition of $t_{NS} + t_{SN} \leq 32\text{ms}$.

