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SSI 32H6825A
Servo and Spindle Predriver

Advance Information

April 1994

DESCRIPTION

The SSI 32H6825A Servo and Spindle Predriver (SSP) is designed to drive a 3-phase hall-sensorless motor and a voice coil actuator with external MOS power devices.

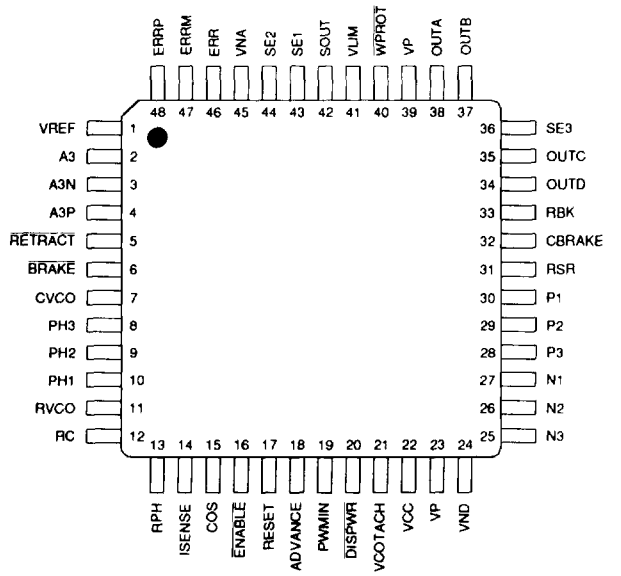
Improvements to the actuator driver include a window comparator to quickly catch high currents caused by power FET failure in the actuator bridge, an uncommitted opamp for use in a notch filter, and reduced power dissipation.

Improvements to the spindle driver include significantly reduced power dissipation, a µP controlled start up ramp to replace the imprecise analog ramp, an external PWM input to allow PWM frequencies above the audible range, active pullup on the P driver, adjustable N-channel slew rate, and improved spindle brake performance.

FEATURES

- **Spindle driver is PWM during run and start**
- **Commutator is driven by a phase lock loop for high jitter immunity**
- **Significantly reduced power dissipation**
- **Adjustable slew rate to minimize stress in the power FETs**
- **Microprocessor controlled spindle start up**
- **Window comparator to monitor actuator bridge fault**
- **Small footprint 48-Lead TQFP package**

PIN DIAGRAM



48-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

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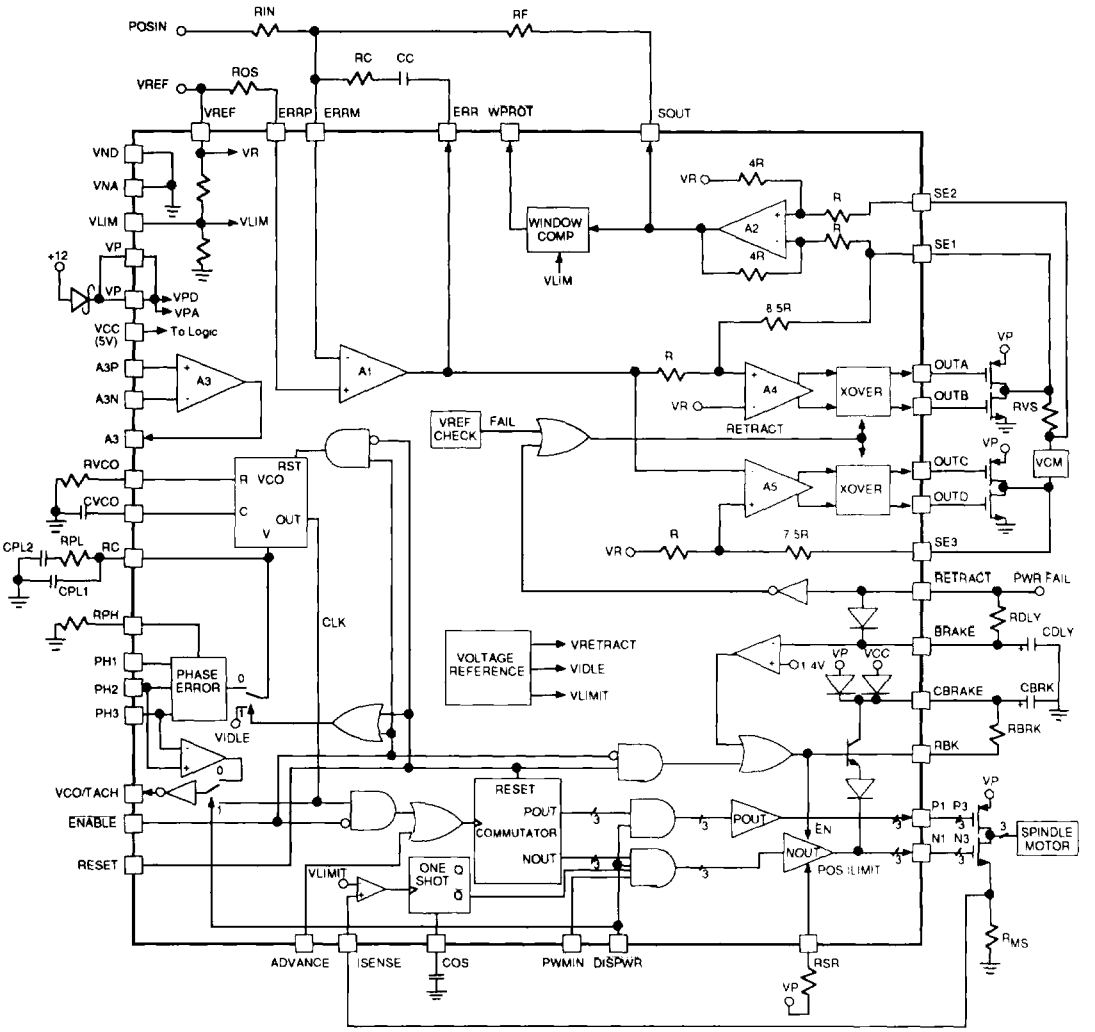
SSI 32H6825A
Servo and Spindle Predriver

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

ACTUATOR

The actuator section consists of A1 through A5, the window comparator, the VREF check, and the XOVER blocks. It is functionally identical to the SSI 32H6231. During linear operation, an acceleration signal from the servo controller is applied through amplifier A1, whose three connections are all available externally. RC components may be used to provide loop compensation at this stage. The ERR signal drives two precision amplifiers, each with a gain of 8.5. The first of these amplifiers is inverting, and is formed from opamp A4, an on-chip resistor divider and an off-chip complementary MOSFET pair. The second is non-inverting, and is formed in a similar manner from opamp A5. Feedback from the MOSFET drains, on sense inputs SE1 and SE3, allows the amplifiers gains to be established precisely. The voice coil motor and a series current sense resistor are connected between SE1 and SE3.

Crossover protection circuitry between the outputs of A4 and A5, and the external MOSFETs, ensures class B operation by allowing only one MOSFET in each leg of the H-bridge to be in conduction. The crossover separation threshold, illustrated in Figure 1, is the maximum drive on any MOSFET gate when the motor voltage changes sign. The crossover circuitry can also apply a constant voltage across the motor (to retract the heads at a constant velocity).

Motor current is sensed by a small resistor placed in series with the motor. The voltage drop across this resistor is amplified by a differential amplifier with a gain of 4 (A2 and associated resistors), whose inputs are SE1 and SE2. The resulting voltage, SOUT, is proportional to motor current, and hence acceleration. This signal is externally fed back to A1, so that the signal ERR represents the difference between the desired acceleration (from the servo controller) and the actual motor acceleration.

SOUT is connected to a window comparator, which is used to detect excessive motor current. When excessive current is detected, WRPROT is pulled low. The VLIM pin may be used to program the voltage limit for the window comparator. The maximum voltage excursion allowed about VREF is (VREF-VLIM). An on-chip resistor divider sets a default value for VLIM and if VLIM is connected to ground, the windowing is effectively disabled.

The SSI 32H6825A has low voltage monitor circuitry that will detect a loss of voltage on VREF. The power supply pin, VP, should be connected to the disk drive's spindle motor so that its stored rotational energy may be used to hold up VP briefly during a power failure. When a low voltage condition is detected, the MOSFET drivers switch from linear operation to retract mode. In this mode a constant voltage is applied across the motor which will cause the heads to move at a constant speed. A mechanical stop must be provided for the heads when they reach a safe location.

The spindle driver monitors spindle back EMF and generates drive signals to 3 MOSFET power bridges. This section includes current limit, a back EMF monitoring circuit to determine commutation points, a phase locked loop to remove jitter from the commutation times, and a delayed spindle brake circuit.

COMMUTATOR

The commutator drives the spindle motor windings in the proper sequence to operate the 3 phase spindle motor. In Run mode, the commutator is clocked by CLK, the VCO output. In Start mode, the commutator is clocked by external pulses applied to the ADVANCE pin. Table 1 shows the commutator sequence and identifies which power FETS are on.

The commutator phase detector technology is licensed from Synektron, patent no. 4,928,043.

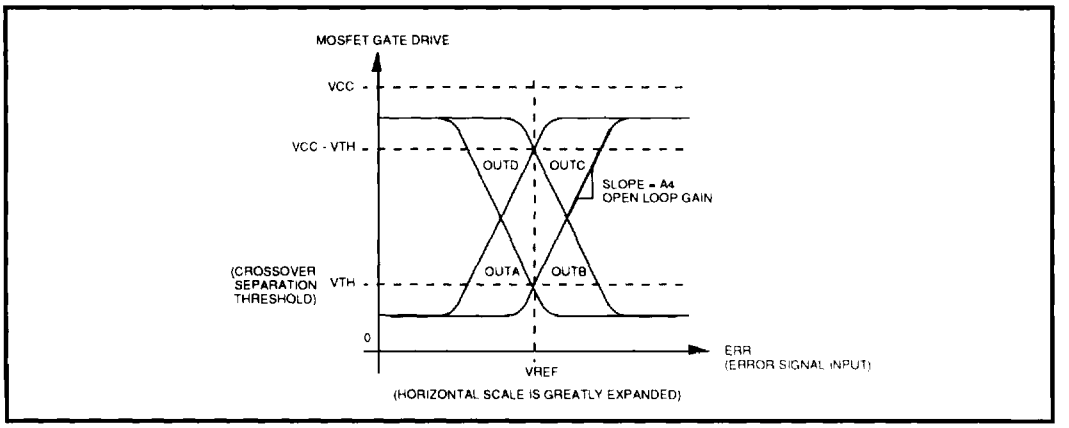


FIGURE 1: Crossover Protection

Table 1: Commutator Sequence

STATE	N1	N2	N3	P1	P2	P3
RST	OFF	ON	OFF	ON	OFF	ON
A	OFF	OFF	ON	ON	OFF	OFF
B	OFF	OFF	ON	OFF	ON	OFF
C	ON	OFF	OFF	OFF	ON	OFF
D	ON	OFF	OFF	OFF	OFF	ON
E	OFF	ON	OFF	OFF	OFF	ON
F	OFF	ON	OFF	ON	OFF	OFF

PHASE ERROR AMPLIFIER

The PHASE ERROR circuit compares the undriven winding with the average of the other two voltages. Depending on the result of the comparison and the state of the commutator, a positive or negative current is put out on the RC pin. Table 2 shows which winding is undriven and which polarity of current is output when that winding is positive with respect to the average of the other two.

Table 2: Undriven Winding and Polarity

Commutator State	Undriven Winding	Polarity
A	PH2	Source
B	PH1	Sink
C	PH3	Source
D	PH2	Sink
E	PH1	Source
F	PH3	Sink

FUNCTIONAL DESCRIPTION (continued)

PHASE ERROR AMPLIFIER (continued)

The PHASE ERROR circuit is only used when mode = RUN. In all other modes, RC is forced to V_{IDLE}, an internally generated voltage that will cause the VCO to idle at approximately 1/20 of the run rate.

The magnitude of the current at RC is the sum of a constant current and a current proportional to the VCO frequency. The constant current value is set by RPH which is biased to 1.2V nominally. The proportional current is set by RVCO, the same resistor that controls the VCO current. The RVCO pin is nominally the same voltage as the RC pin.

VCO

The VCO is a triangle wave oscillator with a wide frequency range set by RVCO and CVCO. The voltage swing on CVCO is nominally 2.2V. The frequency formula is:

$$F_{VCO} = \frac{V_{RC}}{8.8\ R_{VCO}\ C_{VCO}}$$

The VCO is reset if $\overline{ENABLE}$ = 1 and RESET = 0. During VCO reset, the CLK output is forced low. The first VCO clock will occur immediately on exiting reset. This timing relationship is shown in Figure 1.

ONE SHOT

The one shot is triggered whenever ISENSE exceeds VLIMIT (nominally 0.1V). When the one shot times out, it will remain high if ISENSE is still above VLIMIT. During the time the one shot output is high, the N drivers are turned off. This behavior implements PWM over-current limit, where the peak current is: $VLIMIT/R_{MS}$

VOLTAGE REFERENCE

The voltage reference circuit generates voltage and current references for the rest of the MSC section. Specifically, these voltages are 3.3V, VRETRACT, and VLIMIT. The circuit also generates the bias voltage: $1.2V + V_{be}(40\ \mu A)$

NOUT AND POUT

The NOUT drivers drive the gates of the N channel power FETs. They have an adjustable source current set by R_{SR}. During BRAKE, the NOUT drivers are disabled and all N channel power FETs are turned on. The POUT drivers drive the P channel power FETs. The POUT drivers are not deactivated during PWM.

DIGITAL INPUTS

All digital inputs are pulled to ground with a 20 kΩ (nominal) resistor to ensure a known state during system power failure.

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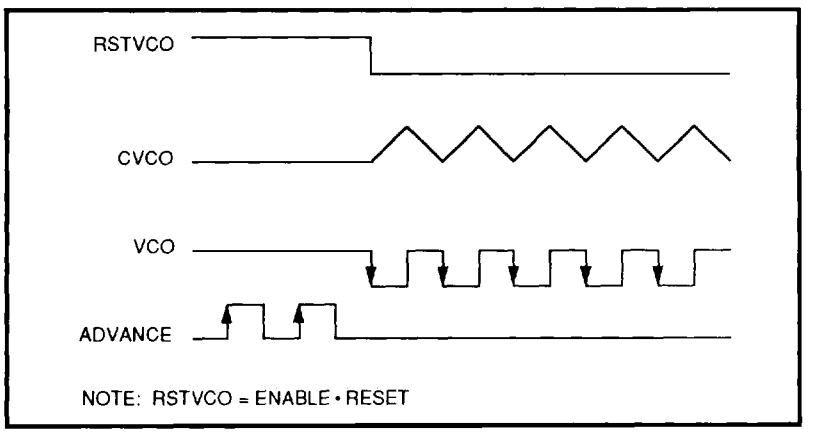

FIGURE 2: VCO Timing Diagram

PIN DESCRIPTION

SUPPLIES

NAME	TYPE	DESCRIPTION
GNDD GNDA	GROUND	Digital and Analog Grounds.
VCC	POWER	System 5V power supply.
VP	POWER	The 12V supply, diode protected from system 12V. Bridge supply for the spindle and actuator FETs.

ACTUATOR

VREF	AN INPUT	REFERENCE VOLTAGE. All actuator analog signals are referenced to this voltage.
VLIM	AN INPUT	LIMITING VOLTAGE. The voltage at this pin sets the $\overline{\text{WRPROT}}$ window comparator limits. Limiting occurs when: |SOUT-VREF| > VREF-VLIM An internal resistor divider establishes a default value that may be externally adjusted.
ERR	AN OUTPUT	POSITION ERROR. The loop compensation amplifier output. This signal is amplified by the MOSFET drivers and applied to the motor by an external MOSFET H-bridge as follows: SE3-SE1 = 17(ERR-VREF)
ERRM	AN INPUT	POSITION ERROR INVERTING INPUT. Inverting input to the loop compensation amplifier.
ERRP	AN INPUT	POSITION ERROR NON-INVERTING INPUT. Non-inverting input to the loop compensation amplifier.
SOUT	AN OUTPUT	MOTOR CURRENT SENSE OUTPUT. This output provides a voltage proportional to the voltage drop across the external current sense resistor, as follows: SOUT-VREF = 4(SE2-SE1)
$\overline{\text{WRPROT}}$	AN OUTPUT	WRITE PROTECT. Active low, an open collector output which is asserted when SOUT exceeds the window comparator limits.
SE2	AN INPUT	MOTOR CURRENT SENSE INPUT. Non-inverting input to the current sense differential amplifier. It should be connected to one side of an external current sensing resistor in series with the actuator. The inverting input of the differential amplifier is connected internally to SE1.
SE1	AN INPUT	MOTOR VOLTAGE SENSE INPUT. This input provides feedback to the inverting MOSFET driver amplifier and to the current sense amplifier. It is connected to the current sensing resistor which is in series with the motor. The gain to this point from ERR is: SE1-VREF = -8.5(ERR-VREF)

PIN DESCRIPTION (continued)

ACTUATOR (continued)

NAME	TYPE	DESCRIPTION
SE3	AN INPUT	MOTOR VOLTAGE SENSE INPUT. This input provides feedback to the non inverting MOSFET driver amplifier. It is connected to one side of the motor. The gain to this point from ERR is: SE3-VREF = 8.5(ERR-VREF)
OUTA, OUTC	AN OUTPUT	P-FET DRIVE. Drive signal for a P channel MOSFET connected between one side of the motor and VP.
OUTB, OUTD	AN OUTPUT	N-FET DRIVE. Drive signal for an N channel MOSFET connected between one side of the motor and GND. Crossover protection circuitry ensures that the P and N channel devices connected to the same side of the motor are never enabled simultaneously.
A3P	AN INPUT	NON-INVERTING A3 INPUT. Positive input to A3, the uncommitted opamp.
A3N	AN INPUT	INVERTING A3 INPUT. Negative input to A3, the uncommitted opamp.
A3	AN OUTPUT	A3 OUTPUT. The output of A3, the uncommitted opamp.

SPINDLE

P1, P2, P3	AN OUTPUT	P CHANNEL SPINDLE FET DRIVERS. These pins are connected to the three P channel power MOSFETs in the spindle motor power bridge.
N1, N2, N3	AN OUTPUT	N CHANNEL SPINDLE FET DRIVERS. These pins are connected to the three N channel power MOSFETs in the spindle motor power bridge.
RSR	COMPONENT	SOURCE CURRENT LIMIT. The peak source current at N1..N3 is set at 20x the current through RSR.
PWMIN	DIG INPUT	PULSE WIDTH MODULATION INPUT. Modulates the N channel power MOSFETs to control spindle motor current.
COS	COMPONENT	ONE SHOT CAPACITOR. Sets the time delay in the one shot. The one shot is clocked whenever the current in the spindle exceeds a limit controlled by R_{MS}.
ISENSE	AN INPUT	SPINDLE CURRENT SENSE. Connects to the spindle current sense resistor, R_{MS}, and is used during startup as part of the current limit circuitry.
VCO/TACH	DIG OUTPUT	SPEED CONTROL OUTPUT. Under normal operation ($\overline{DISPWR}$ = 1), this pin provides the speed sensitive signal used by the µP to control spindle speed. When $\overline{DISPWR}$ = 0, the pin provides the output of the TACH comparator.
RVCO	COMPONENT	VCO RESISTOR. Sets the speed range of the VCO. The voltage at RVCO is forced to track RC.

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SPINDLE (continued)

NAME	TYPE	DESCRIPTION
CVCO	COMPONENT	VCO CAPACITOR. Sets the speed range of the VCO.
RC	COMPONENT	PLL LOOP FILTER. Sets the time constant for the PLL in Run mode. In all other modes, it is connected to a DC voltage, V_{IDLE}. V_{IDLE} determines the VCO frequency at which crossover from startup to run should occur (by lowering $\overline{ENABLE}$).
RPH	COMPONENT	PHASE ERROR CURRENT SET. The pump current in the phase error amplifier is the sum of the VCO current (through RVCO) and the current through RPH.
PH1, PH2, PH3	AN INPUT	SPINDLE MOTOR TERMINALS. These pins are used to calculate the phase error in the PLL.

CONTROL

$\overline{RETRACT}$	DIG INPUT	POWER FAIL. Active low, this digital input should be asserted by external power fault detection circuitry. When low, this pin forces an actuator retract.
$\overline{BRAKE}$	AN INPUT	BRAKE. Active low, this input is pulled low by external circuitry to perform a delayed brake.
CBRAKE	COMPONENT	BRAKE CAPACITOR. A large capacitor is connected to CBRAKE to provide pullup to the N channel spindle MOSFETs during brake.
RBK	O/C OUTPUT	BRAKE RESISTOR. A high value (10 Meg) resistor is connected between CBRAKE and RBK to pull up the base of the brake transistor. This pin is pulled low while BRAKE is not asserted.
$\overline{DISPWR}$	DIG INPUT	DISABLE POWER. Active low, this input turns off the high and low sides of the spindle drivers. A brake command will over-ride $\overline{DISPWR}$. An internal pull down resistor guarantees a logic 0 when $\overline{DISPWR}$ floats.
$\overline{ENABLE}$ RESET	DIG INPUT	MODE CONTROLS. These inputs control the spindle modes according to the following truth table:

$\overline{ENABLE}$	RESET	MODE	RC	VCO	Commutator
0	0	Run	Run	Run	Run
0	1	Brake	V_{IDLE}	Idle	Rst
1	0	Start	V_{IDLE}	Rst	Run
1	1	Preset	V_{IDLE}	Idle	Rst

Note:

Spindle braking is activated in Brake mode. Brake mode, whether activated by $\overline{ENABLE}$ and RESET or by a power failure is internally latched and can only be turned off by asserting Preset mode.

ADVANCE	DIG INPUT	COMMUTATION ADVANCE. A rising edge on this pin will cause the commutator to advance whenever RESET is low. While high, ADVANCE prevents other commutation clocks from occurring.

ELECTRICAL SPECIFICATIONS

Recommended conditions apply unless otherwise specified.

ABSOLUTE MAXIMUM RATINGS

Operation outside these rating limits may cause permanent damage to this device.

PARAMETER	RATING
VP	0 to 14V
VCC	0 to 7V
VREF	0 to 10V
SE1, SE2, SE3, N1, N2, N3, $\overline{\text{BRAKE}}$, CBRAKE, RBK, OUTD	0 to 15V
PH1, PH2, PH3	-2 to 15V
VCOTACH, $\overline{\text{DISPWR}}$, PWMIN, ADVANCE,RESET, $\overline{\text{ENABLE}}$, $\overline{\text{RETRACT}}$	0 to VCC
All other pins	0 to VP
Storage Temperature	-45 to 165°C
Solder temperature - 10 sec duration	260°C

RECOMMENDED OPERATING CONDITIONS

Unless otherwise noted, the following conditions are valid throughout this document.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
VP	Normal Mode	9	12	13.2	V
	Retract Mode	3.5		14	V
VCC		4.5		5.5	V
VREF		4.5		7	V
Operating Temperature		0		70	°C

DC CHARACTERISTICS

VP Current			20	35	mA
VCC Current			5	10	mA
VREF Current	SE2 = VREF			2	mA

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A1, LOOP COMPENSATION AMPLIFIER

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Input bias current				500	nA
Input offset voltage				3	mV
Voltage swing	About VREF = 5.4	±2			V
Common mode range					
V_{IL}				1	V
V_{IH}, wrt VP		-1.3			V
Load resistance	to VREF	4			kΩ
Load capacitance				100	pF
Gain		80			dB
Unity gain bandwidth		0.5			MHz
CMRR		60			dB
PSRR		60			dB

A2, CURRENT SENSE AMPLIFIER

Input Impedance - SE1	SE2 = VREF	1.8	3.3		kΩ
Input Impedance - SE2	SE1 = VREF	4.8	9.6		kΩ
Input offset voltage	SE1 = SE2 = VREF			2	mV
Output voltage swing					
V_{OL}				1.4	V
V_{OH}, wrt VP		-1.3			V
Common mode range					
V_{IL}				0	V
V_{IH}, wrt VP	VP ≥ 10V, VREF = 5	-0.2			V
Load Resistance	to VREF	20			kΩ
Load capacitance				100	pF
Output impedance				20	Ω
Gain (SOUT-VREF)/SE1-SE2)		3.9	4	4.1	V/V
Unity gain bandwidth		0.5			MHz
CMRR		52			dB
PSRR		60			dB

ELECTRICAL SPECIFICATIONS (continued)

A3 AMPLIFIER

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Input bias current				250	nA
Input offset voltage				2	mV
Voltage swing					
V_{OL}				1.4	V
V_{OH}, wrt VP		-1.2			V
Common mode range					
V_{IL}				2.5	V
V_{IH}, wrt VP		-3			V
Load resistance	to VREF	10			kΩ
Load capacitance				100	pF
Gain		60			dB
Unity gain bandwidth		150			kHz
CMRR		60			dB
PSRR		60			dB

WINDOW COMPARATOR

Window comparator threshold	|SOUT-VREF| increasing		VREF-VLIM		V
Threshold hysteresis			50		mV
VLIM voltage	No external parts	92	94	96	%VREF
VLIM input resistance		8	15		kΩ
$\overline{\text{WRPROT}}$ Vol	Iol < 1 mA			0.4	V
$\overline{\text{WRPROT}}$ input leakage				10	µA
$\overline{\text{WRPROT}}$ delay	SOUT = VREF to VREF + 0.6V			10	µs

VREF MONITOR

VREF fail threshold	VREF Descending	2.6	3.3	4	V
Hysteresis			85		mV

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ACTUATOR MOSFET DRIVERS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
SE3 Input impedance	to VREF	10	25		kΩ
OUTA, OUTC voltage swing	|IOUT| < 1 mA	0.7		VCC-1	V
OUTB, OUTD voltage swing	|IOUT| < 1 mA	1		VCC-1	V
VTH, crossover separation threshold				2	V
Slew rate, OUTA..D	CL < 1000 pF	0.5			V/µs
Crossover time	300 mV step at ERR			6	µs
Output impedance, OUTA..D			50		kΩ
Transconductance I(OUTA..D)/(ERR-VREF)			8		mA/V
Gain -(SE1-VREF)/(ERR-VREF) or (SE3-VREF)/(ERR-VREF)		8	8.5	9	V/V
Retract motor voltage	VP > 5V	0.7	0.82	1	V

VCO (unless otherwise specified, CVCO = 0.01 µF, RVCO = 12 kΩ)

Typical frequency		$\frac{V_{RC}}{8.8\ R_{VCO}\ C_{VCO}}$			Hz
Run Frequency	RC = 2V	1705	1950	2150	Hz
Idle Frequency	Mode = Preset	90	108	125	Hz
Reset Phase Error	RC = V_{IDLE}			36	Degree

PHASE ERROR AMPLIFIER (unless otherwise specified, RVCO=12 kΩ, RPH=not used)

VRC (VIDLE)	Mode = Preset		100		mV
Pump Current at RC					
Start Mode	$V_{RC} = V_{IDLE}$, RPH = ∞		4		µA
Run Mode, at speed	V_{RC} = 2V		80		µA
Source/Sink Current Mismatch	V_{RC} = 2V			5	%
PH1 Input Offset, State B	PH2 = VP, PH3 = 0	-60		60	mV
PH1 Input Offset, State E	PH2 = 0, PH3 = VP	-60		60	mV
PH2 Input Offset, State A	PH1 = VP, PH3 = 0	-60		60	mV
PH2 Input Offset, State D	PH1 = 0, PH3 = VP	-60		60	mV
PH3 Input Offset, State F	PH1 = VP, PH2 = 0	-60		60	mV
PH3 Input Offset, State C	PH1 = 0, PH2 = VP	-60		60	mV
RPH Voltage	RPH = 120 kΩ		1.2		V

ELECTRICAL SPECIFICATIONS (continued)

MOTOR CURRENT CONTROL

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
ISENSE threshold (VLIMIT)		90	100	110	mV
One shot off time	COS = 0.002 µF	15	25	35	µs

BRAKING CIRCUIT

$\overline{\text{BRAKE}}$ threshold	Ta = 25°C, VP = 4V	0.8	1.2	1.6	V
$\overline{\text{BRAKE}}$ VP threshold	$\overline{\text{BRAKE}}$ = 1.6V, Ta = 25°C			3.8	V
$\overline{\text{BRAKE}}$ VP threshold temperature coefficient			-7.2		mV/°C
$\overline{\text{BRAKE}}$ bias current				0.1	µA

NMOS MOTOR DRIVER OUTPUTS (N1, N2, N3)

Source Current	RSC = 50k, VOUT = 4V	3		6	mA
	RSC = 100k, VOUT = 4V	2		4	mA
Sink Current	VOUT = 4V	9		25	mA
Output Low Voltage	Isink = 5 mA			1	V
Output High Voltage (wrt VP)	Isource = 0.1 mA	-2.5			V

PMOS MOTOR DRIVER OUTPUTS (P1, P2, P3)

Source Current	VOUT = VP-4	20			mA
Sink Current	VOUT = VP-4	9		25	mA
Output Low Voltage	Isink = 1 mA			1.5	V
Output High Voltage (wrt VP)	Isource_P = 5 mA, V_N = 6V	-1			V

DIGITAL INPUTS;

V_{IL}		0.8			V
V_{IH}				2	V
I_{IH}	V_{IN} = 4V			200	µA
Open circuit voltage				0.4	V

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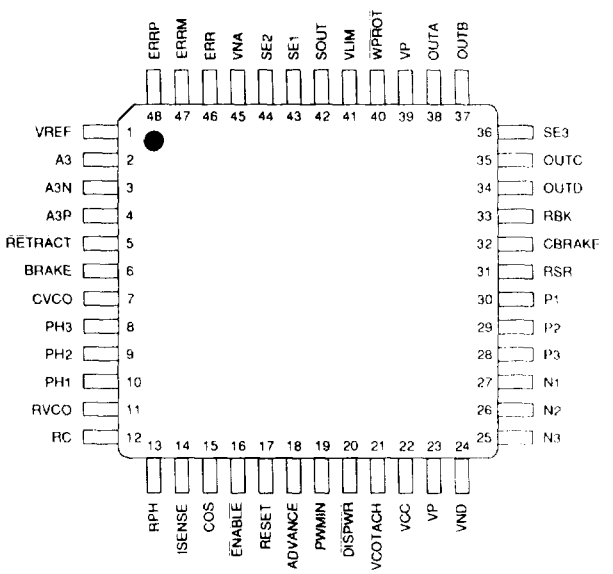
PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



48-Lead TQFP

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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