

Document Title

128Kx36-Bit Synchronous Pipelined Burst SRAM

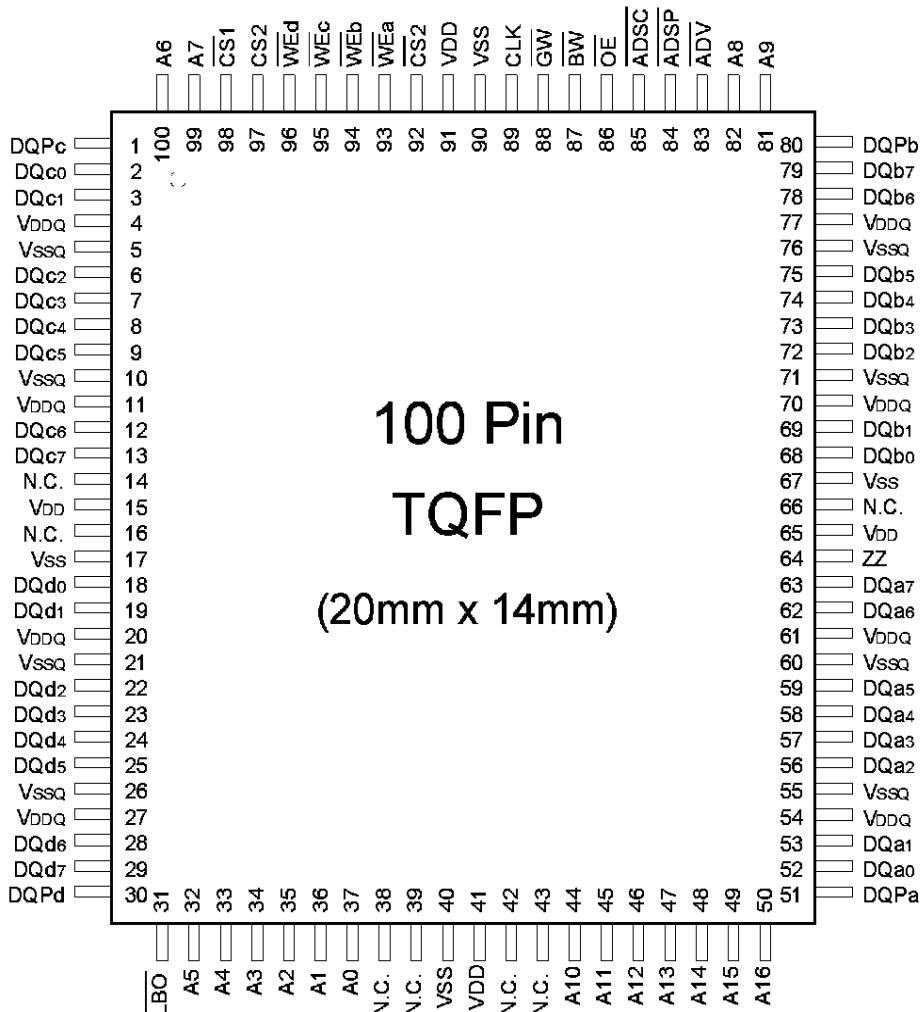
Revision History

<u>Rev. No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0.0	Initial draft	December. 15. 1997	Preliminary
0.1	Change speed symbol 6.0/6.7/7.5/8.5 to 60/67/75/85, Change 7.5 bin to 7.2	February. 02. 1998	Preliminary
0.2	Change speed bin from 60/67/75/85 to 72/85/10.	February. 06. 1998	Preliminary
0.3	Change DC characteristics $V_{DD}$ condition from $3.3V \pm 5\%$ to $3.3V + 10\% / -5\%$ Change Input/output leakage current for $\pm 1\mu A$ to $\pm 2\mu A$ , Insert Note 4 at AC timing characteristics. Modify read timing & Power down cycle timing. Change $I_{S2}$ value from 10mA to 20mA. Remove Low power version.	February. 12. 1998	Preliminary
0.4	Change Undershoot spec from $-3.0V$ (pulse width $\leq 20ns$ ) to $-2.0V$ (pulse width $\leq t_{CYC}/2$ ) Add Overshoot spec $4.6V$ ((pulse width $\leq t_{CYC}/2$ ) Change $V_{IN}$ max from 5.5V to $V_{DD} + 0.5V$	April. 14. 1998	Preliminary
0.5	Change $I_{S2}$ value from 20mA to 30mA. Change $V_{DD}$ condition from $V_{DD} = 3.3V + 10\% / -5\%$ to $V_{DD} = 3.3V + 0.3V / -0.165V$ .	May. 13. 1998	Preliminary
0.6	Modify DC characteristics( Input Leakage Current test Conditions) form $V_{DD} = V_{SS}$ to $V_{DD}$ to Max.	May. 14. 1998	Preliminary
1.0	Final spec Release	May. 15. 1998	Final

The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any questions, please contact the SAMSUNG branch office near your office, call or contact Headquarters.



PIN CONFIGURATION(TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A17	Address Inputs	32,33,34,35,36,37,44,45,46,47,48,49,50,81,82,99,100	VDD	Power Supply(+3.3V)	15,41,65,91
			VSS	Ground	17,40,67,90
			N.C.	No Connect	14,16,38,39,42,43,66
ADV	Burst Address Advance	83	DQa0~a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
ADSP	Address Status Processor	84	DQb0~b7		68,69,72,73,74,75,78,79
ADSC	Address Status Controller	85	DQc0~c7		2,3,6,7,8,9,12,13
CLK	Clock	89	DQd0~d7		18,19,22,23,24,25,28,29
CS1	Chip Select	98	DQPa~Pd		51,80,1,30
CS2	Chip Select	97	VDDQ	Output Power Supply (+3.3V)	4,11,20,27,54,61,70,77
CS2	Chip Select	92	VSSQ	Output Ground	5,10,21,26,55,60,71,76
WEx	Byte Write Inputs	93,94,95,96			
OE	Output Enable	86			
GW	Global Write Enable	88			
BW	Byte Write Enable	87			
ZZ	Power Down Input	64			
LBO	Burst Mode Control	31			

**FUNCTION DESCRIPTION**

The KM736V790 is a synchronous SRAM designed to support the burst address accessing sequence of the P6 and Power PC based microprocessor. All inputs (with the exception of OE, LBO and ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by ADSC, ADSP and ADV and chip select pins.

The accesses are enabled with the chip select signals and output enabled signals. Wait states are inserted into the access with ADV.

When ZZ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2cycles of wake up time. ZZ pin is pulled down internally.

Read cycles are initiated with ADSP (regardless of WEx and ADSC) using the new external address clocked into the on-chip address register whenever ADSP is sampled low, the chip selects are sampled active, and the output buffer is enabled with OE. In read operation the data of cell array accessed by the current address, registered in the Data-out registers by the positive edge of CLK, are carried to the Data-out buffer by the next positive edge of CLK. The data, registered in the Data-out buffer, are projected to the output pins. ADV is ignored on the clock edge that samples ADSP asserted, but is sampled on the subsequent clock edges. The address increases internally for the next access of the burst when WEx are sampled High and ADV is sampled low. And ADSP is blocked to control signals by disabling CS1.

All byte write is done by GW (regardless of BW and WEx), and each byte write is performed by the combination of BW and WEx when GW is high.

Write cycles are performed by disabling the output buffers with OE and asserting WEx. WEx are ignored on the clock edge that samples ADSP low, but are sampled on the subsequent clock edges. The output buffers are disabled when WEx are sampled Low (regardless of OE). Data is clocked into the data input register when WEx sampled Low. The address increases internally to the next address of burst, if both WEx and ADV are sampled Low. Individual byte write cycles are performed by any one or more byte write enable signals (WEa, WEb, WEc or WEd) sampled low. The WEa control DQa0 ~ DQa7 and DQPa, WEb controls DQb0 ~ DQb7 and DQPb, WEc controls DQc0 ~ DQc7 and DQ Pc, and WEd control DQd0 ~ DQd7 and DQPd. Read or write cycle may also be initiated with ADSC, instead of ADSP. The differences between cycles initiated with ADSC and ADSP as are follows;

ADSP must be sampled high when ADSC is sampled low to initiate a cycle with ADSC.  
WEx are sampled on the same clock edge that sampled ADSC low (and ADSP high).

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the LBO pin. When this pin is Low, linear burst sequence is selected. When this pin is High, Interleaved burst sequence is selected.

**BURST SEQUENCE TABLE**

(Interleaved Burst)

LBO PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
	First Address	0	0	0	1	1	0	1	1
	↓	0	1	0	0	1	1	1	0
	↓	1	0	1	1	0	0	0	1
	Fourth Address	1	1	1	0	0	1	0	0

(Linear Burst)

LBO PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
	First Address	0	0	0	1	1	0	1	1
	↓	0	1	1	0	1	1	0	0
	↓	1	0	1	1	0	0	0	1
	Fourth Address	1	1	0	0	0	1	1	0

NOTE : 1. LBO pin must be tied to High or Low, and Floating State must not be allowed.

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

CS1	CS2	CS2	ADSP	ADSC	ADV	WRITE	CLK	Address Accessed	Operation
H	X	X	X	L	X	X	↑	N/A	Not Selected
L	L	X	L	X	X	X	↑	N/A	Not Selected
L	X	H	L	X	X	X	↑	N/A	Not Selected
L	L	X	X	L	X	X	↑	N/A	Not Selected
L	X	H	X	L	X	X	↑	N/A	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle

- NOTE : 1. X means "Don't Care".      2. The rising edge of clock is symbolized by ↑.  
 3.  $\overline{\text{WRITE}} = \text{L}$  means Write operation in WRITE TRUTH TABLE.  
 $\overline{\text{WRITE}} = \text{H}$  means Read operation in WRITE TRUTH TABLE.  
 4. Operation finally depends on status of asynchronous input pins(ZZ and  $\overline{\text{OE}}$ ).

WRITE TRUTH TABLE

GW	BW	WEa	WEb	WEc	WEd	Operation
H	H	X	X	X	X	READ
H	L	H	H	H	H	READ
H	L	L	H	H	H	WRITE BYTE a
H	L	H	L	H	H	WRITE BYTE b
H	L	H	H	L	L	WRITE BYTE c and d
H	L	L	L	L	L	WRITE ALL BYTES
L	X	X	X	X	X	WRITE ALL BYTES

- NOTE : 1. X means "Don't Care".  
 2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

ASYNCHRONOUS TRUTH TABLE

(See Notes 1 and 2):

Operation	ZZ	$\overline{\text{OE}}$	I/O Status
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

NOTE

1. X means "Don't Care".
2. ZZ pin is pulled down internally
3. For write cycles that following read cycles, the output buffers must be disabled with  $\overline{\text{OE}}$ , otherwise data bus contention will occur.
4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
5. Deselected means power down state of which stand-by current depends on cycle time.

PASS-THROUGH TRUTH TABLE

Previous Cycle		Present Cycle				Next Cycle
Operation	WRITE	Operation	CS <sub>i</sub>	WRITE	OE	
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	Initiate Read Cycle Address=An Data=Qn-1 for all bytes	L	H	L	Read Cycle Data=Qn
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=Qn-1 for all bytes	H	H	L	No carryover from previous cycle
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=High-Z	H	H	H	No carryover from previous cycle
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	Initiate Read Cycle Address=An Data=Qn-1 for one byte	L	H	L	Read Cycle Data=Qn
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	No new cycle Data=Qn-1 for one byte	H	H	L	No carryover from previous cycle

NOTE : 1. This operation makes written data immediately available at output during a read cycle preceded by a write cycle.

ABSOLUTE MAXIMUM RATINGS\*

Parameter	Symbol	Rating	Unit
Voltage on V <sub>DD</sub> Supply Relative to V <sub>SS</sub>	V <sub>DD</sub>	-0.3 to 4.6	V
Voltage on V <sub>DDQ</sub> Supply Relative to V <sub>SS</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V
Voltage on Input Pin Relative to V <sub>SS</sub>	V <sub>IN</sub>	-0.3 to 6.0	V
Voltage on I/O Pin Relative to V <sub>SS</sub>	V <sub>IO</sub>	-0.3 to V <sub>DDQ</sub> +0.5	V
Power Dissipation	P <sub>D</sub>	1.6	W
Storage Temperature	T <sub>STG</sub>	-65 to 150	°C
Operating Temperature	T <sub>OPR</sub>	0 to 70	°C
Storage Temperature Range Under Bias	T <sub>BIAS</sub>	-10 to 85	°C

\*NOTE : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS (0°C ≤ TA ≤ 70°C)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V <sub>DD</sub>	3.135	3.3	3.6	V
	V <sub>DDQ</sub>	3.135	3.3	3.6	V
Ground	V <sub>SS</sub>	0	0	0	V

CAPACITANCE\*(TA=25°C, f=1MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0V	-	5	pF
Output Capacitance	C <sub>OUT</sub>	V <sub>OUT</sub> =0V	-	7	pF

\*NOTE : Sampled not 100% tested.

DC ELECTRICAL CHARACTERISTICS(TA=0 to 70°C, VDD=3.3V+0.3V/-0.165V)

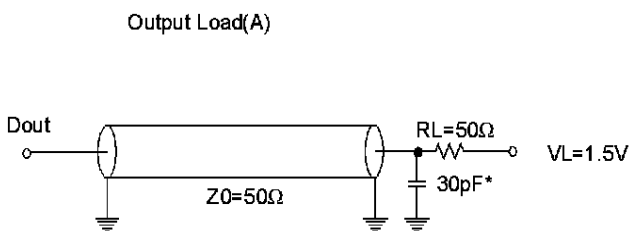
Parameter	Symbol	Test Conditions	Min	Max	Unit	
Input Leakage Current(except ZZ)	IIL	VDD = Max ; VIN=VSS to VDD	-2	+2	µA	
Output Leakage Current	IoL	Output Disabled, VOUT=VSS to VDDQ	-2	+2	µA	
Operating Current	Icc	Device Selected, IOUT=0mA, ZZ≤VIL, All Inputs=VIL or VIH Cycle Time ≥ tCYC Min	-72	-	350	mA
			-85	-	320	
			-10	-	300	
Standby Current	Iss	Device deselected, IOUT=0mA, ZZ≤VIL, f=Max, All Inputs≤0.2V or ≥ VDD-0.2V	-72	-	80	mA
			-85	-	70	
			-10	-	60	
	Iss1	Device deselected, IOUT=0mA, ZZ≤0.2V, f= 0, All Inputs= fixed (VDD-0.2V or 0.2V)	-	-	30	mA
Iss2	Device deselected, IOUT=0mA, ZZ≥VDD-0.2V, f=Max, All Inputs≤VIL or ≥VIH	-	-	30	mA	
Output Low Voltage	VoL	IoL=8.0mA	-	0.4	V	
Output High Voltage	VoH	IoH=-4.0mA	2.4	-	V	
Input Low Voltage	VIL		-0.5*	0.8	V	
Input High Voltage	VIH		2.0	VDD+0.5**	V	

- \* VIL(Min)=-2.0(Pulse Width ≤ tCYC/2)
- \*\* VIH(Max)=4.6(Pulse Width ≤ tCYC/2)
- \*\* In Case of I/O Pins, the Max. VIH=VDDQ+0.5V

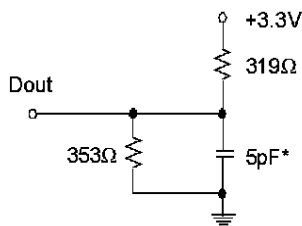
TEST CONDITIONS

(TA=0 to 70°C, VDD=3.3V+0.3V/-0.165V, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time(Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1



Output Load(B),(3.3V I/O)  
(for tLZC, tLZOE, tHZOE & tHZC)



\* Capacitive Load consists of all components of the test environment.

\* Including Scope and Jig Capacitance

Fig. 1

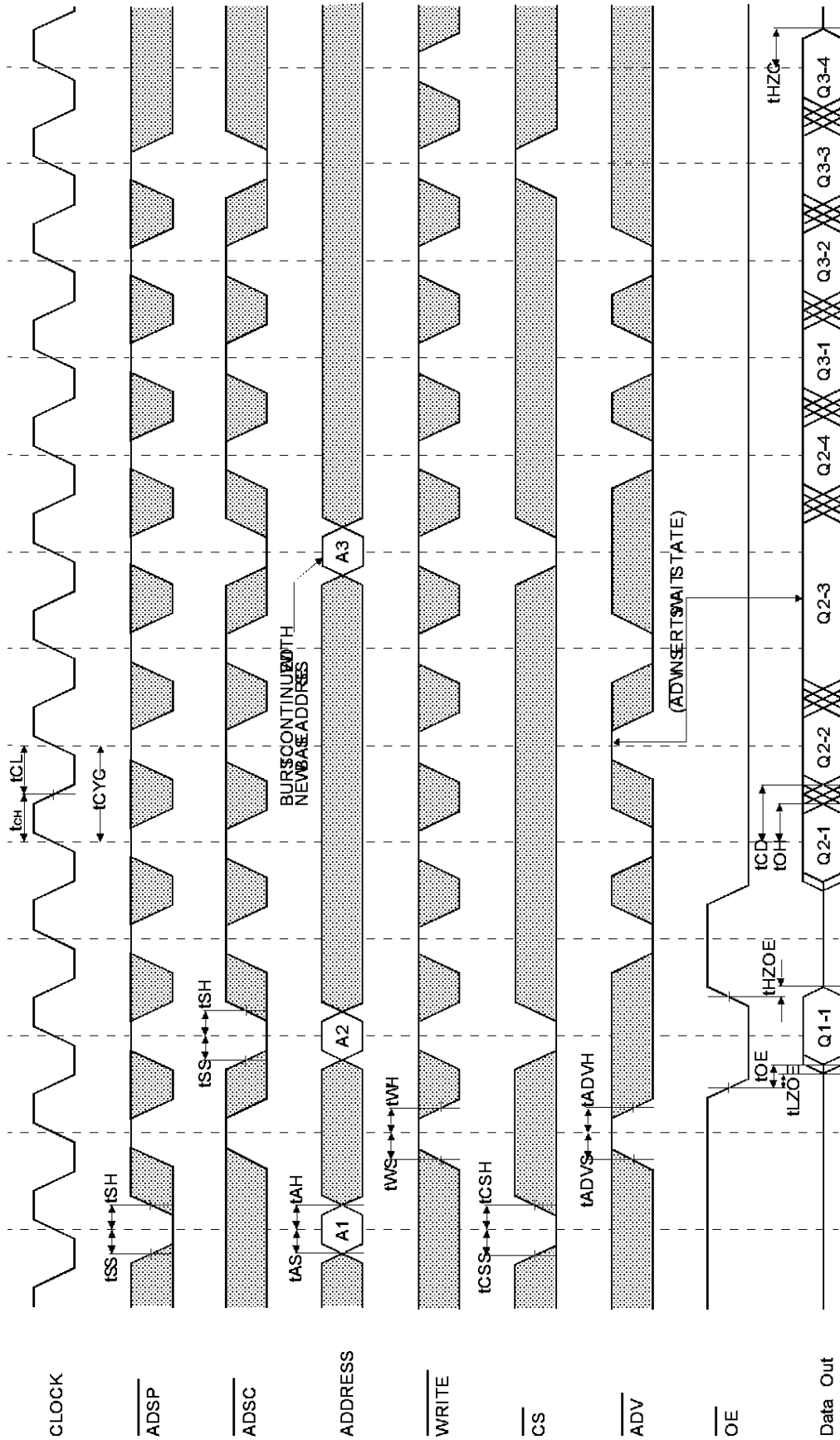
## AC TIMING CHARACTERISTICS

(V<sub>DD</sub>=3.3V±0.3V/-0.165V, T<sub>A</sub>=0 to 70°C)

Parameter	Symbol	-72		-85		-10		Unit
		Min	Max	Min	Max	Min	Max	
Cycle Time	t <sub>CYC</sub>	7.2	-	8.5	-	10	-	ns
Clock Access Time	t <sub>CD</sub>	-	4.5	-	5.0	-	5.0	ns
Output Enable to Data Valid	t <sub>OE</sub>	-	4.5	-	5.0	-	5.0	ns
Clock High to Output Low-Z	t <sub>LZC</sub>	0	-	0	-	0	-	ns
Output Hold from Clock High	t <sub>OH</sub>	1.5	-	1.5	-	1.5	-	ns
Output Enable Low to Output Low-Z	t <sub>LZOE</sub>	0	-	0	-	0	-	ns
Output Enable High to Output High-Z	t <sub>HZOE</sub>	-	4.0	-	4.0	-	4.0	ns
Clock High to Output High-Z	t <sub>HZC</sub>	1.5	5.0	1.5	5.0	1.5	5.0	ns
Clock High Pulse Width	t <sub>CH</sub>	3.0	-	3.5	-	4.0	-	ns
Clock Low Pulse Width	t <sub>CL</sub>	3.0	-	3.5	-	4.0	-	ns
Address Setup to Clock High	t <sub>AS</sub>	2.0	-	2.0	-	2.0	-	ns
Address Status Setup to Clock High	t <sub>SS</sub>	2.0	-	2.0	-	2.0	-	ns
Data Setup to Clock High	t <sub>DS</sub>	2.0	-	2.0	-	2.0	-	ns
Write Setup to Clock High (GW, BW, WEx)	t <sub>WS</sub>	2.0	-	2.0	-	2.0	-	ns
Address Advance Setup to Clock High	t <sub>ADVS</sub>	2.0	-	2.0	-	2.0	-	ns
Chip Select Setup to Clock High	t <sub>CSS</sub>	2.0	-	2.0	-	2.0	-	ns
Address Hold from Clock High	t <sub>AH</sub>	0.5	-	0.5	-	0.5	-	ns
Address Status Hold from Clock High	t <sub>SH</sub>	0.5	-	0.5	-	0.5	-	ns
Data Hold from Clock High	t <sub>DH</sub>	0.5	-	0.5	-	0.5	-	ns
Write Hold from Clock High (GW, BW, WEx)	t <sub>WH</sub>	0.5	-	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	t <sub>ADVH</sub>	0.5	-	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	t <sub>CSH</sub>	0.5	-	0.5	-	0.5	-	ns
ZZ High to Power Down	t <sub>PDS</sub>	2	-	2	-	2	-	cycle
ZZ Low to Power Up	t <sub>PUS</sub>	2	-	2	-	2	-	cycle

- NOTE :**
1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever ADSC and/or ADSP is sampled low and CS is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
  2. Both chip selects must be active whenever ADSC or ADSP is sampled low in order for the this device to remain enabled.
  3. ADSC or ADSP must not be asserted for at least 2 Clock after leaving ZZ state.
  4. At any given voltage and temperature, t<sub>hzc</sub> is less than t<sub>lzc</sub>.

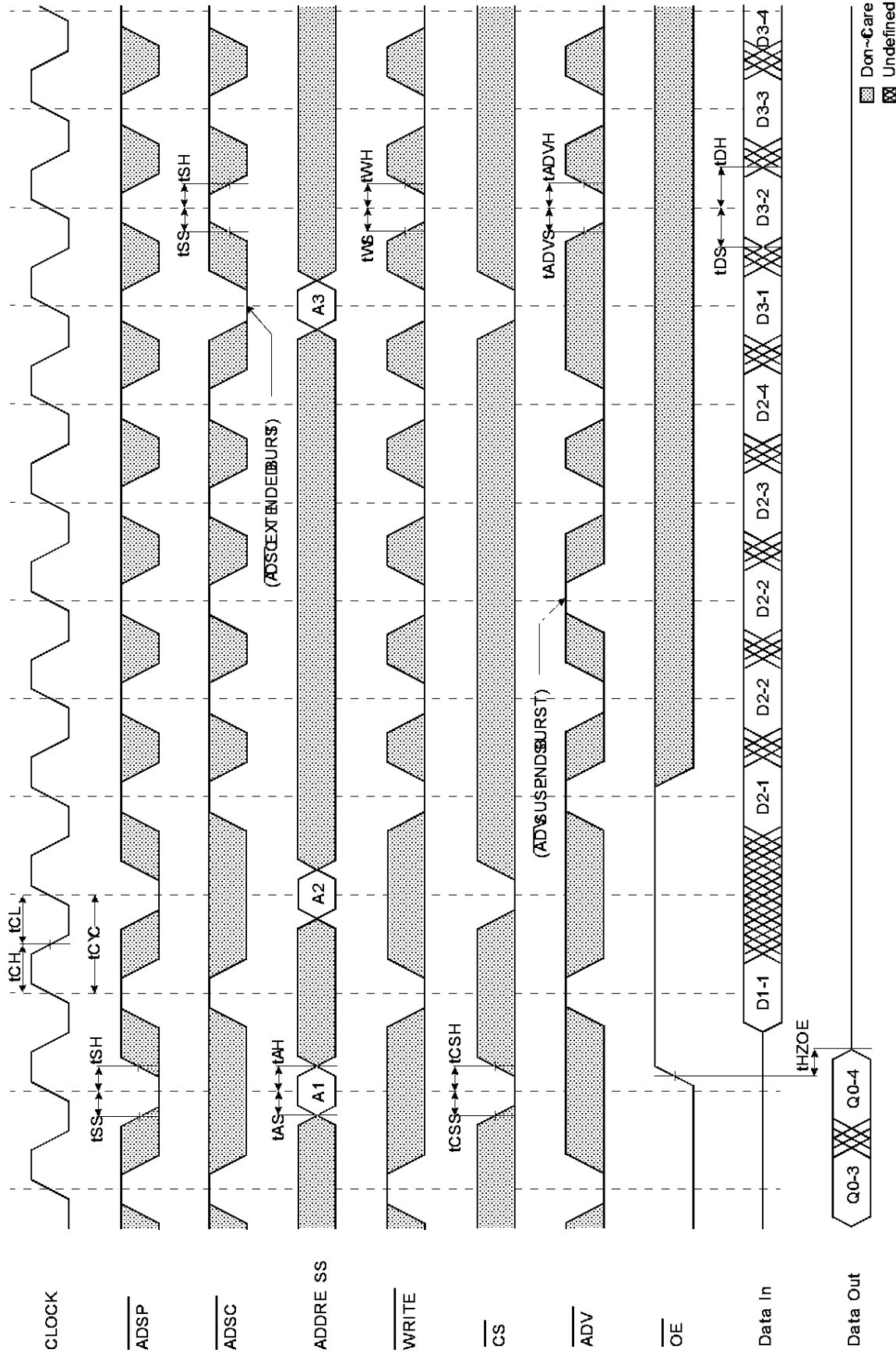
TIMING A FORM OF READ CYCLE



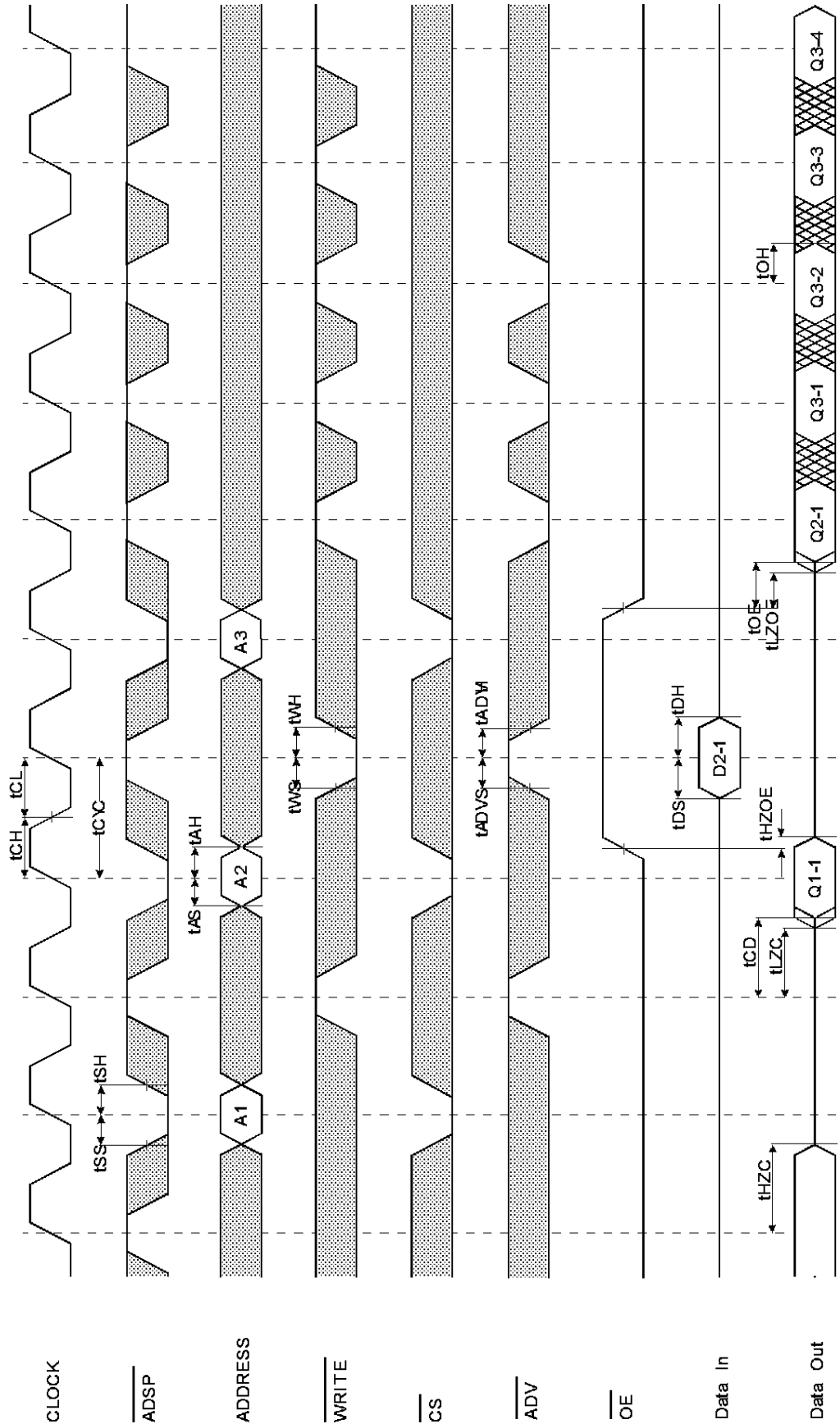
Don-Care  
 Undefined

NOTES WRITE=L means  $\overline{GM}=L$ , or  $\overline{GM}=H$ ,  $\overline{BW}=L$ ,  $\overline{WE}=L$   
 CS=L means  $\overline{CS}=L$ , CS = H and  $\overline{CS2}=L$   
 CS=H means  $\overline{CS}=H$ , or  $\overline{CS}=L$  and  $\overline{CS}=H$ , or  $\overline{CS}=L$ , and  $\overline{CS}=L$

TIMING A EFORM OF RTE CYCLE

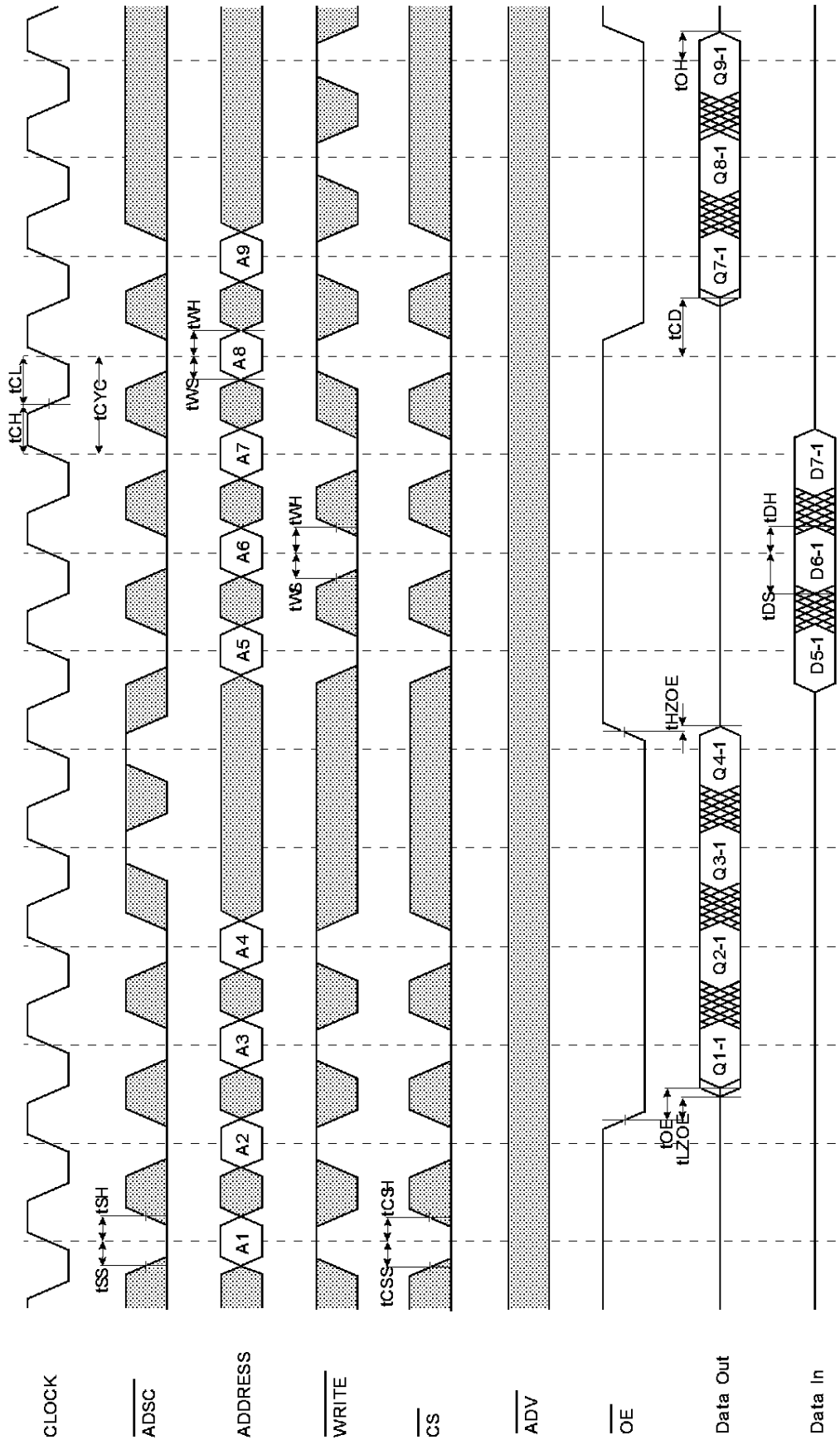


TIMING A EFORM OF COMBINATION READ RTE CYCLE ADSP CONTROLLED ADSC HIGH



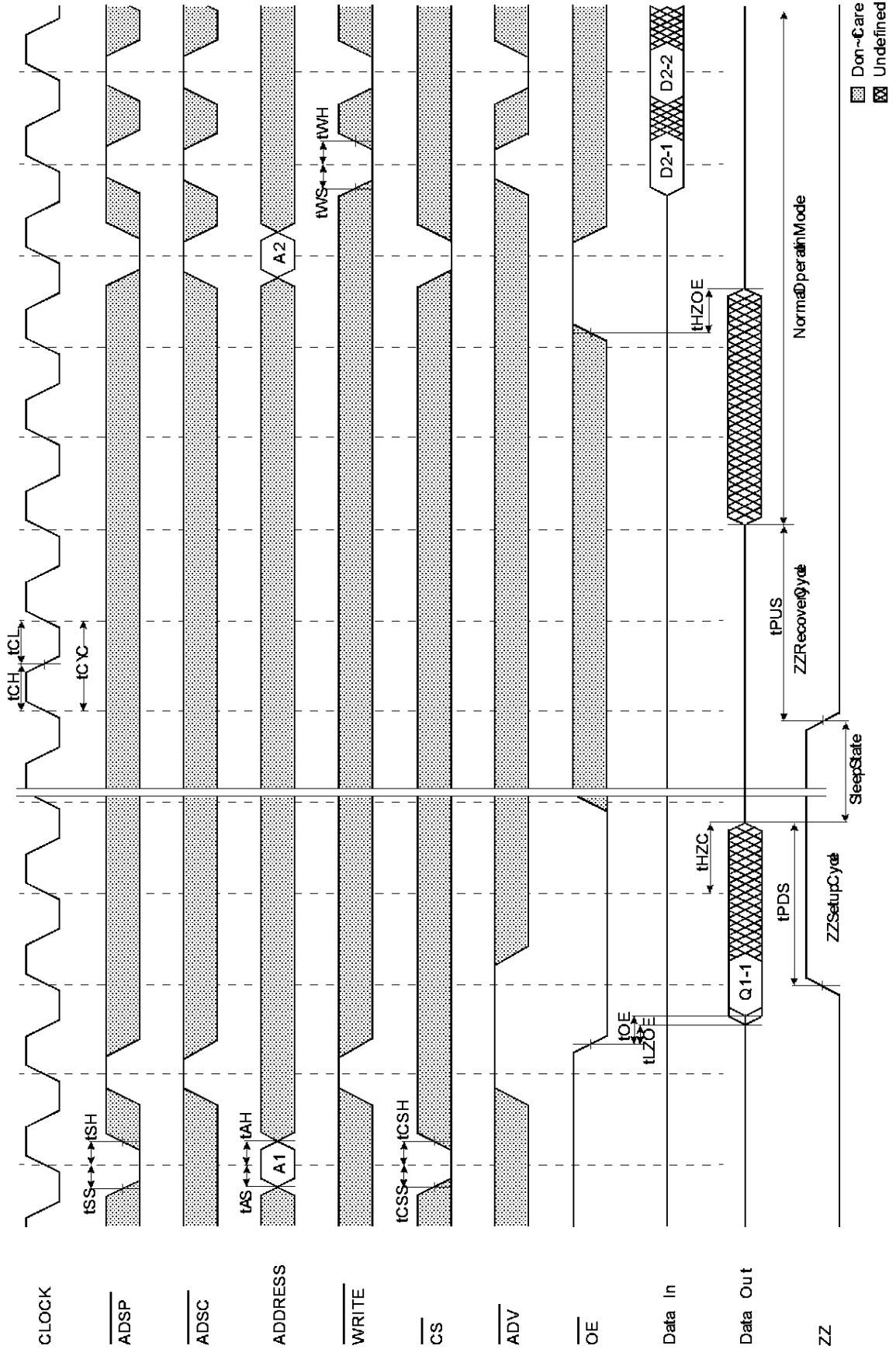
Don-Care  
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TIMING A EFORM OF SINGLE READ RITE CYCLE ADSC CONTROLLED ADSP HIGH



Don't-Care  
 Undefined

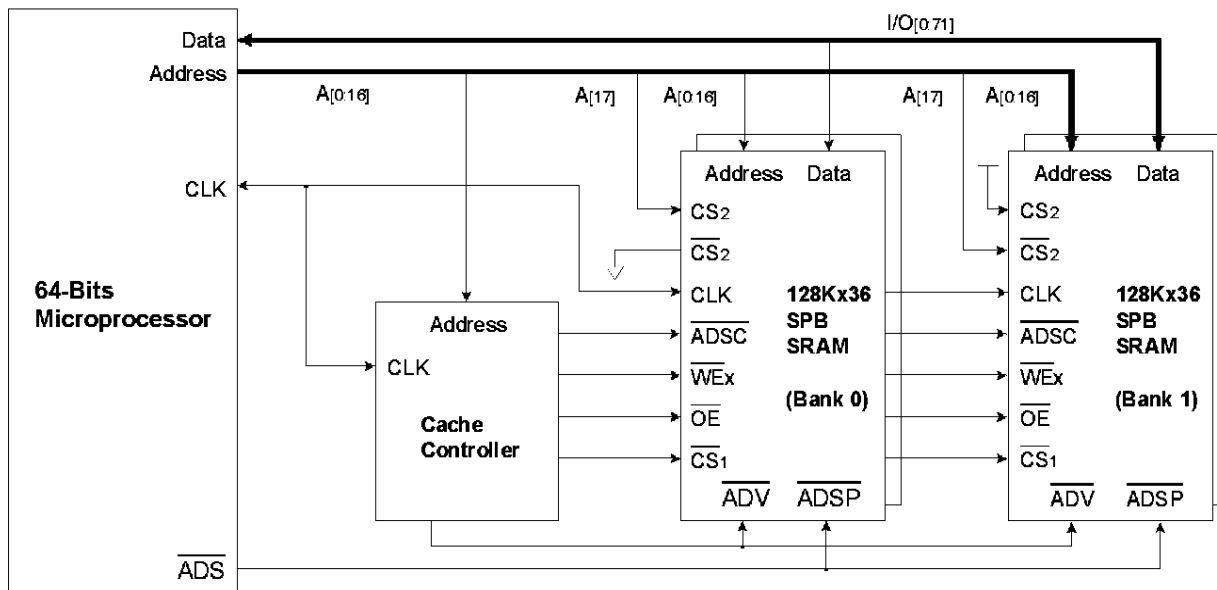
TIMING A FORM OF POWER DOWN CYCLE



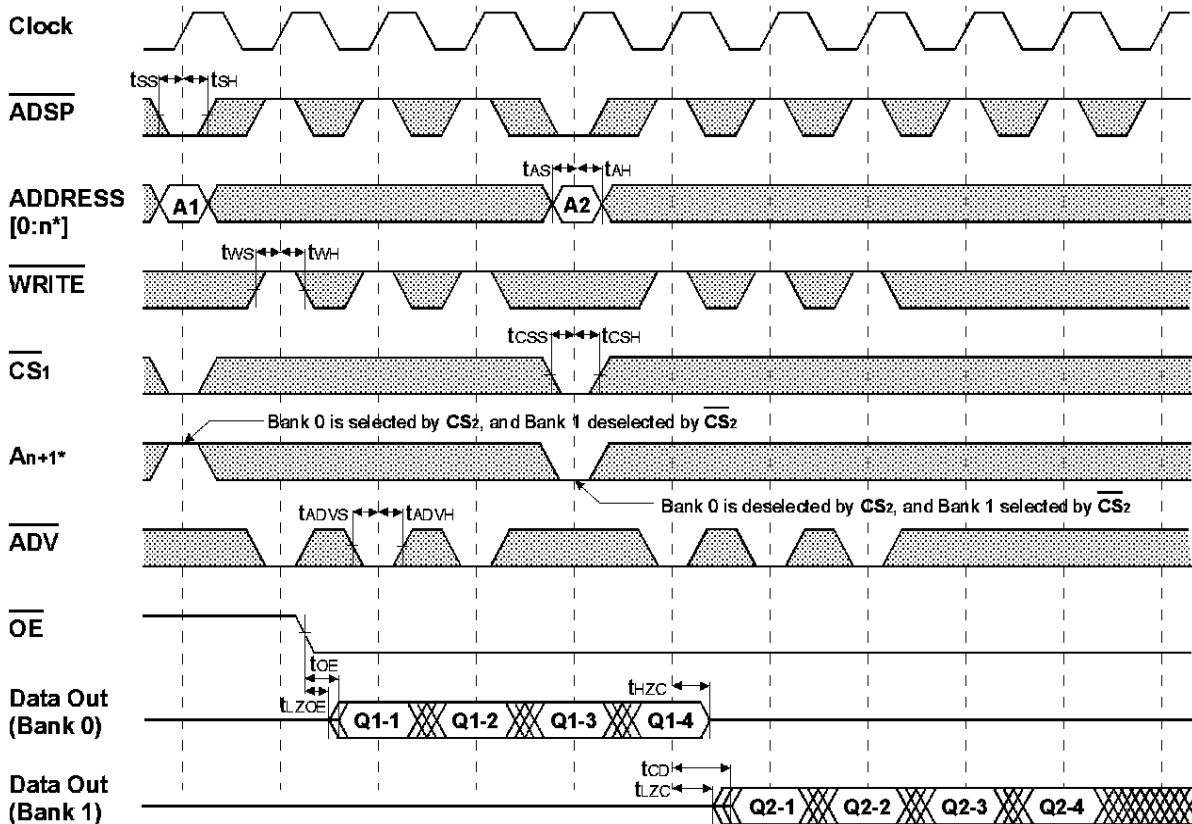
APPLICATION INFORMATION

DEPTH EXPANSION

The Samsung 128Kx36 Synchronous Pipelined Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 128K depth to 256K depth without extra logic.



INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)  
(ADSP CONTROLLED, ADSC=HIGH)



\*NOTES n = 14 32K depth, 15 64K depth, 16 128K depth, 17 256K depth

□ Don't Care    ⊗ Undefined

PACKAGE DIMENSIONS

100-TQFP-1420A

Units: millimeters/inches

