VTC Inc.
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VM65014

ANALOG PRML CHANNEL DETECTOR

960801

PRELIMINARY

August,1996

FEATURES

- Register programmable user data rates from 46 to 140 Mbps
- Sampled data read channel with maximum likelihood Viterbi detection
- Programmable continuous-time filter with two independently-variable real zeros
- Programmable seven tap transversal filter for PR4 equalization
- Programmable two level write precompensation with 1.25% resolution
- Direct Write/Read feature for equalizer optimization
- Analog/sampled AGC
- Zero phase restart for fast acquisition
- Servo area detectors for burst demodulation
- Fast timing control during acquisition by bypassing FIR filter
- Register programmable power management (<5 mW Power Down mode)
- Serial interface port for access to internal program storage registers to load and verify
- Single power supply (5V ±10%)
- Small footprint 64-pin PQFP package

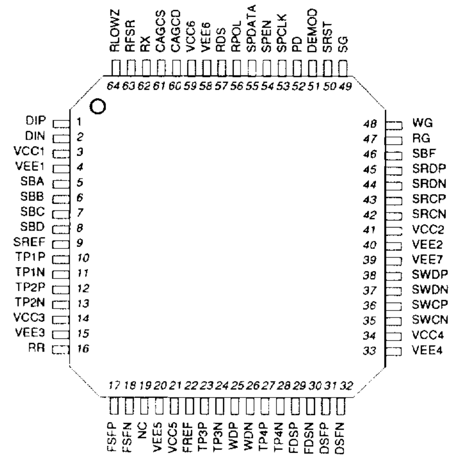
DESCRIPTION

The VM65014 is a high performance BiCMOS read channel IC that provides all of the data processing needed to implement the front end of a Partial Response Maximum Likelihood (PRML) read channel for zoned recording MR hard disk drive systems with user data rates from 46 to 140 Mbps.

BiCMOS process technology along with advanced circuit design techniques result in high performance devices with low power consumption. The part requires a single +5V power supply and is available in a 64-Lead PQFP package. This chip along with its companion, the VM65020, provides a complete channel solution.

Functional blocks include AGC, programmable continuous time filter, adaptive FIR filter, maximum likelihood Viterbi detector, frequency synthesizer, 2-level nonlinear write precomp and area detectors for servo bursts. Programmable functions such as data rate, filter cutoff/boost, FIR tap weights or adaption parameters, write precomp values, etc. are controlled by writing to the serial port registers. No external component changes are required to change zones.

CONNECTION DIAGRAM



64-lead PQFP

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	
V_{CC}	-0.3V to +7V
Input Voltages	
Digital Input Voltage V_{IN}	-0.3V to (V_{CC} + 0.3)V
Analog Input Voltage V_{IN}	-0.3V to (V_{CC} + 0.3)V
Storage Temperature T_{stg}	-65°C to 150°C
Junction Temperature T_J	150°C
Thermal Impedance Characteristics, Θ_{JA}:	
64-Lead PQFP	43°C/W

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:	
V_{CC}	+5V ± 10%
Junction Temperature T_J	0°C to 125°C

BLOCK DIAGRAM DESCRIPTION

AUTOMATIC GAIN CONTROL:

- Dual mode AGC, analog during acquisition, sampled during read data
- Separate AGC level storage pins for data and servo
- Dual rate attack and decay charge pump for rapid AGC recovery
- Programmable, symmetric, charge pump currents during read data
- Charge pump currents track programmable data rate
- Low drift AGC hold circuitry
- Internal Low Z for write mode.
- Externally adjustable one-shot pulse width for LOWZ control
- AGC hold, fast recovery, and AGC input impedance control signals
- Wide bandwidth, precision full-wave rectifier

LOW PASS FILTER/EQUALIZER:

- Programmable, 7-pole, continuous time filter provides:
  - Channel filter and pulse slimming equalization for equalization to PR4
  - Programmable cutoff frequency from 7 to 48 MHz
  - Programmable boost/equalization of 0 to 13 dB
  - Programmable group delay of ±30%
  - Differentiator outputs match normal output phase
  - Minimized size and power

FIR FILTER/EQUALIZER:

- Seven tap filter
- Individual tap adjustment for fine equalization to PR4 target
- No external components required
- Independent and/or dependent self adaption of tap weights
- User programmable adaption parameters:
  - Integration time
  - Dead zone control
  - Tap starting points
  - Number of taps to adapt
  - Selection of which taps to independently adjust

LEVEL QUALIFICATION:

- Level pulse qualifier for servo and sync field reads
- Independent positive and negative thresholds for asymmetrical signals (e.g. from MR heads)
- Independent thresholds for servo

MAXIMUM LIKELIHOOD DETECTOR:

- Sampled Viterbi detection of signal equalized to PR4
- Programmable threshold window
- Survival register length of five

FREQUENCY SYNTHESIZER:

- Better than 1% frequency resolution
- Up to 160 MHz frequency output
- Independent M and N divide-by registers
- No active external components required

TIMING RECOVERY

- Single external capacitor required
- Register programmable to user data rate of 140 Mbps operation
- Fast Acquisition, sampled data phase lock loop
- Decision directed clock recovery from data samples
- Programmable damping ratio which is constant over all data rates

WRITE PRECOMPENSATION:

- Independently-programmable write precompensation for three data patterns
- Step resolution of 1.25% up to 40%
- Precompensation tracks Frequency Synthesizer period
- Differential PECL write data output
- Precoding function suited for PR4 channel

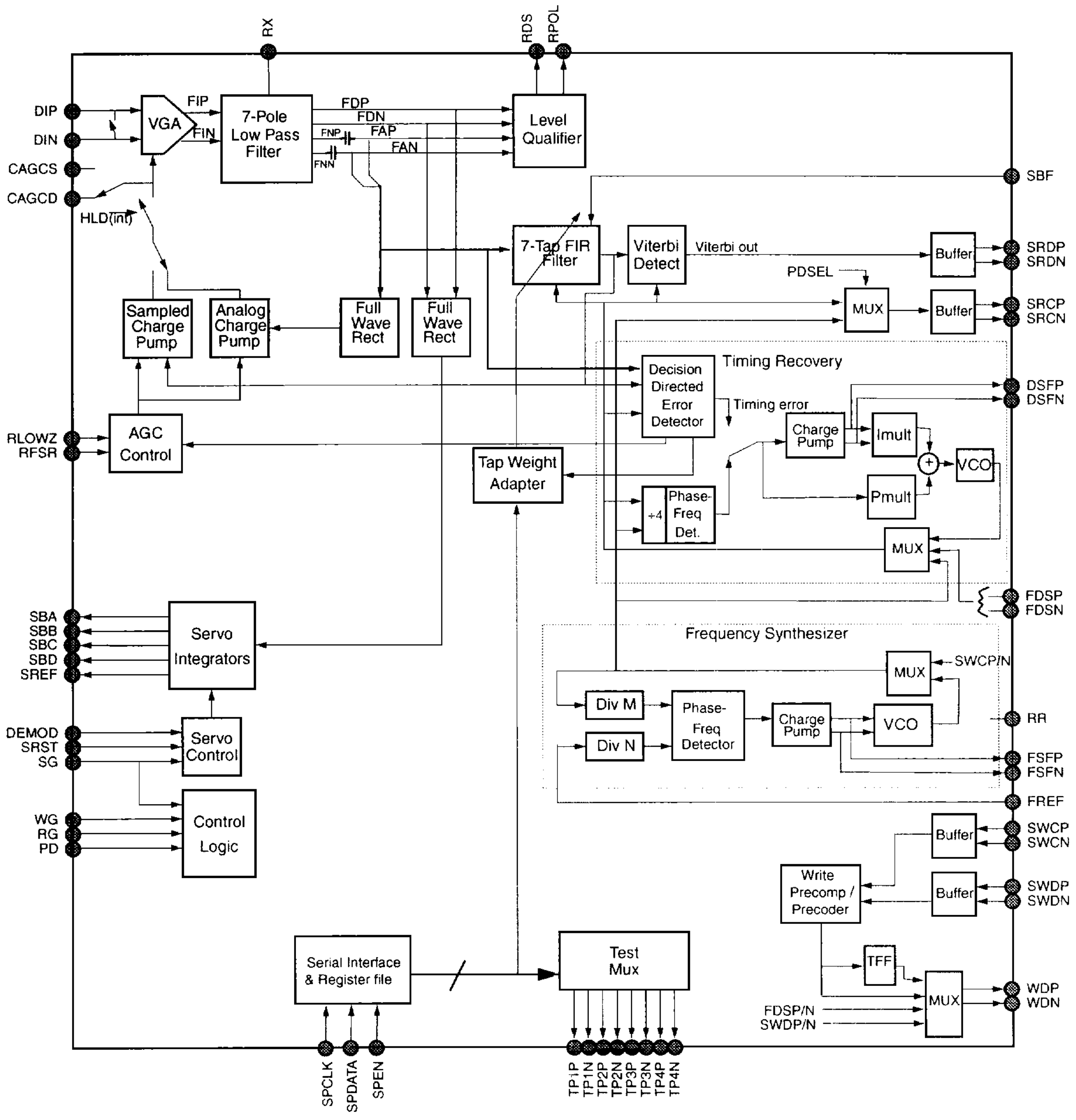
SERVO:

- Wide bandwidth, precision full-wave rectifier
- Separate, automatically-selected registers for servo f_c, boost, and group delay
- Individual area detectors for servo bursts A, B, C and D
- Programmable servo gain of ± 4 dB

PIN FUNCTIONS AND DESCRIPTION

Pin functions are described on 37.

BLOCK DIAGRAM



BLOCK-BY-BLOCK FUNCTIONAL DESCRIPTION

TheVM65014 along with the VM65020 implements a complete high performance PRML read channel. The VM65014 includes an AGC, programmable filter/equalizer, adaptive FIR filter, Viterbi detector, frequency synthesizer, decision-directed timing recovery, write precompensation and area detect servo, and supports user data rates up to 140 Mbps. A serial port is provided to read and write control data to the 16 internal programmable storage registers.

GAIN CONTROL (GC)

The Gain Control section of the VM65014 consists of a wideband variable gain amplifier (VGA) and a programmable continuous time filter, with a charge pump, amplitude detector, and exponentiator. The Gain Control has two modes: Automatic (AGC), and Programmable (PGC). The mode is selected with the PGC register bit.

Servo reads employ a fully differential analog AGC loop, while data reads employ both the analog loop (for fast acquisition) and a sampled/decision-directed loop (for fine tuning of the gain). The programmable gain control (PGC) circuit controls the VGA gain with an internal DAC. In PGC mode, the AGC loop is disabled and the VGA gain is a linear function of the DAC count.

The read signal is externally AC-coupled into the VGA amplifier on the DIP/DIN pins. The gain of the VGA is controlled by the voltage stored on the CAGCD hold capacitor for data reads (SG=0) and CAGCS for servo reads (SG=1). Two external holding capacitors allow for data and servo fields to have independent charge and discharge rates to avoid long reacquisitions of the gain at the beginning of the servo and data fields. The read signal is amplified and equalized by a low pass filter. The AGC loop locks the differential peak-to-peak voltage at FAP/FAN to $V_{FA} = 0.5V_{ppd}$ for inputs ranging from 20 to 200 mV_{ppd}. Test modes are provided in which the normal and differentiated filter outputs (FNP/FNN, FDP/FDN), the VGA inputs and outputs (DIP/DIN, DOP/DON), and the pulse qualifier inputs (FAP/FAN) are multiplexed to the TP2P/TP2N output pins respectively.

The analog AGC loop consists of the VGA amplifier, programmable continuous time filter, amplitude detector, exponentiator, and dual rate charge pump for fast transient recovery. Charge currents (decay) increase the capacitor voltage, V_{cagcx}, and increase the VGA gain while discharge currents (attack) lower the capacitor voltage, V_{cagcx}, and reduce the VGA gain.

When switching between data and servo modes, the VGA gain is momentarily squelched and the input impedance is reduced by a factor of 10 (to allow quick recovery from transient offsets), then a fast recovery mode is initiated. External resistor R_{LOWS} sets the amount of time the low Z state is on.

During ultra fast recovery, the VGA gain is increased to 144 times its normal rate until the signal exceeds its target value. The loop then enters a "fast" mode. This high bandwidth mode continues until the fast acquisition window T_{FAQ} times-out, whereupon normal charge pump currents are reinstated and loop bandwidth is reduced to its normal value for servo mode. External resistor R_{FSQ} sets the fast acquisition window period, T_{FAQ}.

To optimize recovery for constant density recording, all charge pump currents track with the value loaded in the data rate register (DRR); current magnitude ranges from I_{QXX} at maximum DR to $I_{QXX}/2$ at minimum DR. The magnitude of the charge pump currents, I_{QXX}, are set by an external resistor connected between the RX pin and ground and are given by the following equations:

$$I_{QND} = \frac{1.2V}{RX} \quad (DRR = 11111),\ RX = 6\ k\Omega \qquad \textit{(eq. 1)}$$

$$I_{QNC} = I_{QND}/18,\ I_{QFC} = I_{QND}/2.25,\ I_{QUFC} = 8I_{QND},\ I_{QFD} = 8I_{QND}$$

The RX = 6 kΩ has been optimized for user data rates of 70-140 Mbps and can be scaled appropriately for lower data rates. VTC recommends that the AGC loop response be altered by varying the CAGCx capacitors and not the RX resistor. Since servo data is written at a lower fixed frequency, the magnitudes of charge pump currents in servo mode are set equal to those that occur at the minimum data rate in read mode.

For data reads, the analog AGC loop is utilized to quickly lock onto the incoming sync field preamble. When RG is asserted, the FIR, Viterbi detector, and decision-directed AGC and timing recovery circuits are powered up (if the programmable power reduction feature is enabled). An internal, delayed RG signal (RGD) is then generated two byte times after external RG is asserted. The sync field count begins when RGD is asserted. Refer to Diagram 1.

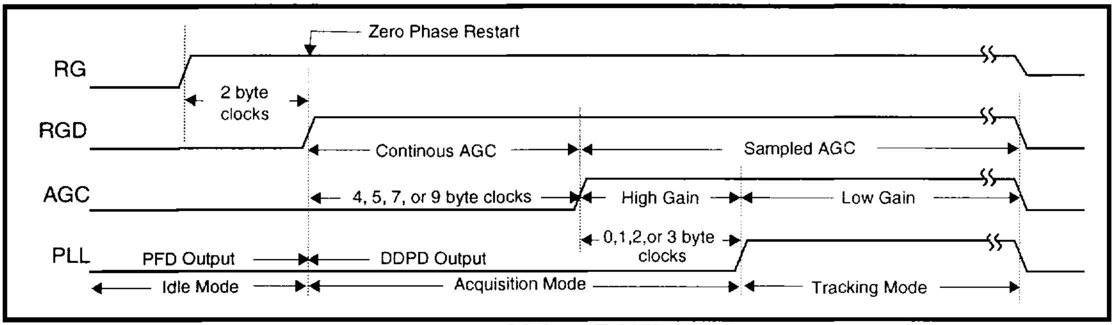


Diagram 1 VCO Sync Field Timing Diagram

The AGC transition in high gain mode and the PLL transition into tracking mode are based on two programmable sync-field counters, the AGC SF counter and the PLL SF counter. The AGC transition from continuous to sampled high gain is determined by one of four programmable counts of 4, 5, 7, or 9 byte times (for this discussion, a 'byte time' equals 8 channel-bit times) which are derived from the frequency synthesizer clock; this is the AGC SF count.

Additionally, the PLL acquisition time can be extended by one of four progammable counts of 0, 1, 2 or 3 byte times following the AGC SF count; this is the PLL SF count. The sampled AGC remains in the high gain mode for the sum of both counts, then transitions into low gain. The PLL transitions from idle to acquisition mode when RGD is asserted. The PLL remains in acquisition mode through the sum of both the AGC SF and PLL SF counts, whereupon, it transitions into the tracking mode.

The sampled AGC loop consists of the VGA, the programmable continuous time filter, the sampling 7-tap FIR equalizer, the decision amplitude detector and charge pump. Symmetrical charge and discharge currents are utilized in the sampled mode. To optimize recovery for constant density recording, the charge pump currents in the sampled mode track with the value loaded in the data rate register (DRR); current magnitude ranges from I_Q at maximum data rate (DR) to $I_Q/2$ at minimum DR. The magnitude of the charge pump currents, I_Q, can be programmed from the sample loop control register to 0, 20, 40, or 60 µA for DRR = 11111. The high gain charge pump current is fixed at 180 µA.

The VGA has an exponential characteristic of gain versus control voltage in order to minimize response time over the entire range of input voltages. When in the PGC mode, the amplitude detector, charge pump, and exponentiator are disabled, and the gain of the VGA is controlled by the PGC control register. The VGA has a linear gain versus DAC count and is expressed by the following equation:

$$A_V = [2(2.5 + N)] \qquad \text{(eq. 2)}$$

where N ranges between 0 and 15 decimal or 0000 to 1111 binary

PULSE QUALIFIER

The pulse detector (PD), converts analog read data into a digital pulse stream, utilizing amplitude discrimination. The timing between peaks is provided on the rising edges of the RDS output. The timing channel inputs, FDP/FDN, are direct-coupled from the differentiated output of the filter. The level channel inputs FAP/FAN are AC-coupled from the normal outputs of the filter.

The timing channel inputs (FD = FDP/FDN) are derived from the differentiated output of the low pass filter. A zero-cross comparator at FD detects the peaks of the waveform to preserve the timing of the read pattern. A bi-directional one shot circuit with nominal pulse width of 4ns clocks the D-type Flip-Flop on either positive or negative transitions of the FD input. Visibility into the timing channel signal HRCLK is provided in test mode (see Test Modes on page 34).

The HRCLK pulses are qualified by signals which are derived from the low pass filter output. Two comparators indicate when the positive (LP) and negative (LN) extents of the signal $V_{FA} = V_{FAP}\text{-}V_{FAN}$ exceed either the positive threshold (V_{THP}) or the negative threshold (V_{THN}) level. Independent control of positive and negative thresholds is provided with 5-bit DACs ranging from 20-80% of V_{FA}. Vthx=20+1.9×VALUE in percent, where VALUE ranges from 0 to 31. Once the signal exceeds the level threshold, a high level is presented to the D-input of the Flip-Flop. When the peak is reached, the timing channel clocks a '1' into the Flip-Flop and triggers a one-shot producing the RDS output. The Flip-Flop resets on the rising edge of RDS and is ready for the next bit after the one-shot times out. A nominal pulse width of 24 ns is provided at the RDS output. Consecutive same-polarity pulses are also qualified. RDS polarity information is provided with the RPOL output.

PROGRAMMABLE LOW PASS FILTER (LPF) / EQUALIZER

The filter is implemented as a 7-pole 0.05 degree linear phase equiripple low pass filter with matched normal and differentiated outputs. The cutoff frequency, boost, and DC group delay equalization are programmable.

The filter supplies normal and differentiated low-pass outputs with matched group delays. The normal output goes to the AGC and servo sections. The differentiated output, along with the normal output, is used by the level qualifier block to provide data and servo peak position information. The relative gain AO_D of the differentiated output to the normal output is nearly constant (at two-thirds the unboosted cutoff frequency) over the range of the cutoff frequency and boost level of the filter.

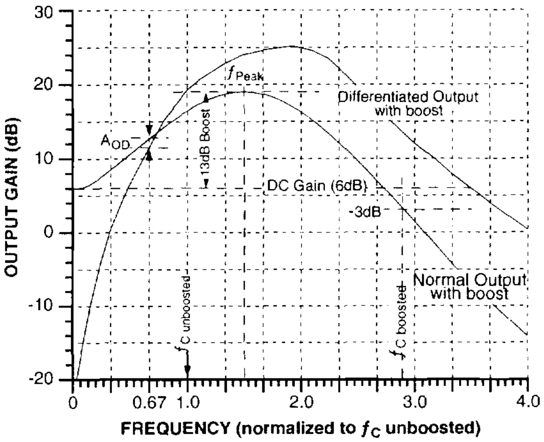
Cutoff frequency is controlled by the continuous time filter f_C DAC. The control word for the DAC is read from the CTF Data f_C register when SG=0; otherwise its read from the CTF Servo f_C register (see Table 4 Serial Register Bit Descriptions). Cutoff frequency (f_C), in MHz, is related to the binary control word by the following equation:

$$f_C = (0.323 \times N) + 4.5 \qquad (eq. 3)$$

where N ranges between 0 and 127 decimal

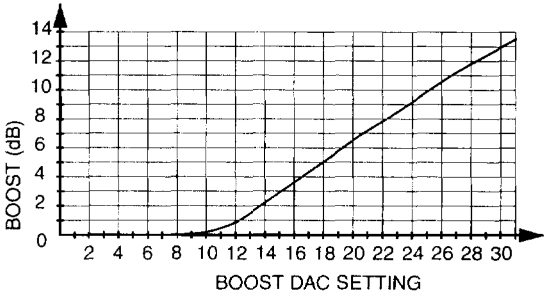
The amount of boost equalization depends on the output of the BOOST DAC. Boost is programmable from 0 to 13dB as measured from the low-frequency gain portion of the frequency domain transfer function to the peak in the transfer function.

Graph 1 shows normalized filter response curves with maximum boost for both the normal and differentiated outputs.



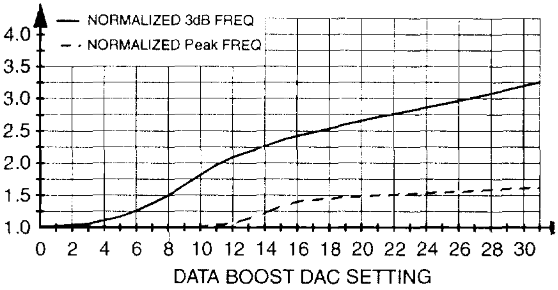
Graph 1 Normal and Differentiated Output Gains

Graph 2 shows the nominal relationship between the BOOST control word and the resulting boost level.



Graph 2 Ideal Boost (in dB) versus BOOST DAC VALUE

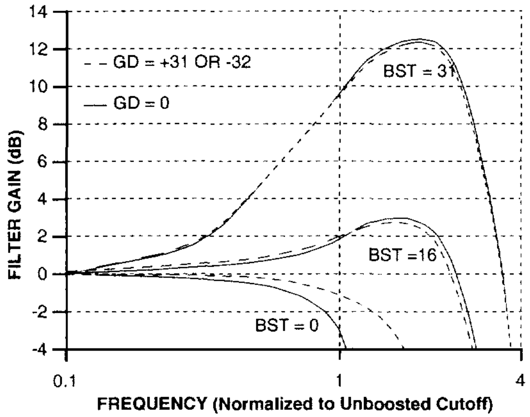
Graph 3 shows the effect of boost on the cutoff frequency.



Graph 3 Normalized f_c and f_{peak} versus DATA

Setting the desired boost through the boost register (with the group delay register set to zero) produces symmetric zeros on the real axis. This maintains the constant group delay as in the no boost case. The group delay register can be used to produce asymmetry in the zeros causing the group delay to vary. This can be desirable to compensate for asymmetry in the heads/media components. Group delay can be varied by ±30% from the symmetric zero (group delay register = 0) condition. The boost is held nearly constant as group delay is varied.

Graph 4 shows what happens to the magnitude response as the Group Delay register varies over extremes and under several boost conditions.



Graph 4 Gain Variations with Different Boost and Group Delay Settings

The group delay register is six bits wide in "two's complement" format. A code of +31 corresponds to a DC shift in group delay of +30%; a code of -32 corresponds to -30% shift in DC group delay. Group delay is expressed as:

$$GD_{DC} = 0.95 \times GD_{DAC} \qquad \textit{(eq. 4)}$$

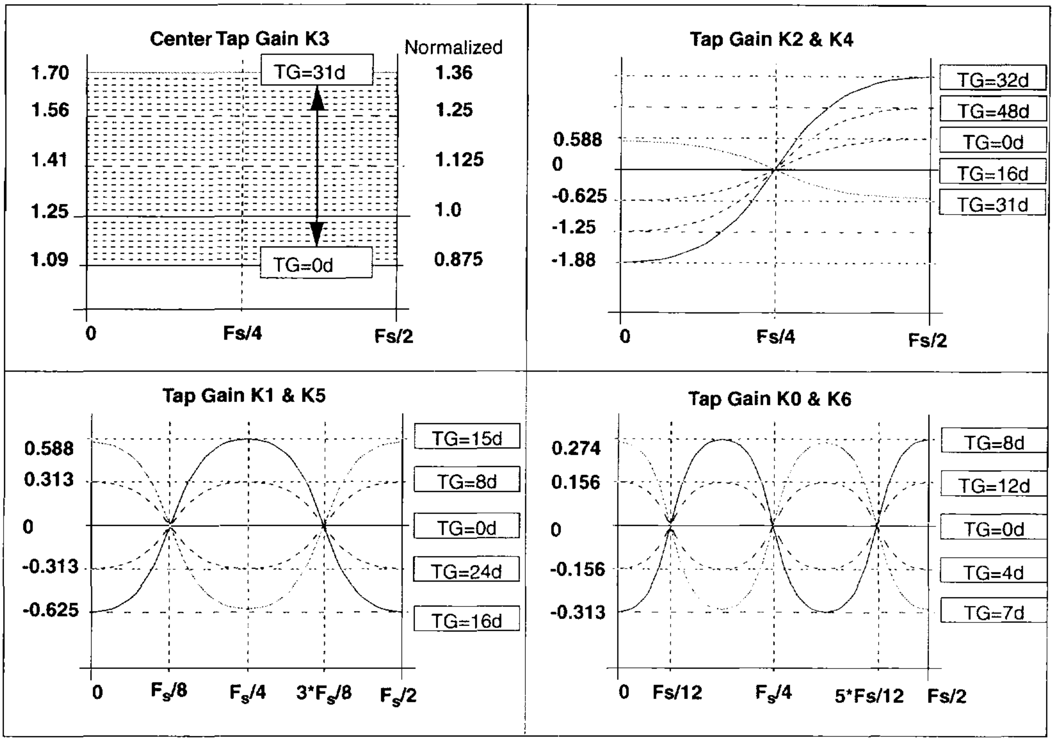
Group delay for an ideal 0.05 degree equiripple filter is flat within one percent out to twice the unboosted cutoff frequency. Because group delay is extremely sensitive to device mismatches and parasitic effects, a "real" filter will have variations of several percent. Group delay flatness is defined as the variation about an average value out to the specified frequency. The VM65014 group delay flatness is specified to be less then ±2% out to 1.5 times the unboosted cutoff frequency. It is expressed in percent because the group delay is inversely related to the unboosted cutoff frequency, and is about 12 ns at a cutoff of 48 MHz. Thus at this cutoff frequency, the group delay varies by less than 0.18 ns out to 72 MHz.

The absolute group delay through the Gain Control block and the filter consists of both a fixed delay and a delay that varies inversely with cutoff frequency. The group delay (T_{GD}), in nanoseconds, is expressed below as a function of the cutoff frequency in MHz.

$$T_{GD} = \left[3 + \frac{434}{f_C}\right]\text{ns} \qquad \textit{(eq. 5)}$$

FIR FILTER EQUALIZER

The FIR is a seven (7) tap transversal filter with independently-controllable tap weights. Independent control provides both gain and phase adjustment of the input signal. The following plot illustrates the possible gain variations achievable when symmetric taps are swept together over the allowable ranges, as listed in Table 1.



Graph 5 Symmetric Tap, frequency response curves

The H_0 term provides only a real valued response equal to the center tap gain. The gain response also includes finite bandwidth characteristics of the sampler. The sampler BW is about 350 MHz and will have some effect on the frequency characteristics. The ideal gain limits for the taps are shown below.

Table 1 FIR Tap Gain settings

Tap	K_{-3}	K_{-2}	K_{-1}	K_0	K_1	K_2	K_3
Gain Range	-0.156 +0.137	-0.312 +0.293	-.9375 +0.293	+1.09 +1.70	-.9375 +0.293	-0.312 +0.293	-0.156 +0.137
Actual bits	4	5	6	5	6	5	4
Eff. bits	7	7	7	7	7	7	7
Resolution	(1/64) X 1.25 = 19.56 mV/V						

FIR ADAPTION CIRCUIT

Normal operation:

The adaption process starts after RG has been asserted and the internal delayed read gate RGDP has become active. It should be noted that since the part is accessing the serial registers during adaption, the user should NOT attempt any serial register operation while RG is asserted and the AE bit is set.

Parameter Descriptions:

- Adaptation Control Test "ACTST"
  These bits allow the basic verification of the Adaptation Control logic.
- Adaptation Enable "AE"
  This bit controls whether adaptation is to be performed. It cannot be modified during an adaptation read cycle.
- Dead Zone "DZ"
  This three-bit control specifies how many update samples are required in either direction to cause adaptation in that direction. The value sets the threshold in symmetrical manner.
- Integration Length "INTL"
  This two-bit control selects the number of samples to average for each update cycle (12, 15, 18, or 21)
- Initial Tap Weight "ITW"
  This value selects which tap to adapt first.
- No Sync Byte "NOSB"
  This feature causes adaptation to occur at the point where the timing recovery circuit makes the transition from acquisition to tracking modes. This occurs during the VCO sync field even before the sync bytes.
  This option may be useful during initial drive optimization and data recovery modes.
- Tap Weight Range "TWR"
  This sets the number of taps that are adjusted. If all six taps are to be adjusted this value should be set to "0". By setting this value to "1" through "4" a reduced range of taps will be adjusted. The taps that are not adjusted are still active but are held at their preprogrammed values.
- Symmetry control "SYMC"
  This two-bit control selects which sets of taps should be controlled in a symmetrical manner.

Tap weights can be written and read by the controller. Thus the initial tap weight values can be preset near their optimal values and the final values can be read back after each adaption read cycle. The final taps weights remain as the initial tap weights for subsequent read cycles.

Proper selection of DZ and INTL can allow for rapid adaptation or for slow highly-stable tracking of system changes.

VITERBI DETECTOR

The Viterbi detector implements the maximum likelihood (ML) detector for PRML. The Viterbi detector block diagram is shown in Diagram 2.

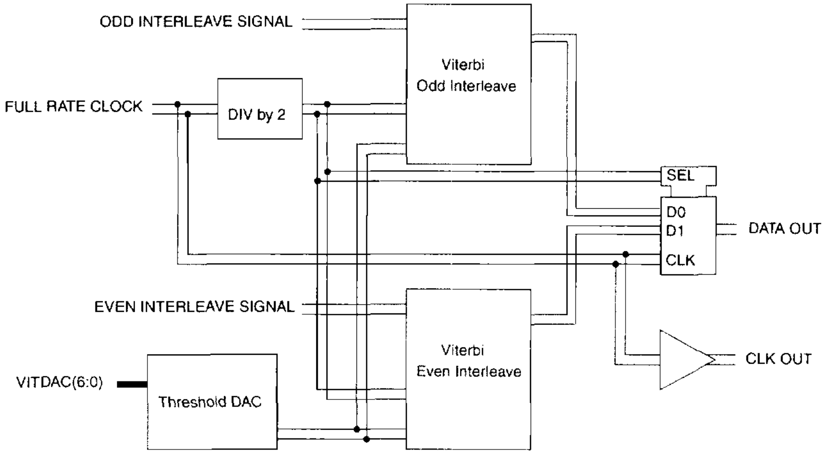


Diagram 2 Viterbi Detector Block Diagram

Note that all signals are differential. The incoming signal (from the FIR filter via the timing recovery block) has been demultiplexed into the odd and even interleaves on a bit-by-bit basis. This is shown in the diagram as the odd interleave signal and the even interleave signal. Each interleave of the Viterbi detector runs at 1/2 the channel data rate. Note that the odd and even interleaves of the Viterbi detector are clocked on opposite phases of the full rate data clock. Each interleave independently processes its data stream. The data streams from the odd and even interleaves are then multiplexed back together on a bit-by-bit basis to yield the recovered bit stream.

The Viterbi detector operates in the continuous amplitude, discrete time domain. This is also known as the sampled domain. The detector compares the sampled level of the analog waveform to the positive and negative thresholds established by the programmable Viterbi threshold window. The nominal Viterbi threshold window size is set by a 7-bit DAC which is controlled by the Viterbi DAC serial control register. Positive and negative thresholds in the Viterbi detector are modified based on the received data.

The dynamic thresholds in the Viterbi detector function to reject pulses of the same polarity as the most recent pulse, but of lesser amplitude. If a pulse of the same polarity as the most recent pulse exceeds the amplitude of the previous pulse, the 1 associated with the previous pulse (which is of lesser amplitude) is erased in the Viterbi detector's path memory. The path memory only has the ability to erase these smaller pulses if four or fewer zeroes have occurred between the two pulses of the same polarity. This requirement is satisfied by the (0,4,4) encoding that is used with this part.

The AGC circuit adjusts the signal amplitude to ±250 mV peak. Side sampling for PR4 produces a nominal sampled signal amplitude of ±180 mV. This is a pseudo-ternary signal with the ±1 levels equal to ±180 mV and the zero level equal to 0 mV. Thus, the Viterbi threshold, VIT_{TH}, is nominally set to 90 mV. Since the data is pseudo-ternary, the nominal Viterbi threshold window size is $2 \bullet VIT_{TH}$.

$$VIT_{TH} = \left[0.03 + 0.24\left(\frac{VALUE}{127}\right)\right] mV \qquad \text{(eq. 6)}$$

where VALUE is between 0 and 127, inclusive

Diagram 3 shows a block diagram of a Viterbi detector interleave.

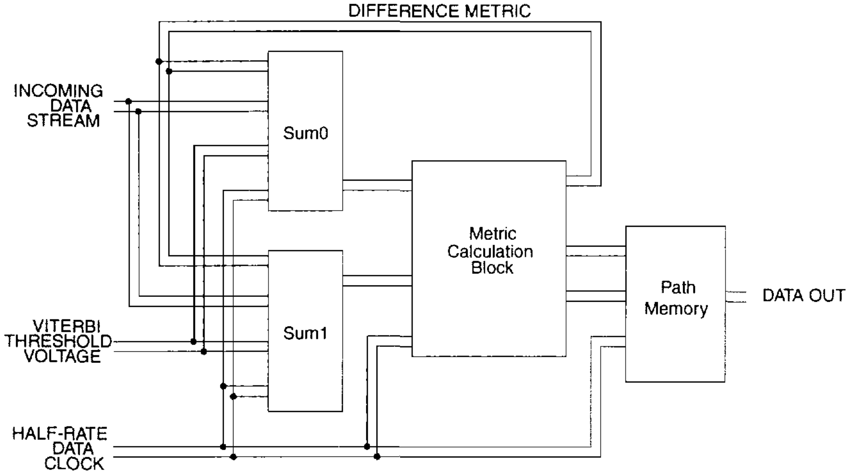


Diagram 3 Viterbi Interleave Block Diagram

The summing blocks, Sum0 and Sum1, each form two signals that are fed to the metric calculation block. Opposite polarities of the incoming data stream and the difference metric are used by Sum0 and Sum1. The metric calculation block outputs the difference metric (which is fed back to the Sum0 and Sum1 blocks) and the two data streams that are used by the path memory block. One of these two data streams from the metric calculation block represents 1's that come from positive pulses in the ternary data signal. The other data stream represents 1's due to the negative pulses in the ternary data stream. Two 1's in one of the data streams without an intervening 1 in the other data stream results in the path memory erasing the first of these two consecutive 1's. A 0 results when neither of the two data streams is a 1. Decoding of the ternary signal is straightforward: a positive or negative pulse results in a 1; no pulse decodes to a 0.This decoding action can be thought of as undoing the precoding function.

The Viterbi algorithm is a maximum likelihood detection technique. A conceptual description of the Viterbi algorithm follows. The data into the Viterbi detector is pseudo-ternary, that is, it has valid levels of 0 and ±1. The Viterbi detector uses the fact that two pulses on an interleave of the same polarity must have a pulse of the opposite polarity between them. As long as pulses of alternating polarity are received by the Viterbi detector, it functions like a simple ternary slicer.

The situation where two pulses of the same polarity arrive on an interleave without a pulse of the opposite polarity separating them can be divided into two cases: the first pulse is bigger than the second pulse or the second pulse is bigger than the first pulse. The Viterbi detector does not recognize the case where both pulses are of the same amplitude; it chooses one of the two pulses to be larger. For the following discussion, assume that two +1 pulses have occurred without a -1 pulse in between.

The case where the second pulse is smaller is handled by the dynamic thresholds in the Viterbi detector. The first (larger) pulse pulls the positive threshold up. The following pulse is smaller and therefore won't cross the upper threshold, thereby rejecting the smaller of the two +1 pulses.

The case where the second pulse is bigger than the first is handled by the path memory. The dynamic positive threshold is pulled up by the first +1 pulse and a 1 is output. The second +1 pulse comes along and exceeds the threshold set by the previous +1 pulse, causing a second 1 to be output to the path memory. The only way these two 1's in a row can be output is for the second pulse to be bigger than the first. The path memory uses this fact and erases the first of these two ones. In order to do this erasure, the path memory requires that no more than four zeros occur between the two 1's of the same polarity.

After evaluating these two cases of consecutive pulses of the same polarity, the Viterbi algorithm can be seen to operate as a ternary slicer except when two consecutive pulses of the same polarity occur. When this situation happens, the Viterbi algorithm chooses the larger of these two pulses and treats the other as if it were a 0.

FREQUENCY SYNTHESIZER

The Frequency Synthesizer (FS) is a PLL-based circuit that provides a programmable reference frequency for constant density recording applications. The frequency synthesizer output frequency can be programmed with a better than 1% accuracy via the M,N ("divide by") and DR (Data Rate) Registers. The synthesizer output frequency, F_{OUT}, should be programmed as close as possible to ((9/8)•User Data Rate). The synthesizer also supplies the timing reference for write precompensation so that the precompensation tracks the VCO period.

The frequency synthesizer requires an external passive loop filter to control its PLL locking characteristics. This filter is pseudo-differential and balanced in order to reduce the effects of common mode noise.

In Write and Idle modes, the programmable frequency synthesizer is used to provide a stable reference frequency to the timing recovery loop. In the Write and Idle modes, the frequency synthesizer output, when selected by the Control Test Mode Register, can be monitored at the TP3 test pin. In the Read mode, the FS output should not be selected for output on the test pins so that the possibility of jitter in the timing recovery PLL is minimized.

The synthesizer output frequency is programmed using the M and N registers of the frequency synthesizer via the serial port, and is related to the external reference clock input, FREF, as follows:

$$f_{out} = f_{FREF}\left[\frac{(M+1)}{(N+1)}\right] \qquad \text{(eq. 7)}$$

The M and N values should be chosen with the consideration of phase detector update rate and the external passive loop filter design. The Data Rate Register must be set to the correct VCO center frequency.

The DR register value directly affects the following:

- Center frequency of the frequency synthesizer VCO
- Center frequency of the timing recovery VCO
- Phase detector gain of the frequency synthesizer phase detector
- Write precompensation

The reference current for the DR DAC is set by an external resistor, RR, connected between the GND and RR pins. The VCO center frequency, f_c, and the charge pump current, I_{QP}, are given by the equations below. RR is the resistance of the external resistor in Ohms, X is the decimal equivalent of the DR Register bits and K_{VCO} (rad/V•s) is the VCO gain.

$$\omega_C = \left(\frac{\pi \times 10^{10}}{RR}\right) \times (33 + X) \quad (0 \le X \le 31) \qquad \text{(eq. 8)}$$

$$K_{VCO} = 0.35 \times \omega_C \qquad \text{(eq. 9)}$$

$$I_{QP} = \left(\frac{0.01875}{RR}\right) \times (63 - X) \qquad \text{(eq. 10)}$$

TIMING RECOVERY

The data synchronizer uses a fully integrated, fast acquisition, PLL to perform clock recovery from the incoming data stream.

Fast acquisition is obtained by locking the loop to the synthesizer during Write, Servo & Idle modes which minimizes the frequency transient that occurs when the Read mode is initiated. Thus the timing recovery PLL uses two separate phase detectors to drive the loop. A Decision-directed Phase Detector (DDPD) is used in the Read mode and phase-frequency detector (PFD) is used in the Write, Servo, and Idle modes.

The Read mode is initiated by performing a zero phase restart of the VCO, which will force a phase alignment to the incoming 2T (1/4 data-rate) clock pattern. The samples taken immediately after the restart will be used by the DDPD to "coarse adjust" the VCO. After the sync field count has reached the programmed count (AGC + PLL offset), as shown in Diagram 1, the PLL will be switched to tracking mode which reduces the loop bandwidth (BW) by a factor of 2 or 4 depending on the register settings. In the tracking mode the input to the DDPD is taken from the output of the FIR filter.

TIMING RECOVERY OPERATION

In Write or Idle mode, active when the RG (read gate) line is low, the mux selects the PFD as the input to the Q-pump and P-mult circuits. The two signal paths provide Proportional and Integral error terms to the VCO input. The benefit of this architecture is independent control of the loop parameters BW (bandwidth) and ζ (damping factor) via the control registers. The proportional term is controlled by the Damping Ratio DAC and the integral term is controlled by the Data Rate (DR) DAC. The VCO center frequency is set by the DR DAC; as the rate is increased the VCO gain must increase in order to maintain a constant locking range. The damping factor remains constant as the loop BW is changed. The net result of the loop is that it will settle in a constant number of clock cycles independent of the clock period.

The Read mode is initiated by a positive transition on the "RG" line as shown in Diagram 4.

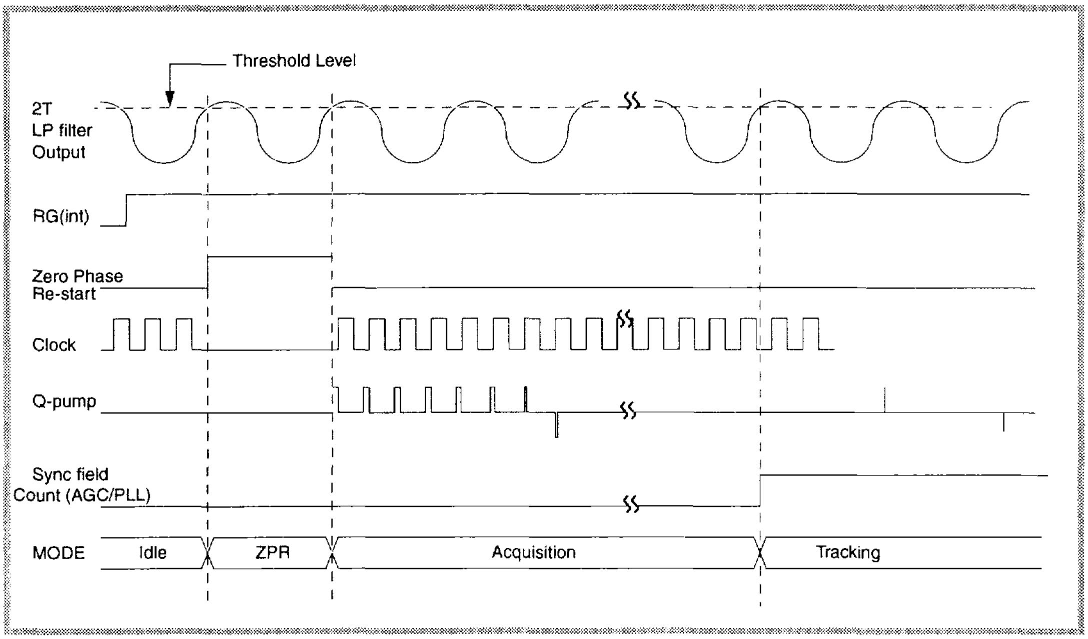


Diagram 4 Timing Recovery Operation

The VCO is held in a low output state when the 2T input signal crosses the threshold set by the Zero Phase Restart DAC. The second time the threshold is crossed the VCO restarts. The threshold is set to align the VCO to the ideal PR4 sample phase of Π/4, which is 0.707 times the AGC's analog servo voltage V_{TH}. The analog and digital delays in the samplers and the VCO require a slight variation of that sample threshold so a multiplying DAC is used to obtain the optimal set point. Once the VCO restarts, the DDPD output is used as the phase error to drive the PLL. The initial gain will be high to minimize the acquisition time and the computation of the phase error is done with a robust technique which prevents any false lock-up modes. After the sync field count has been reached the error detection mode will be changed to allow for three valid signal levels (only two are used in Acquisition) and the gains are reduced to reduce jitter. Since the AGC gain control is independent the timing control it can be switched at any point after the FIR has taken 7 samples (7-tap filter) and is switched slightly before the timing transition from Acquisition to Tracking. If the DSP mode is in progress this transition will enable the detection of the sync byte.

WRITE PRECOMPENSATION

The write precompensation circuitry is provided to compensate for media bit shift caused by magnetic nonlinearities. The circuit recognizes six specific write data patterns of 4 channel bit lengths and can add delay in the transition of write data bits to counteract the magnetic non-linearity effect. The magnitude of the time shift is programmable via a Register and is made proportional to the frequency synthesizer's VCO period (i.e. data rate). Since the WPC operation is performed prior to the final T-FF (which is part of the precoding function) only three distinct patterns are decoded. Each of these three patterns may be independently programmed. The precoding operation is included with the WPC circuitry.

Each DAC allows write precompensation delay (Twpc) values to be programmed from 0 to 0.20T with 1.25% resolution as shown in the following equations.

$$\text{Twpc(Pattern1, 3)} = (0.013 \bullet \text{Kwp} + 0.20 \bullet \text{HBIT}) \bullet \text{T} \qquad \textit{(eq. 11)}$$

$$\text{Twpc(Pattern2)} = (0.013 \bullet \text{Kwp}) \bullet \text{T} \qquad \textit{(eq. 12)}$$

where T is the period of the VCO, in nano-seconds, and Kwp is the value of the 4-bit DAC word for any of the three patterns

HBIT is an independently-programmable bit which allows an addition 20% precompensation for patterns 1 and 3. By setting this bit high, patterns 1 and 3 will have a range from 20 to 40 percent of the VCO period. HBIT does not affect pattern 2. If no compensation is desired for any of the three patterns, then that particular DAC word may be set to 0.

The precoder and all internal states in the WPC get reset with the de-assertion of write gate (WG) so that the write path is always in the same state upon assertion of WG. This also prevents any false data from being sent to the preamp during non-write modes.

Pattern	*Data Pattern*	*Write Data Pattern*
1	011	0010/1101
2	101	0110/1001
3	111	0101/1010

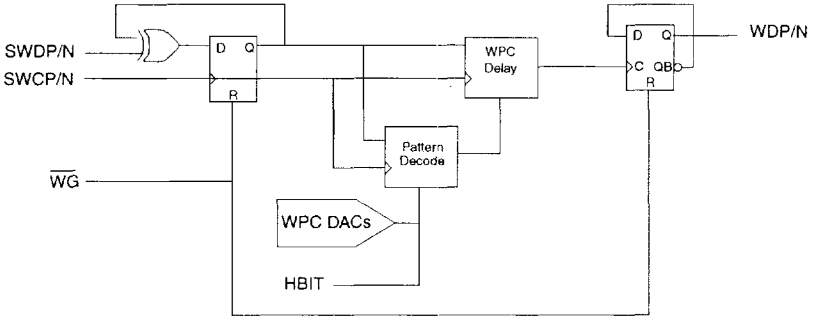


Diagram 5 WPC/Precoder Block Diagram

SERVO DEMODULATOR

The embedded servo demodulator processor extracts the head position error information from the embedded servo bursts using an area detection technique. It supports full quadrature demodulation through the use of an array of four area detector channels. The area detection technique provides improved noise immunity over peak detection. A block diagram for the servo demodulator is shown in Diagram 6.

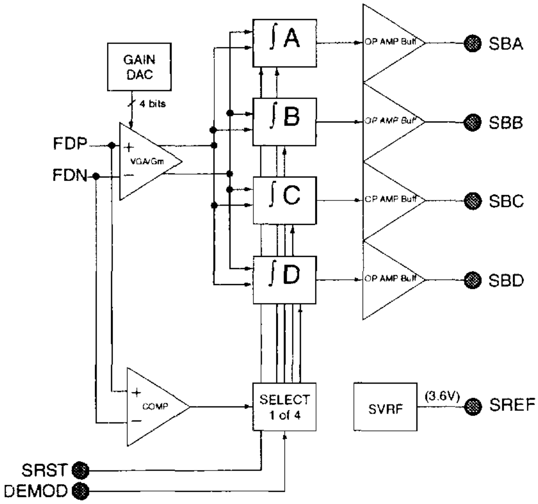


Diagram 6 Servo Demodulator Block Diagram

The demodulator contains a variable gain amplifier, rectifier, four pulse area detectors and required timing logic. The differentiated filtered servo bursts are input to a variable gain amplifier (VGA). The VGA allows the demodulator block to accommodate a wide dynamic range of servo burst amplitudes and process variations of the internal integration capacitors and resistors. The gain range of the VGA is ±40% in steps of 5%, as defined in the servo gain control register. The amplified signal is full-wave rectified and input to an array of four area detectors. The area detector consists of a gm stage driving an on-chip integration capacitor. Note that the ±30% tolerance of the on-chip capacitors and gm block can be calibrated by adjusting the gain of the VGA.

Each area detector is selectively enabled when the DEMOD control input goes high and integrates the pulse voltage amplitude of the servo burst. After the burst pulses have been integrated, the DEMOD signal is brought low, the area detector is disabled and the final integrated voltage is held. Consecutive cycles of the DEMOD pin cause the A, B, C, and D area detectors to sample the input waveform. Upon the low level of SRST, the servo burst outputs are reset to the SREF voltage.

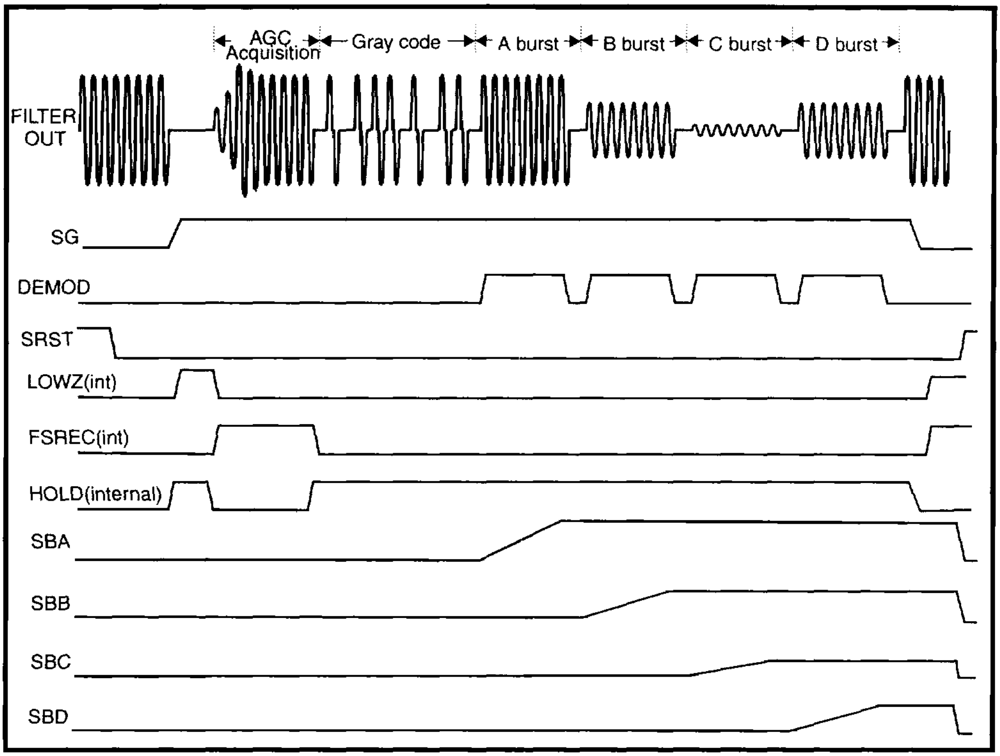


Diagram 7 Servo Timing Diagram

MODE CONTROL AND POWER MANAGEMENT

The fundamental operating modes are controlled by the servo gate (SG), read gate (RG), and write gate (WG) input pins. The exclusive assertion of any of these inputs causes the circuit to enter that mode. If none of these inputs is asserted, the circuit is in IDLE mode. If more than one of the inputs is asserted, the mode is determined by the following hierarchy: SG overrides RG which overrides WG. The mode that is overriding takes effect immediately. SG and RG are asynchronous inputs and may be initiated or terminated at any time. WG is also an asynchronous input, but should not be terminated prior to the last output write data pulse to the preamp.

Table 2 Mode Control

WG	*RG*	*SG*	*PD*	*MODE*
X	X	X	1	Entire chip powered down; serial port still functional
0	0	0	0	IDLE mode; read data blocks powered down if PREN = '1'
X	X	1	0	SERVO mode; read data blocks powered down if PREN = '1'
X	1	0	0	READ mode; read data blocks powered on
1	0	0	0	WRITE mode; read data blocks powered down if PREN = '1'

DIGITAL CONTROL

Control of the chip is performed through a serial digital interface and a (16,12) bit wide register file. Control information is stored in the register file and used directly as digital control lines or sent to one of the DACs to create analog control signals.

The interface consists of three CMOS-level signals for input/output data, clock, and enable. Upon asserting SPEN, the serial port is enabled and ready for input on SPDATA and SPCLK. The SPDATA line provides the read/write, address and data information.

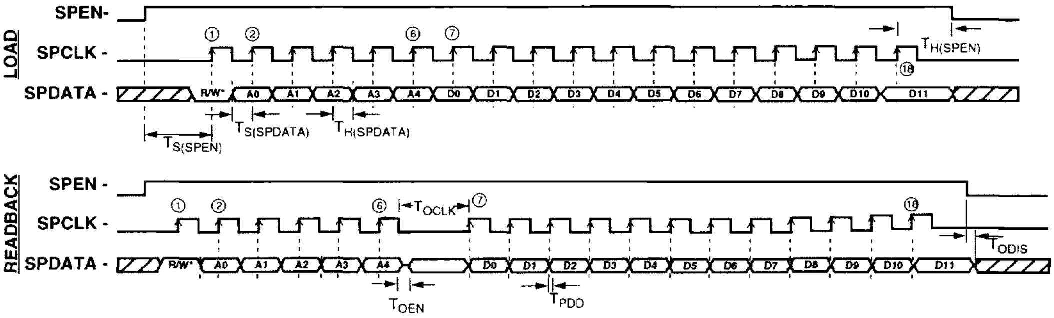


Diagram 8 Serial Register Load & Readback Timing

Table 3 Serial Register Bit Allocation

<table>
<tr><th rowspan="2">Register Address</th><th colspan="12">Data Bit</th></tr>
<tr><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>0</td><td colspan="4">PGC DAC</td><td colspan="2">SQPI DAC</td><td colspan="4">FIR Tap 0</td><td>rsv'd</td><td>rsv'd</td></tr>
<tr><td>1</td><td colspan="5">DR DAC</td><td>TFAQ</td><td colspan="4">FIR Tap 6</td><td>rsv'd</td><td>rsv'd</td></tr>
<tr><td>2</td><td colspan="6">CTF Data Group Delay</td><td colspan="5">FIR Tap 1</td><td>rsv'd</td></tr>
<tr><td>3</td><td colspan="6">CTF Servo Group Delay</td><td colspan="5">FIR Tap 5</td><td>rsv'd</td></tr>
<tr><td>4</td><td colspan="4">WPC Pattern 2</td><td>PGCEN</td><td>DHBW</td><td colspan="6">FIR Tap 2</td></tr>
<tr><td>5</td><td colspan="4">WPC Pattern 3</td><td>WPCHR</td><td>FAQSEN</td><td colspan="6">FIR Tap 4</td></tr>
<tr><td>6</td><td colspan="4">WPC Pattern 1</td><td>WPCCK</td><td>YC24</td><td>TC 3</td><td colspan="5">FIR Tap 3</td></tr>
<tr><td>7</td><td colspan="6">FS Divide-by-N</td><td>SLEEP</td><td>PRST</td><td>TRCKSL</td><td>TBUFF</td><td>PDTST</td><td>VITOWD</td></tr>
<tr><td>8</td><td colspan="4">Servo Gain</td><td>FSCKSL</td><td colspan="7">CTF Data Boost</td></tr>
<tr><td>9</td><td colspan="5">Level Qual Pos V_{TH}</td><td colspan="7">CTF Servo Boost</td></tr>
<tr><td>10</td><td colspan="5">Level Qual Neg V_{TH}</td><td>LPFBYP</td><td colspan="2">WDSEL (1:0)</td><td>SRVDB</td><td>TRGAIN</td><td>REFSEL</td><td>PREN</td></tr>
<tr><td>11</td><td colspan="7">CTF Data Fc</td><td colspan="5">Zero Phase Restart DAC</td></tr>
<tr><td>12</td><td colspan="7">CTF Servo Fc</td><td colspan="5">DSP Select</td></tr>
<tr><td>13</td><td>HLD</td><td>rsv'd</td><td>rsv'd</td><td colspan="2">ACTST</td><td colspan="2">SYMC</td><td colspan="5">Zero Phase Restart DAC</td></tr>
<tr><td>14</td><td>CMXEN</td><td colspan="3">TP1 Select</td><td>S E LTE</td><td>AGCEN</td><td>PLLEN</td><td>TSRV</td><td>BMXEN</td><td colspan="3">Test Mux Select</td></tr>
<tr><td>15</td><td colspan="8">FS Divide-by-M</td><td colspan="2">AGC SF Count</td><td colspan="2">PLL SF Count</td></tr>
<tr><td>24</td><td>AE</td><td colspan="2">DZ</td><td colspan="2">INTL</td><td colspan="3">ITW</td><td>NOSB</td><td colspan="3">TWR</td></tr>
</table>

Table 4 Serial Register Bit Descriptions

Reg. Addr	Bit(s)	Description	Usage
0	5:2	FIR Tap 0 2's Complement	$K_0 = 0.0194 \times$ VALUE in V/V $-8 \leq$ VALUE ≤ 7
	7:6	SQPI DAC: AGC Sampled Charge Pump Current DAC	I = 20 × VALUE in µA I = Charge Pump Current
	11:8	PGC DAC: Programmable Gain Control DAC	$A_V = (2.8 \times \text{VALUE}) + 2.4$ $0 \leq$ VALUE ≤ 15 A_V = VGA Gain

Table 4 Serial Register Bit Descriptions

1	5:2	FIR Tap 6 2's Complement	$K_6 = 0.0194 \times \text{VALUE}$ in V/V $-8 \le \text{VALUE} \le 7$
	6	TFAQ: Test Fast Acquisition. Allows for testing of fast and ultra fast charge current.	0: Normal Mode 1: Test Mode (Fast Acquisition. always on)
	11:7	DR DAC: Data Rate DAC	$\omega_0 = \left(\frac{4 \times 10^{10}}{RR}\right) \times (33 + \text{VALUE})$ in Mrad/s $0 \le \text{VALUE} \le 31$ ω_0 = VCO center frequency RR = Value of external resistor in Ohms
2	5:1	FIR Tap 1 2's Complement	$K_1 = 0.0195 \times \text{VALUE}$ in V/V $-16 \le \text{VALUE} \le 15$
	11:6	CTF Data Group Delay 2's Complement	$GD_{DC} = 0.95 \times \text{VALUE}$ in % $-32 \le \text{VALUE} \le 31$
3	5:1	FIR Tap 5 2's Complement	$K_5 = 0.0195 \times \text{VALUE}$ in V/V $-16 \le \text{VALUE} \le 15$
	11:6	CTF Servo Group Delay 2's Complement	$GD_{DC} = 0.95 \times \text{VALUE}$ in % $-32 \le \text{VALUE} \le 31$
4	5:0	FIR Tap 2 2's Complement	$K_2 = (0.0195 \times \text{VALUE}) - 0.3125$ in V/V $-32 \le \text{VALUE} \le 31$
	6	DHBW: Disable High Bandwidth Mode of AGC. Disables fast discharge currents when FAQ is high. Normal charge/discharge currents are used.	0: Normal Mode 1: Disable high bandwidth
	7	PGCEN: Enable Programmable Gain Control Mode of VGA. Allows the VGA gain to be adjusted through PGC DAC.	0: Normal Mode (AGC loop active) 1: Programmable Gain Mode
	11:8	WPC Pattern 2: Determines amount of precomp for pattern 2	$Twpc = (0.013 \bullet \text{VALUE}) \bullet T$ $0 \le \text{VALUE} \le 15$ Twpc = Time delay of pattern transition T = Period of Data Rate clock
5	5:0	FIR Tap 4 2's Complement	$K_4 = (0.0195 \times \text{VALUE}) - 0.3125$ in V/V $-32 \le \text{VALUE} \le 31$
	6	FAQSEN: Enable Fast Acquisition on falling edge of Servo Gate (SG).	0: Normal Mode 1: Enable fast Acquisition
	7	WPCHR: WPC High Range Bit; Selects patterns 1& 3's precomp range See WPC Pattern 1 & 3	0: 0 - 20% Precompensation 1: 20 - 40% Precompensation
	11:8	WPC Pattern 3: Determines amount of precomp for pattern 3	$Twpc = (0.013 \bullet \text{VALUE} + 0.20 \bullet \text{WPCHR}) \bullet T$ $0 \le \text{VALUE} \le 15$ Twpc = Time delay of pattern transition T = Period of Data Rate Clock WPCHR = WPCHR Bit Setting

Table 4 Serial Register Bit Descriptions

6	4:0	FIR Tap 3	$K_3 = (0.0195 \times \text{VALUE}) + 1.094$ in V/V $0 \le \text{VALUE} \le 31$
	5	TC3: Tap Centering, 3rd Tap. Controls gain offset in FIR center tap (tap 3).	1: Normal Mode, $1 < \text{gain} < 1.7$ 0: Test Mode, $0 < \text{gain} < 0.7$
	6	TC24: Tap Centering, 2nd & 4th Taps. Controls the gain offset of FIR taps 2 & 4.	1: Normal Mode, $-.93 < \text{gain} < +.3$ 0: Test Mode, $-.62 < \text{gain} < +.62$
	7	WPCCK: WPC clock select. Allows either the Positive or Negative edge of SWCP/N to be chosen to clock in SWDP/N	0: Positive edge chosen 1: Negative edge chosen
	11:8	WPC Pattern 1: Determines amount of precomp for Pattern 1	$\text{Twpc} = (0.013 \bullet \text{VALUE} + 0.20 \bullet \text{WPCHR}) \bullet \text{T}$ $0 \le \text{VALUE} \le 15$ Twpc = Time delay of pattern transition T = Period of Data Rate Clock WPCHR = WPCHR Bit Setting
7	0	VITOWD: Viterbi OverWrite Disable. Allows the path memory over-write feature to be disabled in the Viterbi Detector	0: Normal Mode 1: Over-write disabled
	1	PDTST: Phase Detector Test. A high prevents the input to the decision-directed phase detector (and Viterbi detector) from switching from the low pass filter output to the FIR output.	0; Normal Mode 1: Test Mode
	2	TBUFF: Allows current mode output buffers to be put into a high current mode, used for testing	0: Normal Mode 1: High current (Test) Mode
	3	TRCKSL: Timing Recovery Clock select, chooses between the TR VCO output being chosen or an alternative reference in its place	0: Timing Recovery VCO chosen (Normal) 1: Alternative reference chosen, specific reference determined by REFSEL bit
	4	PRST: Programmable reset for synth. dividers and divide-by-4 in timing recovery PFD.	0: Normal Mode 1: Reset Mode
	5	Sleep	0: Normal (Powered On) Mode 1: Power Off Mode
	11:6	FS Divide-by-N: Reference divider value in the Frequency Synthesizer	$f_{out} = f_{FREF}\left[\frac{(M+1)}{(N+1)}\right]$ f_{out} = Output frequency of VCO (in MHz) f_{FREF} = Input frequency on FREF pin M = Divide-by-M setting N = Divide-by-N setting

Table 4 Serial Register Bit Descriptions

8	6:0	Viterbi Threshold DAC. Nominal setting is VALUE = 45.	$VIT_{TH} = 0.047 + 0.376\left(\frac{VALUE}{127}\right)$ in Volts $0 \le VALUE \le 127$
	7	FSCKSL: Frequency Synthesizer clock select	0: VCO output selected (Normal Mode) 1: SWCP/N input selected
	11:8	Servo Gain DAC: 4 bit DAC which controls the voltage gain of the servo block.	$V_{SB} = \left[\left(\frac{N \cdot V_{DIFF}}{3}\right) \cdot \left(0.6 + \frac{SDAC}{20}\right)\right] + 0.05$ V_{SB} = Integrated servo burst output in V. N = Number of integer servo burst cycles. V_{DIFF} = Continuous time filter differentiated output. (dppV). This signal can be measured on TP2 test point output. SDAC = Servo DAC setting (0 - 15). Nominal setting: 1000.
9	6:0	Damping Ratio DAC	$P = K \bullet \left(\frac{127 - VALUE}{127}\right)$ $\xi = \frac{P}{2}\sqrt{\frac{KVCO \cdot KDS \cdot C}{I \cdot G_m}}$ $0 \le VALUE \le 127$ K = Gain of Pmultiplier KVCO = Gain of TR VCO KDS = Gain of phase detector, either the PFD in W/I mode or DDPD in Read Mode C = Value of external capacitor I = Gain of Imultiplier G_m = Gain of QPUMP
	11:7	Level Qual Pos V_{TH}: PDQ Positive Threshold Qualification Level. Measured as a percentage of V_{LQ}	Vth = 20 + (1.9 × VALUE) in percent $0 \le VALUE \le 15$

Table 4 Serial Register Bit Descriptions

10	0	PREN: WRITE/IDLE (W/I) mode power reduction enable	0: No power reduction in W/I mode 1: FIR/VIT/DDPD powered off during W/I
	1	REFSEL: Selects reference to use in place of Timing Recovery VCO output. Used in conjunction with TRCKSL Bit	0: Selects FDSP/N Input 1: Selects synth. output as reference
	2	TRGAIN: Selects Gain of QPUMP and Pmultiplier while in Tracking Mode compared to respective gains in Acquisition Mode	0: Attenuate QPUMP gain by 16, Pmult by 4 1: Attenuate QPUMP gain by 4, Pmult by 2
	3	SRVDB: Disables (powers down) Servo block and enables analog test mux	0: Servo block enabled 1: Servo block disabled
	5:4	WDSEL: Write Data Select, determines what signal will be selected as output on the WDP/N lines	BIT (5:4) 0 0: Toggle Flip-Flop in data path 0 1: No Toggle Flip-Flop in data path 1 0: SWDP/N inputs selected as output 1 1: FDSP/N inputs selected as output
	6	LPFBYP: Low Pass Filter Bypass. Allows differential signal to be injected immediately after the internal AC Coupling Caps. Test signal is input on RLOWZ and RFSR pins	0: Normal Mode 1: Test Mode (lowpass filter bypassed)
	11:7	Level Qual Neg V_{TH}: PDQ Negative Threshold Qualification Level. Measured as a percentage of V_{LQ}	$V_{TH} = -20 + (1.9 \times \text{VALUE})$ in percent $0 \le \text{VALUE} \le 15$
11	4:0	CTF Data Boost	See Graph 2
	11:5	CTF Data Fc: Cutoff frequency of LPF while in READ Mode	$f_C = (0.323 \times \text{VALUE}) + 7$ in MHz $0 \le \text{VALUE} \le 127$
12	4:0	CTF Servo Boost	See Graph 2
	11:5	CTF Servo Fc: Cutoff frequency of LPF while in SERVO Mode	$f_C = (0.323 \times \text{VALUE}) + 7$ in MHz $0 \le \text{VALUE} \le 127$

Table 4 Serial Register Bit Descriptions

13	4:0	ZPR DAC: Zero Phase Restart DAC used to determine time before first sample is taken on the Sync Field 2T pattern	Nominal setting: 10001
	6:5	Symmetric Control: Determines which if any of the taps will be symmetrically adjusted.	SYMC...........Taps which will be identical 0.....................(2 & 4) 1.....................(2 & 4) & (1 & 5) 2.....................(2 & 4) & (1 & 5) & (0 & 6) 3.....................all taps asymmetric
	8:7	Adaption Control Test: Allows the adaption circuitry to be tested by forcing either an up, down or hold signal.	ACTest.......Resulting mode 0....................Normal operation 1....................Up forced 2....................Down forced 3....................Hold forced
	11	HLD: Hold mode for AGC and timing recovery loops.	0: Normal operation. 1: Both AGC and timing recovery loops forced into a hold (coast) mode. Intended for coasting over thermal asperities.

Table 4 Serial Register Bit Descriptions

14	2:0	Test Mux Select: Selects which internal signal will be multiplexed to the various output pins	See Table 6
	3	BMXEN: Enables the Bipolar test point muxes	0: Bipolar Test Muxes disabled (Normal Mode) 1: Bipolar Test Muxes enabled
	4	TSRV: *Test Servo operating mode*	0: Normal Mode (synchronous) 1: Test Mode (asynchronous)
	5	PLLEN: Allows the internal PLL signal to be programmably enabled/disabled for test purposes. PLL is asserted at the transition from acquisition mode to tracking mode	1: Normal Mode, (PLL SF count enabled) 0: Test Mode, (PLL SF count disabled)
	6	AGCEN: Allows the internal AGC signal to be programmably enabled/disabled for test purposes. AGC is asserted once the AGC count is reached in the Sync Field	1: Normal Mode, (AGC SF count enabled) 0: Test Mode, (AGC SF count disabled)
	7	SELTE: Selects which Timing Error the QPUMP will receive from the DDPD	0: Resampled Timing Error (Normal Mode) 1: Non-resampled Timing Error
	10:8	TP1 Select: Selects which internal signal to mux out to the TP1 test point.	See Table 5
	11	CMXEN: CMOS Test muxes enable	0: CMOS test mode enabled 1: CMOS test mode disabled (Normal Mode)
15	1:0	PLL SF Count: Determines how many user data bytes of data rate clock pass, after AGC has timed out, before PLL signal, tracking mode, begins	Bit Byte Clocks 1 0 0 0 0 1 0 1 2 1 0 3 1 1
	3:2	AGC SF Count: Determines how many user data bytes of data rate clock pass, after RGD has occurred, before AGC signal begins *RGD occurs 2 user data bytes clocks following external RG being asserted*	Bit Byte Clocks 1 0 4 0 0 5 0 1 7 1 0 9 1 1
	11:4	FS Divide-by-M: VCO feedback divider value in the Frequency Synthesizer	$f_{out} = f_{FREF}\left[\frac{(M+1)}{(N+1)}\right]$ in MHz f_{out} = Output frequency of VCO f_{FREF} = Input frequency on FREF pin M = Divide-by-M setting N = Divide-by-N setting

Table 4 Serial Register Bit Descriptions

24	2:0	Tap Weight Rollover value: Determines which of the FIR taps will be adapted by determining which tap gets adapted following Tap 4.	TWR.......Tap to 'roll-back' to 0...............Tap 0 1...............Tap 6 2...............Tap 1 3...............Tap 5 4...............Tap 2 5...............Tap 4
	3	NO Sync Byte: Allows the FIR adaption routine to begin without requiring a Sync Byte Found to occur. Adaption will begin after PLL SF Count has been reached with this bit set.	0: Normal mode, Sync Byte starts adaption 1: PLL SF Count starts adaption
	6:4	Initial Tap Weight: Determines which tap the adaption routine will adapt first.	ITW.........Tap to adjust first 0...............Tap 0 1...............Tap 6 2...............Tap 1 3...............Tap 5 4...............Tap 2 5...............Tap 4
	8:7	Integration Length: Determines the number of cycles the adaption circuit will integrate over when deciding whether the current tap weight should be incremented, decremented or held.	INTL.........Integration Length 0...............12 cycles 1...............15 cycles 2...............18 cycles 3...............21 cycles
	10:9	Dead Zone: Determines the required differential number of updates (delta) in either direction to qualify an increment or decrement decision. If this delta is not reached then the current tap weight is simply held.	DZ...........Differential number of updates 0...............delta = 3 1...............delta = 7.5 2...............delta = 10.5 3...............delta = 16
	11	Adaption Enable: Enables the adaption circuitry	0: Adaption circuit NOT active 1: Adaption circuit enabled

TEST MODES

There are sixteen test modes that are used in the VM65014. The test modes are controlled by two different sets of test addresses (TSEL[2:0] & TP1[2:0]) in the serial register, the bipolar test enable (BMXEN) and the CMOS test enable (CMXEN), as shown in Table 5, Table 6 and Table 7.

Table 5 TP1 Control

BMXEN	***TP1 SEL[2:0] bits***			***Output pins***
	2	***1***	***0***	***TP1 (diff analog)***
1	0	0	0	TR VCO/4
1	0	0	1	Timing Error
1	0	1	0	Y_n
1	0	1	1	Vit Sig E
1	1	0	0	Held Sig Odd
1	1	0	1	FIR out
1	1	1	0	TR VCO Control
1	1	1	1	CTF diff
0	X	X	X	normal op.

Table 6 Bipolar Test Register Decode

BMXEN	***TSEL[2:0] bits***			***mode***	***Output pins***		
	2	***1***	***0***		***TP2 (diff analog)***	***TP3 (PECL)***	***TP4 (PECL)***
1	0	0	0	0	Held Sig Evn	DV64	DV256
1	0	0	1	1	VGA in	FSUP	FSDN
1	0	1	0	2	VGA out	FS VCO	TR VCO
1	0	1	1	3	Vit Sig O	MX	T0
1	1	0	0	4	CTF norm	YHB/YLB	XPB/XNB
1	1	0	1	5	CTF norm ac	TRUP	TRDN
1	1	1	0	6	Int_ε	ε_n	C_n
1	1	1	1	7	Y_{n-1}	X_1	X_{N1}
0	X	X	X	X	power down	power down	power down

Table 7 CMOS Test Register Decode

CMXEN	TSEL[2:0] bits			mode	Output pins	
	2	1	0		RDS (CMOS)	RPOL (CMOS)
1	0	0	0	0	LP	HCLK
1	0	0	1	1	LZDEL	FRDEL
1	0	1	0	2	HLDEL	RGDP
1	0	1	1	3	dv/dt comp	
1	1	0	0	4	AGCN	PLLN
1	1	0	1	5	SHGN	PDSELN
1	1	1	0	6	DMN	SRVCNT
1	1	1	1	7		
0	X	X	X	X	normal op.	normal op.

Table 8 Test Signal Descriptions

Test Signal Name	Description
TR VCO/4	Timing recovery VCO clock divided by 4
Timing Error	Timing error for the Timing Recovery Loop.
Yn	Resampled FIR output at the "current" time
Vit Sig E	The even FIR interleave being input to the Viterbi detector.
Held Sig Odd	Held signal value for the odd interleave of Viterbi detector.
FIR out	Output of the Finite Impulse Response filter.
TR VCO Control	Analog control input to the Timing Recovery VCO.
CTF diff	Differentiated output of the Continuous Time Filter, FDP/FDN.
Held Sig Evn	Held signal value for the even interleave of Viterbi Detector.
DV64	Output of the 6-bit divide-by-N counter in the frequency synthesizer.
DV256	Output of the 8-bit divide-by-M counter in the frequency synthesizer.
VGA in	Analog input to the Variable Gain Amplifier of the AGC loop, DIP/DIN.
FSUP	Pump up signal from the phase-frequency detector in the frequency synthesizer.
FSDN	Pump down signal from the phase-frequency detector in the frequency synthesizer.
VGA out	Analog output of the Variable Gain Amplifier of the AGC loop, DOP/DON.
FS VCO	Frequency synthesizer VCO output.

Table 8 Test Signal Descriptions

Test Signal Name	***Description***
TR VCO	Timing recovery VCO output.
Vit Sig O	The odd FIR interleave being input to the Viterbi detector.
MX	FIR mux0 to mux1 transition.
T0	FIR track and hold 0 control signal.
CTF norm	Normal output of the Continuous Time Filter, FNP/FNN.
YHB/YLB	Timing recovery pump up (=0) / down (=1) in sampled mode, qualified by XPB/XNB signal = 1.
XPB/XNB	Timing recovery positive/negative sample sign indicator. Equivalent to (X1 xor X2).
CTF norm ac	AC coupled normal output of the Continuous Time Filter, FAP/FAN.
TRUP	Pump up signal into the charge pump of the Timing recovery loop.
TRDN	Pump down signal into the charge pump of the Timing recovery loop.
Int_ε	Integrated lms tap weight error.
ε_n	Sign of the PR4 equalization error estimate.
C_n	Sign of the Channel data.
Yn-1	Resampled FIR output, one clock cycle before the “current” time.
X1	Positive sample sign indicator for decision directed phase detector in the timing recovery.
XN1	Negative sample sign indicator for decision directed phase detector in the timing recovery.
LP	Signal from the level qualifier block indicating when the input pulse exceeds the programmed threshold.
HCLK	Signal from the level qualifier block which outputs a pulse for each input peak.
LZDEL	One-shot pulse which controls how long the AGC loop stays in low impedance mode. The RLOWZ external resistor controls the one-shot pulse width.
HLDEL	Hold control signal for the AGC loop. Active only in servo mode.
FRDEL	One-shot pulse which controls how long the AGC loop stays in fast acquisition mode. The RFSR external resistor controls the one-shot pulse width.
RGDP	Read gate delayed. Internal control signal which is delayed from RG by two bytes.
dv/dt comp	The CTF differentiated output after passing it through a comparator. Used by the servo block.
AGCN	Internal control signal indicating when the AGC loop switches from acquisition (continuous time) mode to tracking (sampled) mode.
PLLN	Internal control signal indicating when the timing recovery loop switches from decision directed acquisition mode to decision directed tracking mode.
PDSELN	Phase detector select signal. Lo selects the decision directed phase detector, hi selects the phase frequency detector.
DMN	Servo control signal that when hi indicates one of the servo channels is integrating.
SRVCNT	One bit from the servo 2-bit counter which controls servo channel selection sequence.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage

VCC	-0.3V to +7V

Input Voltages

Digital Input Voltage V_{IN}	-0.3V to VCC+0.3V
Analog Input Voltage V_{IN}	-0.3V to VCC+0.3V
Storage Temperature T_{stg}	-65°C to 150°C
Junction Temperature T_J	150°C
Thermal Impedance, Θ_{JA} 64-Lead PQFP	43°C/W

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage

VCC	+5V ± 10%
Junction Temperature T_J	0°C to 125°C

PIN FUNCTION LIST AND DESCRIPTION

There are a number of different input and output buffers used on this chip. There are CMOS TTL inputs, Bipolar ECL-like differential outputs, Analog differential inputs, and several analog reference input and output pins. Because of pin limitations some pins serve double duty. A table showing the various pin types is provided in Table 9 below.

Table 9 VM65014 Pin Descriptions

PIN TYPE	*PIN NAME*	*#*	*INFORMATION*
Power Supplies	VCC1		LPF, servo, analog AGC, analog pulse qualification, analog test mux power
	VCC2		FIR, Viterbi detector, digital test muxes, DSP circuitry power
	VCC3		Frequency synthesizer analog power
	VCC4		Timing recovery analog power
	VCC5		Frequency synthesizer digital, timing recovery digital, write precomp and PECL output power
	VCC6		Front end digital CMOS power and N well.
Ground Supplies	VEE1		LPF, servo, analog AGC, analog pulse qualification, analog test mux ground
	VEE2		FIR, Viterbi detector, digital test muxes, DSP circuitry ground
	VEE3		Frequency synthesizer analog ground
	VEE4		Timing recovery analog ground
	VEE5		Frequency synthesizer digital, timing recovery digital and write precomp ground
	VEE6		Front end digital CMOS ground
	VEE7		Bipolar substrate connection

Table 9 VM65014 Pin Descriptions

PIN TYPE	*PIN NAME*	#	*INFORMATION*
CMOS Inputs	RG		Read Gate. When this signal is asserted, the read path circuitry is enabled. (Active High)
	WG		Write Gate. When this signal is asserted, the write path circuitry is enabled. (Active High)
	SG		Servo Gate. When this signal is asserted, the servo demodulator circuitry is enabled. (Active High)
	SRST		Servo Reset (Active High)
	DEMOD		Enables selected area detector.
	SBF		Sync byte found. Active low. Used in DSP mode to determine when to switch from Viterbi qualified data to DSP sliced data.
	SPEN		Serial port I/O enable (active high)
	SPCLK		Serial port clock (latch on positive edge)
	FREF		Reference frequency for the frequency synthesizer.
	PD		Power down control signal. When this signal is asserted, the chip is powered down. (Active High)
CMOS Outputs	RDS		Level qualifier data output. A high indicates a servo peak of qualified amplitude.
	RPOL		Level qualifier polarity output. A high indicates a positive servo polarity. A lo indicates a negative servo polarity.
Bidirectional CMOS Input/Outputs	SPDATA		Bidirectional serial data port.
External Component Connections	RX		Filter reference resistor. An external 1% resistor is connected from this pin to Analog ground to establish a precise internal reference current for the DACs controlling the continuous-time filter cut-off frequency. Resistor (4kΩ to 32kΩ) to Ground [see equation (eq. 1),]
	RR		PLL reference resistor. An external 1% resistor is connected from this pin to Analog ground to establish a precise internal reference current for the DACs controlling the timing recovery and synthesizer VCO center frequencies. Resistor (2kΩ to 6kΩ) to Ground [see equation (eq. 8),]
	RLOWZ		Low Z duration control. A resistor between this pin and ground defines the duration of the Low Z period.
	RFSR		Fast recovery/decay duration control. A resistor between this pin and ground defines the duration of the fast gain acquisition period.
	CAGCD		AGC Data Field Gain storage, Capacitor (390pF) to Ground
	CAGCS		AGC Servo Field Gain storage, Capacitor (390pF) to Ground
	DSFP DSFN		Timing Recovery PLL loop filter. Differential connections for the timing recovery PLL loop filter component. Capacitor (150pF) between pins.
	FSFP FSFN		Frequency Synthesizer PLL loop filter. Differential connections for the frequency synthesizer PLL loop filter components.

Table 9 VM65014 Pin Descriptions

PIN TYPE	***PIN NAME***	***#***	***INFORMATION***
Analog Differential Inputs	DIP DIN		Analog Read Data input from the preamplifier chip.
Bipolar ECL-like Differential Outputs	WDP WDN		Write data to the preamplifier.
	TP3P TP3N		Test point 3 output
	TP4P TP4N		Test point 4 output
Current Mode Differential Outputs	SRDP SRDN		This is the data output from the Viterbi detector's survival registers.
	SRCP SRCN		Clock synchronized to SRDP/N during read mode or output of the frequency synthesizer during write/idle mode.
Bipolar ECL-like Differential input	FDSP FDSN		Reference frequency used to replace the timing recovery VCO output.
Current Mode Differential input	SWDP SWDN		Scrambled/Encoded write data input to the write precomp/ precoder block.
	SWCP SWCN		Clock synchronized to SWDP/N
Analog Outputs	SREF		Servo Reference Voltage (0.6V)
	SBA		Servo burst A integrator output
	SBB		Servo burst B integrator output
	SBC		Servo burst C integrator output
	SBD		Servo burst D integrator output
	TP1P TP1N		Analog test point 1 output
	TP2P TP2N		Analog test point 2 output

ELECTRICAL PARAMETERS, BY FUNCTIONAL SECTION

AC and DC CHARACTERISTICS
Recommended operating conditions apply unless otherwise specified. 0°C < T_A < 70°C, 4.5V < VCC < 5.5V

OVERALL

Production Tested

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Current	I_{CC}	Read Mode, Data Rate = 55 Mbps		220	275	mA
		Read Mode, Data Rate = 140 Mbps		220	300	mA
		Standby Mode		5	12	mA

Characterization Only

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Recovery Time Standby to Fully Functional	T_{REC}	AGC within 10% final value, Pulse Detector w/o pulse pairing, Filter cutoff within 10% final value			10	µs

Guaranteed By Design

No "Guaranteed By Design" parameters for "Overall".

LOGICAL SIGNALS; ALL DIGITAL PINS

Production Tested

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2.0		VCC + 0.3	V
Input Low Voltage	V_{IL}		–0.3		0.8	V
Input Leakage Current	I_{IL}	V_{IL} = 0.8V			±10	µA
	I_{IH}	V_{IH} = 2.0V			±10	µA
Control Signal Rise and Fall Times	T_{CS}				100	ns

Characterization Only

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance	C_{IN}				10	pF

Guaranteed By Design

No "Guaranteed By Design" parameters for Logical Signals; all digital pins.

GAIN CONTROL

Production Tested

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Input Dynamic Range	V_{DI}	$V_{DI} = (V_{DIP} - V_{DIN})$	20		200	mV_{ppd}
Input Common Mode Voltage	V_{CMDI}	$V_{CMDI} = (V_{DIP} + V_{DIN})/2$	VCC–3.1	VCC-2.7	VCC–2.3	V
Differential Input Resistance	$R_{in(DA)}$	LOWZ = Low	1.2	2.5	3.8	KΩ
		LOWZ = High, WG = 4.0V	120	250	380	Ω
Single Ended Input Resistance	$R_{in(SA)}$	LOWZ = Low	.6	1.25	1.9	KΩ
		LOWZ = High, WG = 4.0V	60	125	190	Ω
VGA Minimum Gain PGC Reg bit = 0	AV_{min}	$AV = (V_{TP2P} - V_{TP2N})/V_{DI}$ V_{CAGCD} = 0.8V, Test Mode 2,		2.4	4.0	V/V
VGA Maximum Gain PGC Reg bit = 0	AV_{max}	$AV = (V_{TP2P} - V_{TP2N})/V_{DI}$ V_{CAGCD} = 3.2V, Test Mode 2,	39	44.5		V/V
VGA Maximum Gain PGC Reg bit = 1	AV_{max}	$AV = (V_{TP2P} - V_{TP2N})/V_{DI}$, TM2				V/V
		DAC = 0000		2.4		
		DAC = 0001		5.2		
		DAC = 0011		10.5		
		DAC = 0111		21.5		
		DAC = 1111		44.5		
Output Common Mode Voltage	V_{CM}	$V_{CM} = (V_{TP2P} + V_{TP2N})/2$ Test Mode 2	VCC–3.2	VCC-2.5	VCC–1.8	V
Output Offset Voltage	V_{OS}	$V_{OS} = (V_{TP2P} - V_{TP2N})$, over entire gain range, Test Mode 2	–50		50	mV

AGC / CHARGE PUMP

Production Tested (unless otherwise specified, RG = 0)

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
RX pin voltage	V_{RX}	R_{ext} = 6kΩ	1.05	1.2	1.35	V
Fast Discharging Current, Continuous Mode	I_{QFD}	V_{FA} = 0.4V				
		SG = 0, DRR = 11111	-2.24	-2.80	-3.36	mA
		SG = 0, DRR = 00000	-1.12	-1.40	-1.68	mA
		SG = 1, DRR = XXXXX	-1.12	-1.40	-1.68	mA
Normal Discharging Current, Continuous Mode	I_{QND}	V_{FA} = 0.3V				
		SG = 0, DRR = 11111	-288	-360	-432	µA
		SG = 0, DRR = 00000	-144	-180	-216	µA
		SG = 1, DRR = XXXXX	-144	-180	-216	µA
Normal Charging Current, Continuous Mode	I_{QNC}	V_{FA} = 0.2V.				
		SG = 0, DRR = 11111	16	20	24	µA
		SG = 0, DRR = 00000	8	10	12	µA
		SG = 1, DRR = XXXXX	8	10	12	µA

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Fast Charging Current, Continuous Mode	I_{QFC}	$V_{FA} = 0.1V$. Enable fast acquisition. TFAQ = 1.				
		SG = 0, DRR = 11111	144	180	236	µA
		SG = 0, DRR = 00000	72	90	118	µA
		SG = 1, DRR = XXXXX	72	90	118	µA
Ultra Fast Charging Current, Continuous Mode	I_{QUFC}	$V_{FA} = 0V$. Enable fast acquisition. TFAQ = 1. WG HI to LO transition.				
		SG = 0, DRR = 11111	2.48	3.10	3.72	mA
		SG = 0, DRR = 00000	1.24	1.55	1.86	mA
		SG = 1, DRR = XXXXX	1.24	1.55	1.86	mA
Charge Pump Currents, Sampled Mode I_{QSX} = 0, 20,40,60µA (as programmed by SQPI DAC)	I_{QSU}	$V_{FA} = 0.270V$. RG = 1.				
		SG = 0, DRR = 11111	$.7 \cdot I_{QSX}$	I_{QSX}	$1.3 \cdot I_{QSX}$	µA
		SG = 0, DRR = 00000	$.35 \cdot I_{QSX}$	$.5 \cdot I_{QSX}$	$.65 \cdot I_{QSX}$	µA
	I_{QSD}	$V_{FA} = 0.450V$ RG = 1.				
		SG = 0, DRR = 11111	$-.7 \cdot I_{QSX}$	$-I_{QSX}$	$-1.3 \cdot I_{QSX}$	µA
		SG = 0, DRR = 00000	$-.35 \cdot I_{QSX}$	$-.5 \cdot I_{QSX}$	$-.65 \cdot I_{QSX}$	µA
High Gain Charge Pump Current, Sampled Mode	I_{QSHU}	V_{FA} = +/- 135mV, $I_{QSX} = 0$. PLLEN = 0, RG transition 0 to 1.				
		SG = 0, DRR = 11111	96	120	144	µA
		SG = 0, DRR = 00000	48	60	72	µA
	I_{QSHD}	V_{FA} = +/- 225mV, $I_{QSX} = 0$. PLLEN = 0, RG transition 0 to 1.				
		SG = 0, DRR = 11111	-96	-120	-144	µA
		SG = 0, DRR = 00000	-48	-60	-72	µA
Charge Pump Leakage Current	I_{LK}	HLD = Active or PGCEN = 1.	−10		10	nA
Output Dynamic Range	V_{FA}	$V_{FA} = (V_{FAP} - V_{FAN})$ $20mV_{ppd} \leq V_{DI} \leq 200mV_{ppd}$ $5MHz < f_{in} < 40MHz$	0.45		.60	V_{ppd}
LOWZ One-shot Pulse Width	PW_{LZ}	LOWZ = Active, $R_{LOWZ} = 10k\Omega$	.28	.35	.42	µs
FSREC One-shot Pulse Width	PW_{LZ}	LOWZ = Active, $R_{FSR} = 20.0k\Omega$	1.2	1.5	1.8	µs

Characterization Only

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Input Capacitance	$C_{in(DA)}$				10	pF
Gain Settle from −30% V_{DI} Step	T_{GD}	$V_{FN} \geq 0.9 \cdot$(final value)		20	25	µs
Gain Settle from +30% V_{DI} Step	T_{GA}	$V_{FN} \leq 1.1 \cdot$(final value)			1.5	µs
Input Referred Noise Voltage	V_{IRN}	gain = AV_{max}, BW = 15MHz $V_{DIP} = V_{DIN}$			10	nV/√Hz
Bandwidth	BW	No AGC action. All gain values.	100			MHz
Common Mode Rejection Ratio	$CMRR_G$	gain = AV_{max}, f_{in} = 5MHz, $V_{DIP} = V_{DIN} = 100mV_{pp}$	40			dB
Power Supply Rejection Ratio	$PSRR_G$	gain = AV_{max}, f_{in} = 5MHz ΔVCC or ΔVEE =$100mV_{pp}$	45			dB
AGC Gain Sensitivity to CAGCx Voltage	AV_{PV}	(Typical range is 1.4V to 2.8V)		17.5		dB/V
Output Distortion	THD	$V_{DI} = 200mV_{ppd}$, $V_{TP2} \leq 0.75V_{ppd}$, Test Mode 2, 1st, 2nd, and 3rd harmonics only			1.0	%

Guaranteed By Design

No "Guaranteed By Design" parameters for Gain Control.

LOW PASS FILTER (7-POLE, 0.05°, EQUIRIPPLE PHASE)

Production Tested (Signals measured at TP2 unless otherwise specified)

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Filter Cutoff Frequency (low end)	f_{Cmin}	Fc_{DAC} = 00h, REXT = 6kΩ	3.15	4.5	5.85	MHz
Filter Cutoff Frequency (middle)	f_{Cmid}	Fc_{DAC} = 40h, REXT = 6kΩ	24.0	26	28.0	MHz
Filter Cutoff Frequency (high end)	f_{Cmax}	Fc_{DAC} = 7Fh, REXT = 6kΩ	45.6	48	50.4	MHz
Normal Lowpass Gain (V_{FN} vs. V_{FI})	AO_N	$BOOST_{DAC}$ = 00h, Fc_{DAC} = 00h, REXT = 6kΩ, f_{in} = 4MHz	-4.2	-3.2	-2.2	dB
Differentiated Lowpass Gain (V_{FD} vs. V_{FN})	AO_D	$BOOST_{DAC}$ = 00h, $f_{in} = 0.67 f_C$	AO_N–5.0	AO_N–3.5	AO_N-2.3	dB
Boost Accuracy	BA		-1		+1	dB
Filter Boost (low end)	AB_{min}	$BOOST_{DAC}$ = 00h, REXT = 6kΩ		0	0.5	dB
Filter Boost (high end)	AB_{max}	$BOOST_{DAC}$ = 1Fh, REXT = 6kΩ	12.0	13.0	14.0	dB
Normal Filter Output Offset	V_{OSFN}	V_{FI} = 0.0V	–200		200	mV
Differentiated Filter Output Offset	V_{OSFD}	V_{FI} = 0.0V, FDP/N outputs	–10		10	mV
AC Coupled Filter Output Offset	V_{OSFA}	V_{FI} = 0.0V, FAP/N outputs	–10		10	mV
Group Delay	T_{GD}	Fc_{DAC} = 7Fh, REXT = 6kΩ	10	12	14	ns
Group Delay Variation (normal or differential), GD = 00h (i.e. symmetric zeros). Measured at Normal Outputs.	T_{GD1}	$0.1 f_C \leq f_{in} \leq 1.5 f_C$, 7 MHz $\leq f_C \leq$ 48 MHz, $BOOST_{DAC}$ = 00h, REXT = 6kΩ	–2.0		2.0	%
	T_{GD2}	$0.1 f_C \leq f_{in} \leq 1.5 f_C$, 7 MHz $\leq f_C \leq$ 48 MHz, $BOOST_{DAC}$ = 1Fh, REXT = 6kΩ	–2.5		2.5	%
Group Delay Variation Nonsymmetric Zeros	T_{GD3}	DC @ FNP/N outputs. GD_{DAC} = -32, relative to GD_{DAC} = 0	–32		-28	%
	T_{GD4}	DC @ FNP/N outputs. GD_{DAC} = +31, relative to GD_{DAC} = 0	28		30	%

Characterization Only

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Normal Output Noise Voltage	V_{NN}	BW = 100MHz, f_C = 30MHz [1] $V_{DIP} = V_{DIN}$, Test Mode 4			<TBD>TBD	mV_{rms}
Differentiated Output Noise Voltage	V_{ND}	BW = 100MHz, f_C = 30MHz [1] $V_{DIP} = V_{DIN}$, Test Mode 4			9.0	mV_{rms}

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Total Harmonic Distortion (V_{FN} or V_{FD} vs. V_{FI})	THD_F	$f_{in} = 0.67 f_C$, Fc_{DAC} = 7Fh, REXT = 6kΩ, $V_{FI} \leq 0.7V_{ppd}$, 2nd, and 3rd harmonics only			1.5	%
Common Mode Rejection Ratio	$CMRR_F$	f_{in} = 5MHz, Fc_{DAC} = 7Fh, REXT = 6kΩ$V_{DIP} = V_{DIN}$ = 100mV_{pp}	40			dB
Power Supply Rejection Ratio	$PSRR_F$	f_{in} = 5MHz, V_{DI} = 0V, ΔVCC or ΔVEE = 100mV_{pp}	40			dB
Filter Settle From Step in Fc and BOOST	T_{FS}	Fc_{DAC} or $BOOST_{DAC}$ step to V_{FN} settle		85	300	ns

[1] Fc_{DAC} = 7Fh, $BOOST_{DAC}$ = 1Fh (boost level is 13dB).

Guaranteed By Design

No "Guaranteed By Design" parameters for the Filter (7-pole, 0.05°, equiripple phase).

READ CHANNEL CIRCUITS

FINITE IMPULSE RESPONSE FILTER

Production Tested

PARAMETER	SYM	CONDITIONS[1]	MIN	TYP	MAX	UNITS
Nom. Center Tap Gain	AV_c	Set bit three in K3 & bits 4 in K2/K4	1.0XX	1.2XX	1.4XX	V/V
Nom. Center Tap off	OFF_c	Set bit three in K3 & bits 4 in K2/K4		5		mV
Feed Through	FTH	Set all taps to 0, clear TC0 & TC1 feed in a.5vp-p low freq. square wave		<TBD>TBD		Vp-p diff
Center Tap Large Signal BW	LSBW	Same as AV_c,with the input being a swept AC signal 0.5vp-p diff[2]		<TBD>TBD		MHz
Center Tap Small Signal BW	SSBW	Same as AV_c,with the input being a swept AC signal 0.05vp-p diff.[2]		<TBD>TBD		MHz
Center Tap K3 Gain & Linearity	OFF_3	Gain with the input code at zero		1.0xx		V/V
	AV_3	K_3 = 11111 bin		1.8xx		V/V
	DNL_3	Differential non-linearity		5		mV/V
	INL_3	Integral non-linearity		19.8		mV/V
Tap K2 & K4 Gain & Linearity	OFF_{24}	Gain with the input code at zero		-.3xx		V/V
	AV_{24}	Gain relative to $AV_3$with the center tap gain set to 0 & K_x = 100000 bin		-0.9xx		V/V
	DNL_{24}	Differential non-linearity		5		mV/V
	INL_{24}	Integral non-linearity		19.8		mV/V
Tap K1 & K5 Gain & Linearity	OFF_{15}	Gain with the input code at zero		0		V/V
	AV_{15}	Gain relative to $AV_3$with the center tap gain set to 0 & K_x = 10000 bin		-0.3xx		V/V
	DNL_{15}	Differential non-linearity		5		mV/V
	INL_{15}	Integral non-linearity		19.8		mV/V
Tap K0 &K6 Gain & Linearity	OFF_{06}	Gain with the input code at zero		0		V/V
	AV_{06}	Gain relative to $AV_3$with the center tap gain set to 0 & K_x = 1000 bin		-0.15x		V/V
	DNL_{06}	Differential non-linearity		5		mV/V
	INL_{06}	Integral non-linearity		19.8		mV/V

[1] The part must be placed in test mode and the ac bypass will be used as an input and the FIR out test points used as outputs. The sample clock is taken from the external clock input and the frequency can be set for convenience.

[2] These test should be done at the highest device clock rate.

Characterization Only

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
DC Offset Variation	OV	DC in = 0 v [1]			<TBD>TBD	mV
Gain Variation	GV	DC in +-0.25 Vdiff [1]			<TBD>TBD	%
Acquisition Alignment	AA	Min. to Max. sample delay variation[1]			<TBD>TBD	ns
TH Droop	DAV	Average droop 0.25 v diff [1]			30	V/µs
	DD	Delta droop max to min [1]			15	V/ns
Center Tap Distortion	$MX2^{nd}$	Set the input to 0.5vp-pdiff @ 31/ 128*F_S with F_S set to max data rate CT only [1]			-35	dBc
	$MX3^{rd}$				-35	dBc
	MXTHD				-30	dBc
Max EQ Distortion	$MX2^{nd}$	Same as center tap distribution. with amplitude set to 0.17vp-pdiff. Max peaking [2]			-35	dBc
	$MX3^{rd}$				-35	dBc
	MXTHD				-30	dBc
Noise	η_{CT}	CT only [1]				Vrmsd/ $\sqrt{Hz}$
	η_{MX}	Max peaking [2]				Vrmsd/ $\sqrt{Hz}$
2T Boost at $F_S/4$ [3]	MXB_{2T}	K2 & K4 set to 32, Vin = 0.1 Vp-p diff, K3 = 8			1.91	V/V
	MNB_{2T}	K2 & K4 set to 31, vin = 0.1 Vp-p diff, K3 = 8	-.6			V/V
2T Boost at $F_S/4$ [1,3]	MXB_{2T}	K1 & K5 set to 16			0.64	V/V
	MNB_{2T}	K1 & K5 set to 15	-.6			V/V
6T Boost at $F_S/4$ [1,3]	MXB_{6T}	K0 & K6 set to 8			0.32	V/V
	MNB_{6T}	K0 & K6 set to 7	-0.28			V/V

[1] Set taps K3 = 8 & K2/K4 = 16 and clear all others
[2] Set taps K3 = 31, K2/4 = 32, K1/5 = 16, & K0/6 = 8
[3] Relative to the nominal center tap gain

Guaranteed By Design

No "Guaranteed By Design" parameters for the Finite Impulse Response Filter.

VITERBI DETECTOR

Production Tested

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Viterbi Threshold Test		Apply 4T signal with 400mVp-p at Viterbi input. Within this signal, include a pulse with 180mV positive peak and -380mV negative peak.				
	VITMIN	Step the Viterbi Threshold DAC until zeros first start to appear on the Viterbi outputs. Record value.	<TBD>TBD	43	TBD	
	VITTH	Continue to step the Viterbi Threshold DAC until the four zero bits are stable on the Viterbi output.	TBD	45	TBD	

Characterization Only

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
PLLP 0-to-1 Transition to Path Memory Set Released.		Read mode			75	ns
Viterbi DAC Differential Nonlinearity					1	LSB

Guaranteed By Design

No "Guaranteed By Design" parameters for the Viterbi detector.

DETECTING SERVO DEMODULATOR

Production Tested

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Servo Input Frequency	f_{INS}		4		13.5	MHz
Gain $[(V_{SVO}-V_{SVR})/V_{LQ}]$	AV_S	measured over 1/4 to 3/4 of scale [4]		<TBD>TBD		V/V
Linearity of V_{FN} vs. V_{DI}	V_{FL}	measured over 1/8 to 7/8 of scale [6]	−0.5		0.5	%
Linearity of $V_{SVO}-V_{SVR}$ vs. V_{DI}	V_{DL1}	measured over 1/8 to 3/4 of scale [6]	−1.4		1.4	%
	V_{DL2}	measured over 3/4 to 7/8 of scale [6]	−4.5		4.5	%
Output Offset (not referred to input)	V_{SO}	intercept of regressed line [6]	−40		40	mV
Output for Zero Input	V_{ZI}	6	0	30	60	mV
Channel A, B, C & D Mismatch	V_{MM}	Variation for a common input % of full scale			±1.0	%
SREF Voltage	V_{SR}		3.50	3.60	3.70	V
Integrating Cap Decay Rate	V_{DR}	0.1% of full scale droop in 50µs			40	V/sec

[4] This specification is the slope of the characteristic ratio of a DC voltage to a peak to peak voltage.
[5] V_{DIL} and V_{DIH} specify the input range over which all other specifications must be met.
[6] In addition to the linearity and offset specifications, the output must also be guaranteed monotonic.
[7] Refer to waveshapes below for this specification.

Characterization Only

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Channel to Channel Cross Talk	V_{CT}	Effect of A on B etc. % of full scale			±0.5	%
Output Impedance	R_{SO}	SREF and SRVOUT pins			50	Ω
Demodulator Repeatability (52dB)	N_{DR}	Repeatability without external noise			±5.0	mV
Power Supply Rejection Ratio	$PSRR_S$	f_{in} = 5MHz, V_{DI} = 0V, ΔV_{CC} or ΔV_{EE} = 100mV$_{pp}$ [8]	25			dB
Common Mode Rejection Ratio	$CMRR_S$	$0\text{MHz} \leq f_{in} \leq 1\text{MHz}$ $V_{LQP} = V_{LQN}$ = 100mV$_{pp}$ [8]	25			dB
Total System Gain Variation $[(V_{SVO}-V_{SVR})/V_{DI}]$	AV_A	over all V_{DI}, 1/4 to 3/4 of scale [4]		<TBD>TBD		V/V

[4] This specification is the slope of the characteristic ratio of a DC voltage to a peak to peak voltage.
[8] The required demodulator output Signal-to-Noise Ratio (SNR) due to external noise is 49dB.

TIMING PARAMETERS

AC CHARACTERISTICS
Recommended operating conditions apply unless otherwise specified. 0˚C < T_A < 70˚C, 4.5V < VCC < 5.5V

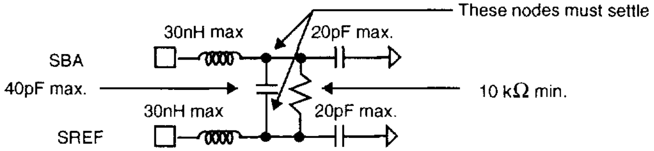
SERVO DEMODULATOR TIMING

Production Tested

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
SRST Pulse Width	T_{SR}		600			ns
[9] Load condition for SBA, SBB, SBC, SBD, and SRVREF given below.						

Characterization Only

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
DEMOD Pulse Width	T_{DMD}		150			ns
DEMOD Recovery Time	T_{REC}		150			ns
DEMOD to Corresponding Select Clock Delay	T_{DS}		0			ns
Trailing Edge SRST to SBA-SBD Reset Delay	T_R	0.25% of final value [9]	150			ns
Trailing Edge SRST to DEMOD Recovery	T_{RR}		100			ns
[9] Load condition for SRV and SREF given below.						



Guaranteed By Design

No "Guaranteed By Design" parameters for Demodulator Timing.

SYSTEM TIMING

Pins: SG, DEMOD

Production Tested

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
FSREC Leading Edge to V_{FN} Stable	T_{FD}	V_{FN} stable within 10%			2.3	µs
Trailing Edge of LOWZ to V_{FN} Stable to 10%	T_{WR}	CAGCD value correct			500	ns
Lead, Trailing Edge SG to V_{FN} stable 10%	T_{GS}	CAGCS or D value correct			500	ns

Guaranteed By Design

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
WG Pulse Width (given for reference only)	T_{WG}		1.6			µs

Guaranteed by Design

No “Guaranteed By Design” parameters for System Timing.

FREQUENCY SYNTHESIZER

Production Tested

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
VCO Frequency	f_{VCO}	$X = f_{0(VCO)} \cdot (1+k_v \cdot (V_{fsfp} - V_{fsfn}))$				MHz
		Guaranteed Range	53		160	MHz
VCO Center Frequency	$f_{0(VCO)}$	$X = k_f \cdot I_{REF} \cdot (33+K_{fsf})$	$0.90 \cdot X$		$1.10 \cdot X$	MHz
VCO Gain	k_v	measured at SRCP/N	0.30		0.40	V^{-1}
VCO Dynamic Range	$f_{dr(VCO)}$	$V_{fsfp} = V_{fsfn}$, $K_{fsf} = 0$ to 32	± 2			% / LSB
RR Voltage	V_{rr}		1.20	1.28	1.36	V
FSFP Voltage	V_{fsfp}		$V_{fsfn} - 1.0$		$V_{fsfn} + 1.0$	V
FSFN Voltage	V_{fsfn}		2.10	2.35	2.60	V
FSFILT Leakage Current	$I_{Lfsfilt}$				± 300	nA
FS Charge Pump Current	I_{fsqp}	$X = I_{REF}(0.5+((31-K_{fsf})/62))$	$0.90 \cdot X$		$1.10 \cdot X$	μA
		Guaranteed Range	100		700	μA

k_f is 5.05 MHz/mA

K_{fsf} is the value of the Data Rate DAC word, [0 to31]

I_{REF} is the reference current being sunk from pin RR in μA, $I_{REF} = V_{rr}/R_{ext}$

Characterization Only

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Closed Loop Jitter	σ_F	VCO output, sample size = 100,000 samples		100		ps

Guaranteed by Design

No "Guaranteed By Design" parameters for the Frequency Synthesizer.

TIMING RECOVERY

Production Tested

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
TRVCO Frequency	f_{TRVCO}	$X = f_{0(TRVCO)} \cdot (1+k_v \cdot (V_{dsfp} - V_{dsfn}))$ DAMP DAC = 127	53		160	MHz
TRVCO Center Frequency	$f_{0(TRVCO)}$	$X = k_I \cdot I_{REF} \cdot (33+K_{fsf})$, DAMP DAC = 127	0.90·X		1.10·X	MHz
TRVCO Gain	k_v	measured at TP4P/N, DAMP DAC = 127	0.35		0.45	V^{-1}
TRVCO Dynamic Range	$f_{dr(TRVCO)}$	$V_{dsfp} = V_{dsfn}$, K_{fsf} = 0 to 32	± 2			% / LSB
DSFP/N CM Voltage	V_{CM}		1.80	2.10	2.40	V
TR Charge Pump Gain (I_{QP}/*Timing Error)*	I_{TRQP}	Idle/Acquisition Mode	322	460	598	µA/V
		Tracking Mode: TRGAIN = 0 TRGAIN = 1	18 81	26 115	34 150	µA/V µA/V
Pmult Gain (TRVCO Cntl/Tmg Err.)	k_{PMULT}	$X = 0.35((127-K_{pmult})/127)$: Idle/Acq. $X = 0.088((127-K_{pmult})/127)$: Trck, TRGAIN = 0 $X = 0.175((127-K_{pmult})/127)$: Trck,TRGAIN = 1. DSFP = DSFN, DR DAC = 0	-20		+20	%

k_I is 3.98MHz/mA
K_{fsf} *is the value of the Data Rate DAC word, [0 to31]*
K_{pmult} is the value of the Damping Ratio DAC word, [0 to127]
I_{REF} is the reference current being sunk from pin RR in µA, $I_{REF}=V_{rr}/R_{ext}$

Characterization Only

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Closed Loop Jitter	σ_F	TRVCO output, sample size=100,000 samples		100		ps

Guaranteed by Design

No "Guaranteed By Design" parameters for Timing Recovery.

WRITE PRECOMPENSATION

Production Tested

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
WPC Resolution (absolute max)	T_{pc}	X = (0.04·T)/16 for patterns 1&3 X = (0.02·T)/16 for pattern 2	0.9·X		1.1·X	ns
WPC Delay	T_{wpc}	X = (0.013·K_{wp}+0.20·WPCHR)·T 1&3 X = 0.013·K_{wp}·T Pattern 2	0.9·X		1.1·X	ns
T is the period of the VCO clock WPCHR is the WPC high range bit in serial register K_{wp} is value of the write precompensation DAC word [0 to 15]						

Characterization Only

No "Characterization Only" parameters for Write Precompensation.

Guaranteed by Design

No "Guaranteed By Design" parameters for Write Precompensation.

SERIAL INTERFACE TIMING

Production Tested

PARAMETER	SYM		MIN	TYP	MAX	UNITS
SPCLK period	T		50			ns
SPEN set-up time	$T_{S(SPEN)}$	Relative to SPCLK ↑	40			ns
SPEN hold time	$T_{H(SPEN)}$	Relative to SPCLK ↑	50			ns
SPDATA set-up time	$T_{S(SPDATA)}$	Relative to SPCLK ↑	20			ns
SPDATA hold time	$T_{H(SPDATA)}$	Relative to SPCLK ↑	5			ns
SPDATA enable	T_{OEN}	Relative to SPCLK ↓	5			ns
SPCLK low time	T_{OCLK}	Relative to SPCLK ↓	30			ns
SPDATA disable	T_{ODIS}	Relative to SPEN ↓			30	ns
Delay to SPDATA output data change	T_{PDD}	Relative to SPCLK ↑			10	ns

Characterization Only

PARAMETER	SYM		MIN	TYP	MAX	UNITS
SPEN high to low to high (Time between successive operations)	T		50			ns

Guaranteed by Design

No "Guaranteed By Design" parameters for Serial Interface Timing.