TOSHIBA BiCMOS Integrated Circuit Silicon Monolithic

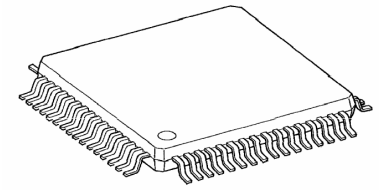
TB1328FG

Audio SW, Video SW, Sync Separation and H/V Frequency Counter IC for TVs

The TB1328FG includes Audio and video SW blocks, pre-filters for AD converter, sync separations and an H/V format detector for TV signals.

The TB1328FG contributes to a reduction in the proportion of PCB occupied by LCR filters and to the simplification of designs in analog interfaces.

The TB1328FG is equipped with an I^2CBUS interface through which various functions can be controlled.



LQFP64-P-1010-0.50A

Weight: 0.34 g (typ.)

Features

AUDIO SW BLOCK
- Audio (L/R) inputs: 8 channels
- Audio (L/R) output: 2 channels

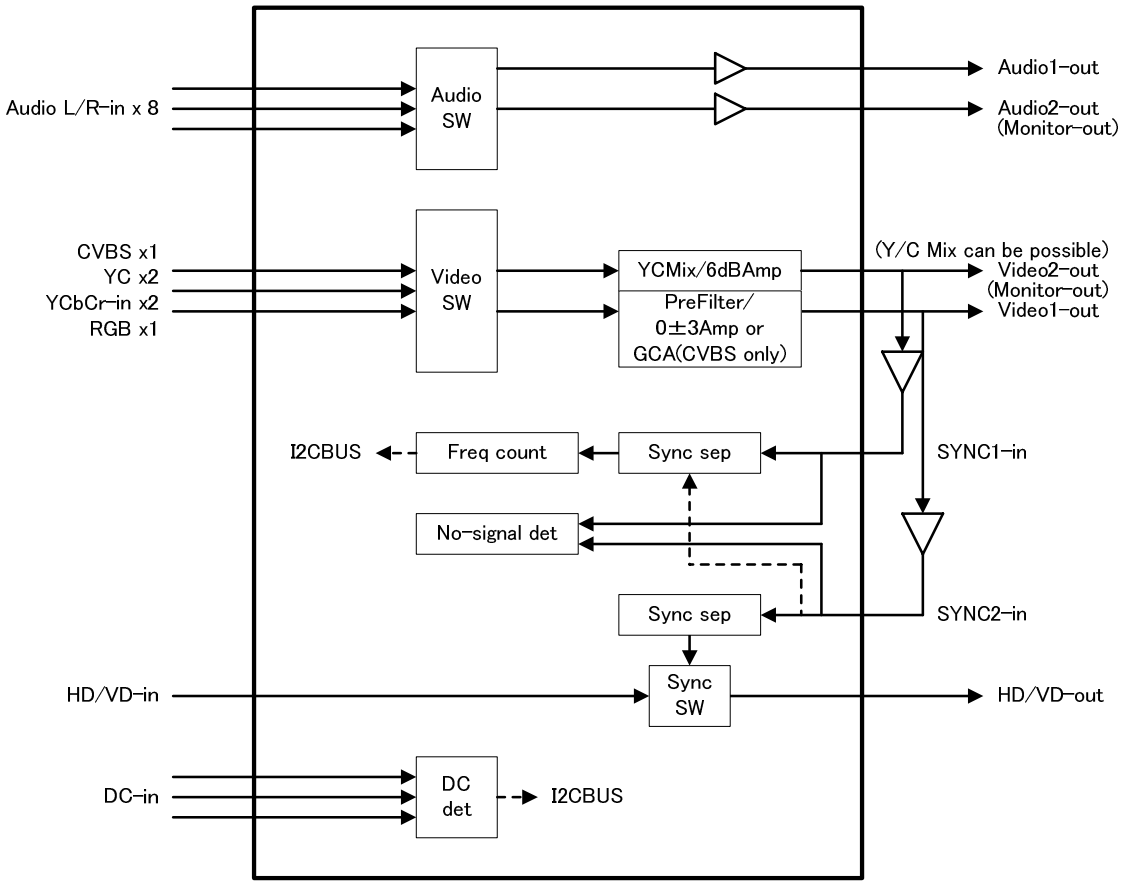
VIDEO SW BLOCK
- CVBS inputs
- Y/C inputs
- Component video inputs (co-use as RGB inputs)
- Output: 1 channel (Y/CVBS/G,C/Cb/B,Cr/R)
- Monitor output (SY/Y/C/CVBS)

VIDEO BLOCK
- Gain switching: -3 dB / 0 dB / +3 dB(Output: 1 channel)
- GCA-Amp for only CVBS: 4 to –6dB,6bit(Output: 1 channel)
- Bandwidth filter: pre-filter for ADC; 5 to 46 MHz variable(Output: 1 channel)
- +6dB Amp, No pre-filter (Monitor output)

SYNC SEPARATION BLOCK
- Supports 525/30p/60i/60p, 625/50i/50p, 750/50p/60p, 1125/24p/24sf/25p/30p/50i/60i/50p/60p, 1250/50i, VGA@60, SVGA@60, XGA@60, SXGA@60, UXGA@60
- HD/VD input: 1 channel; positive and negative input acceptable
- HD/VD output: positive and negative output selectable
- Masking pseudo-sync for copyguard signal

OTHERS
- Line detector for Japanese D-pin
- S2, S1, insertion detection for S-pin
- Horizontal and vertical frequency counter
- Input signal format detection circuit
- No-input detection
- Automatic sync process switching mode
- Programmable number of video inputs

Block Diagram 1 (simplified complete diagram)

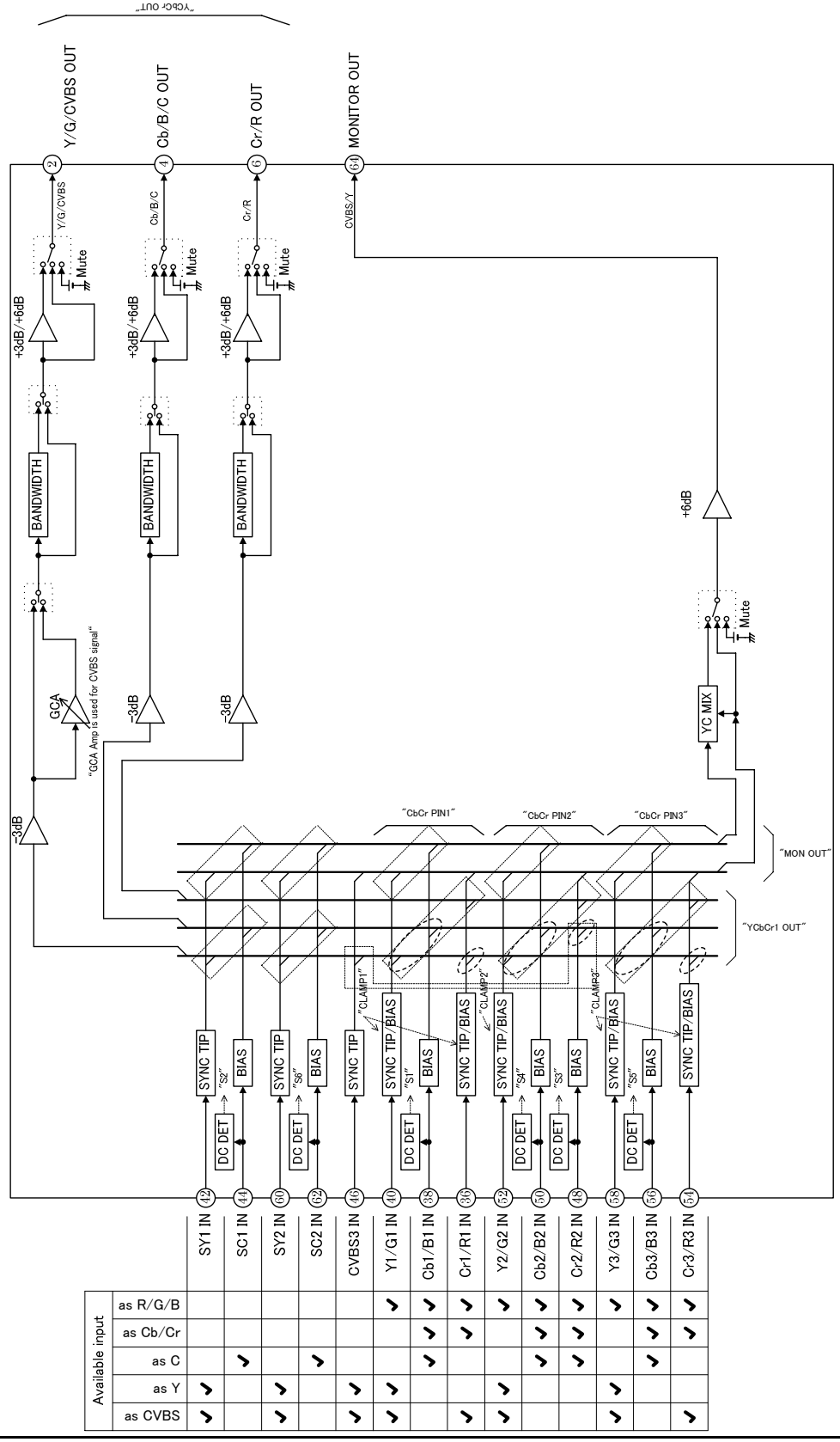


This IC will not function with non-standard signals such as weak signals, ghost signals, etc.

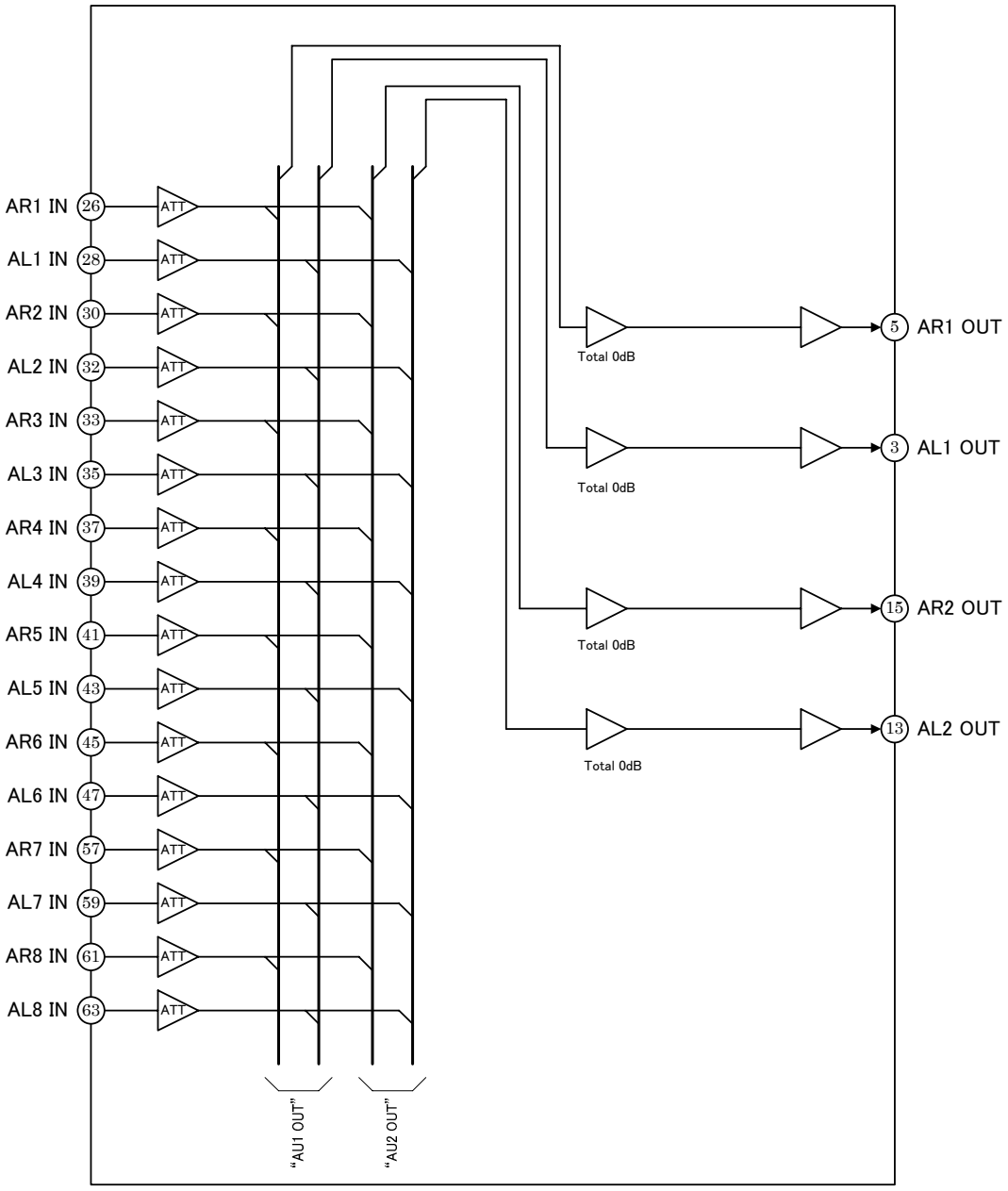
Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

Block Diagram 2 (Video block)

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

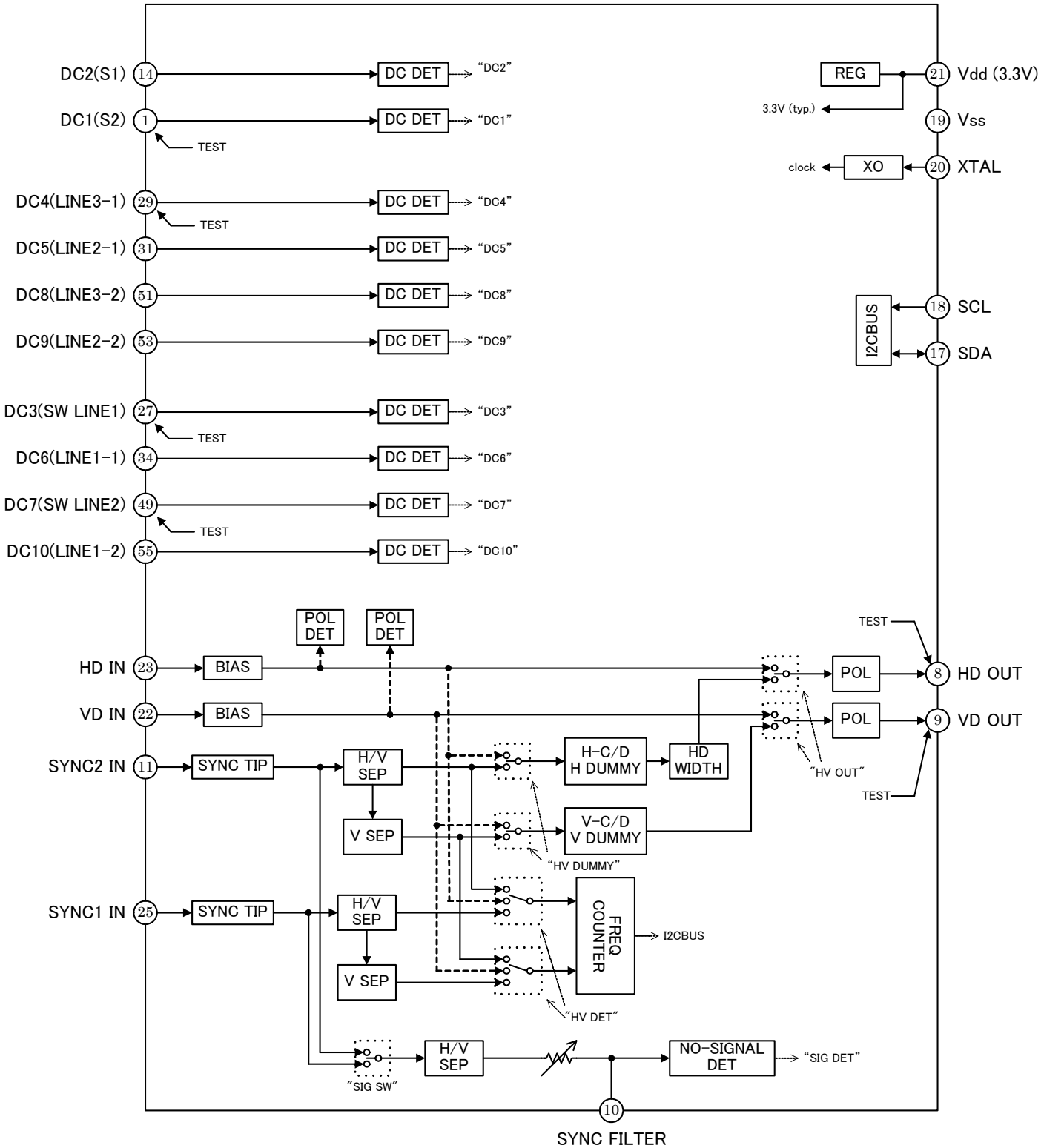


Block Diagram 3 (Audio block)



Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

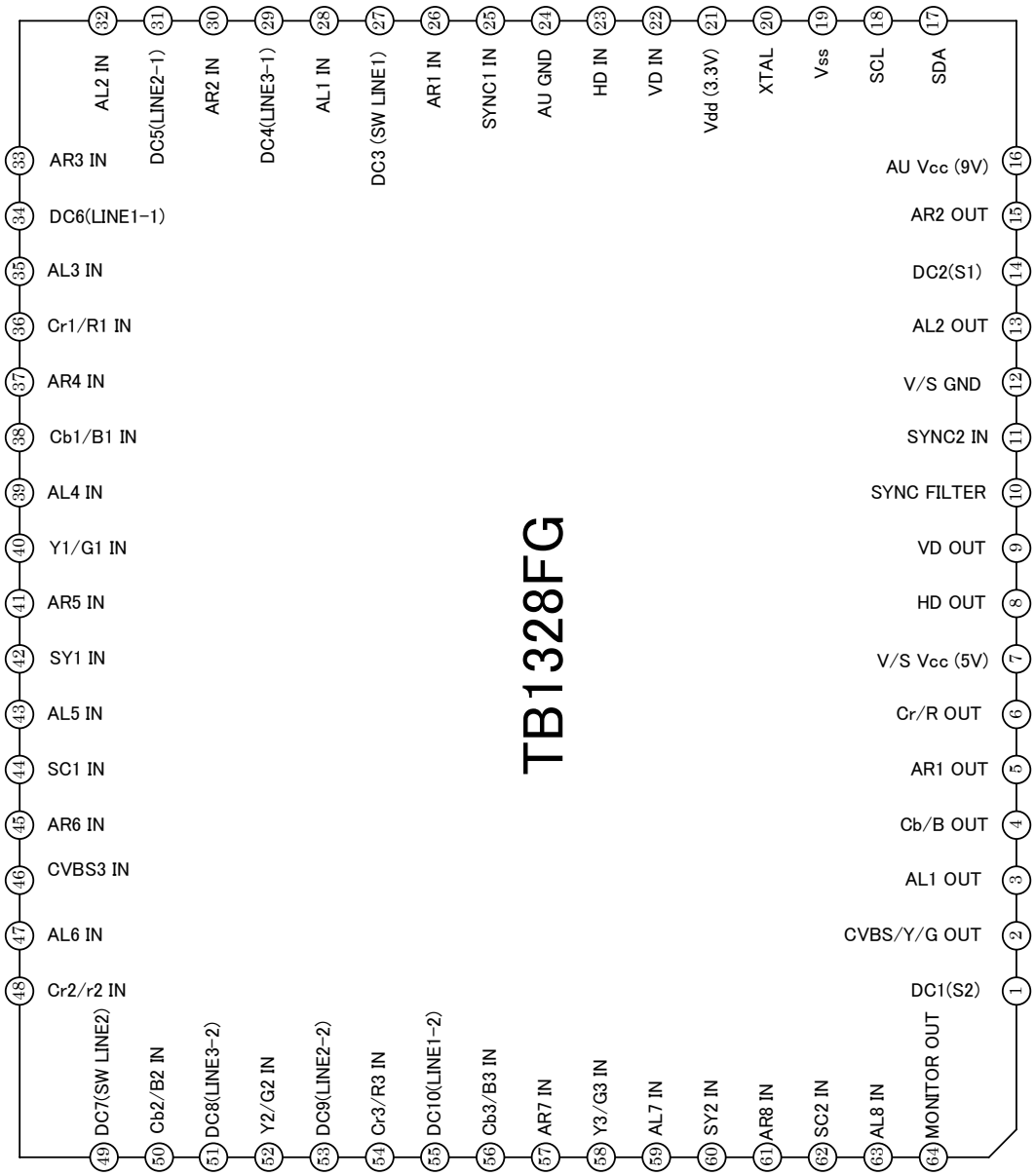
Block Diagram 4 (Other blocks)



This IC will not function with non-standard signals such as weak signals, ghost signals, etc.

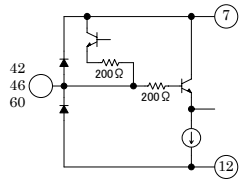
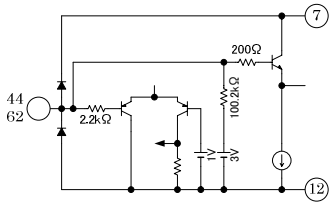
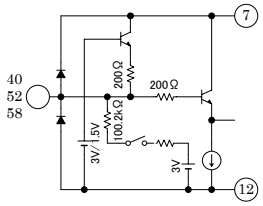
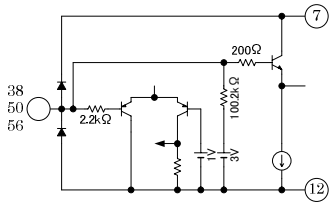
Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

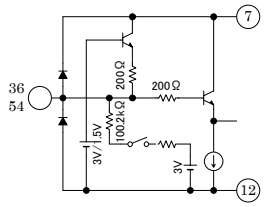
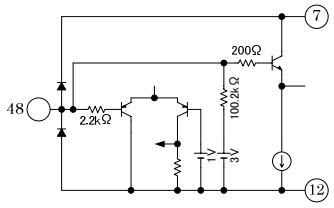
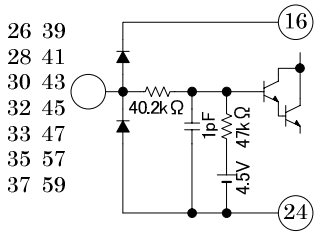
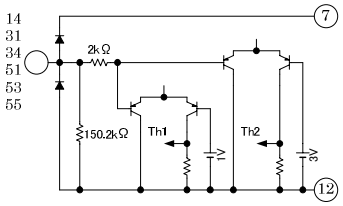
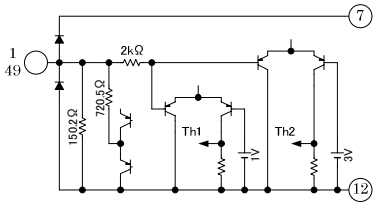
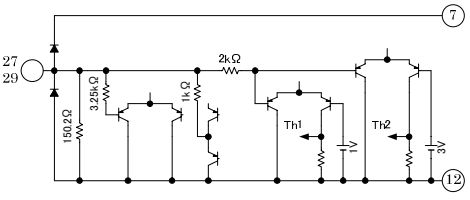
Pin Assignment

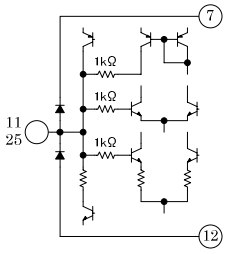
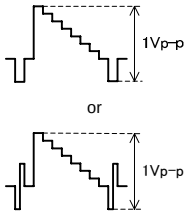
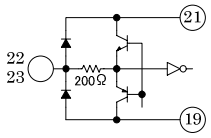
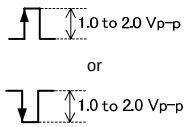
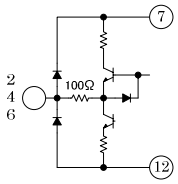
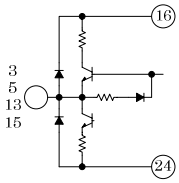
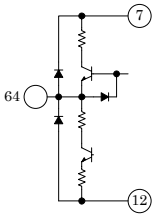
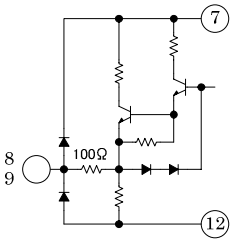
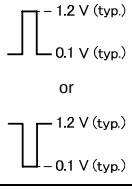
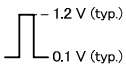
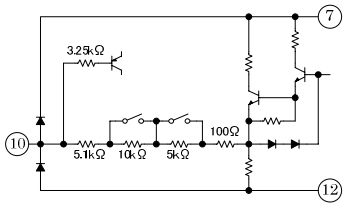


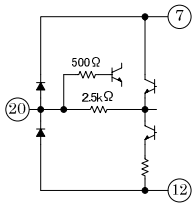
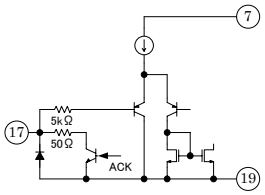
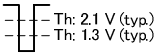
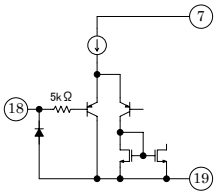
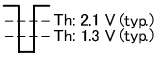
Pin Functions

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

Pin No.	Pin Name	Function	Interface Circuit	Input Signal/Output Signal
21	V_{dd} (3.3 V)	V_{CC} pin for the logical circuits. Supply power through a resistor from pin 11 as in the Application Circuit. This pin voltage is clipped to 3.3 V (typ.) by the internal regulator.		3.3 V (typ.)
19	Vss	GND pin for the logical circuits.	–	–
7	V/S V_{CC} (5 V)	V_{CC} pin for the sync and video circuits. Connect 5.0 V (typ.)	–	5.0 V (typ.)
12	V/S GND	GND pin for the sync and video circuits.	–	–
16	AU V_{CC} (9 V)	V_{CC} pin for the audio circuits. Connect 9.0 V (typ.)	–	9.0 V (typ.)
24	AU GND	GND pin for the audio circuits.	–	–
42 46 60	SY1 IN CVBS3 IN SY2 IN	CVBS or Y input pin. Input the CVBS or Y signal in NTSC, PAL or SECAM via a clamp capacitor.		Sync tip level: 2.3 V (typ.) Y/CVBS signal amplitude: 1.0 Vp-p (with sync)
44 62	SC1 IN SC2 IN	Chroma signal input pin. Input C signal via a capacitor. This pin's voltage is detected and the status is returned to I^2CBUS Read functions S2 or S6. It is used for detecting whether S-pin is connected or not.		2.9 V bias (typ.) Burst signal amplitude: 0.3 Vp-p
40 52 58	Y1/G1 IN Y2/G2 IN Y3/G3 IN	Y, G or CVBS input pin. Input the signal via a clamp capacitor. The clamp system is selectable by CLAMP1, 2 or 3 registers.		Sync tip level: 2.3 V (typ.) Bias level: 2.9 V (typ.) Y/G/CVBS signal amplitude: 1.0 Vp-p (with sync)
38 50 56	Cb1/B1 IN Cb2/B2 IN Cb3/B3 IN	Cb, B or C input pin. Input the signal via a capacitor.		2.9 V bias (typ.) Cb/B signal amplitude: 0.7 Vp-p (without sync) Burst signal amplitude: 0.3 Vp-p

Pin No.	Pin Name	Function	Interface Circuit	Input Signal/Output Signal
36 54	Cr1/R1 IN Cr3/R3 IN	Cr, R or CVBS input pin. Input the signal via a capacitor.		Sync tip level: 2.3 V (typ.) Bias level: 2.9 V (typ.) Cr/R signal amplitude: 0.7 Vp-p (without sync) CVBS/Y signal amplitude: 1.0 Vp-p (with sync)
48	Cr2/R2 IN	Cr, R or C input pin. Input the signal via a capacitor.		2.9 V bias (typ.) Cr/R signal amplitude: 0.7 Vp-p (without sync) Burst signal amplitude: 0.3 Vp-p
26 28 30 32 33 35 37 39 41 43 45 47 57 59 61 63	AR1 IN AL1 IN AR2 IN AL2 IN AR3 IN AL3 IN AR4 IN AL4 IN AR5 IN AL5 IN AR6 IN AL6 IN AR7 IN AL7 IN AR8 IN AL8 IN	Audio input pin. Input the signal via a resistor and a capacitor. When the resistor value is 5.6 kΩ, the internal gain becomes 0 dB (typ.).		Bias level: 4.4 V (typ.) Audio input: 2.8 V p-p (100%)
14 31 34 51 53 55	DC2(S1) DC5(LINE2-1) DC6(LINE1-1) DC8(LINE3-2) DC9(LINE2-2) DC10(LINE1-2)	DC voltage input. Input the signal via a resistor for protection purposes.		
1 49	DC1(S2) DC7(SW LINE2)	DC voltage input. Input the signal via a resistor for protection purposes. This pin is also used as test signal output pin for shipping only.		
27 29	DC3(SW LINE1) DC4(LINE3-1)	DC voltage input. Input the signal via a resistor for protection purposes. This pin is also used as test signal output pin for shipping only.		

Pin No.	Pin Name	Function	Interface Circuit	Input Signal/Output Signal
11 25	SYNC IN 2 SYNC IN 1	Composite SYNC input pin to separate into H- and V-SYNC. Input the signal via a clamp capacitor. Remark: SYNC1 IN is not available when A-SYNC = 1 (ON).		Sync tip level: 1.8 V (typ.) 
23 22	HD IN VD IN	HD or VD input pin. Input a separated horizontal or vertical sync signal (1.0 to 2.0 Vp-p) via a resistor and a coupling capacitor. The polarity of the input signal is detected and its leading edge becomes a timing trigger.		1.45 V bias (typ.) 
2 4 6	CVBS/Y/GOUT Cb/B OUT Cr/R OUT	Video signal output pin. Refer to Bus Control Functions for the output from each pin.		AC: -3, 0 or +3 dB (typ.)
3 5 13 15	AL1 OUT AR1 OUT AL2 OUT AR2 OUT	Audio signal output pin. Refer to Bus Control Functions for the output from each pin.		
64	MONITOR OUT	Video signal output pin for a monitor output. Refer to Bus Control Functions for the output from the pin.		AC: +6 dB (typ.)
8 9	HD OUT VD OUT	HD or VD output pin. The polarity of the output is selectable by HV-POL register. The tailing edge of the VD-OUT has a jitter. Use the leading edge only.		 
10	SYNC FILTER	A filter pin for sync detection. Connect a capacitor between this pin and GND.		–

Pin No.	Pin Name	Function	Interface Circuit	Input Signal/Output Signal
20	XTAL	Crystal connection pin. Connect a 3.579545 MHz crystal for NTSC demodulation to generate internal clocks.		–
17	SDA	SDA pin for I²CBUS.		 H to L: 1.3 V (typ.) L to H: 2.1 V (typ.)
18	SCL	SCL pin for I²CBUS.		 H to L: 1.3 V (typ.) L to H: 2.1 V (typ.)

BUS Control Map

Write Mode Slave address: DE_H

SA	D7	D6	D5	D4	D3	D2	D1	D0	PRESET
00	(0)	(0)	(0)	fc HALF	YCbCrOUT				00000000
01	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	00000000
02	(0)	(0)	FILPASS	YC MIX	MON OUT				00000000
03	f0 SW	BANDWIDTH1							00000000
04	GCA V timing	GCA SW	GCA GAIN(D5～D0)						00000000
05	(0)	(0)	(0)	(0)	CVBS/YGAIN		CbCr GAIN		00000000
06	(0)	CbCr PIN3	CbCr PIN2	CbCr PIN1	(0)	CLAMP3	CLAMP2	CLAMP1	00000000
07	(00000000)TEST0								00000000
08	AU2 OUT				AU1 OUT				00010001
09	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	00000000
0A	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	00000000
0B	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	00000001
0C	HV-SEP2		HV-SEP1		(0)	(0)	SYNC LPF2	SYNC LPF1	00000000
0D	A-SYNC	SIG LPF	(0)	(0)	(0)	(0)	(0)	(0)	00000000
0E	(0)	PS MASK	V-DET	HD WIDTH	HV POL	(0)	HV DET	HV OUT	00000000
0F	H DMY	V DMY	(0)	HV FREQ2					00000000
10	H COUNT MAX				(0)	H COUNT MIN			00000000
11	SIG DET N				SIG RESET N				00000000
12	(0)TEST1	(0)	SIG RESET	SIG SW	SIG DET IMPE		SIG DET LVL		00000000
13	(00000000)TEST2								00000000
14	(00000000)TEST3								00000000

NOTE:To activate GCA V timing without V separation (input V sync signal to SYNC2 IN(11 pin)), set D7=1(SA 12H,13H 14H). After changing GCA SW, GCA gain, set D7=0(SA:12H,13H, 14H).

Read Mode Slave address: DF_H

	D7	D6	D5	D4	D3	D2	D1	D0
0	POR	H FM2	V FM2	H IN	V IN	V-SYNC-W	HD-POL	VD-POL
1	H FORMAT				V FORMAT			*
2	*	*	SIG DET	HV-OUT FORMAT				
3	DC4（29Pin）		DC3(27Pin)		DC2(14PIN)		DC1(1PIN)	
4	DC8(51Pin)		DC7(49Pin)		DC6(34Pin)		DC5(31Pin)	
5	*	*	*	*	DC10(55Pin)		DC9(53Pin)	
6	S6(62Pin) SC2in	S5(56Pin) Cb3in	S4(50Pin) Cb2in	S3(48Pin) Cr2in	S2(44Pin) SC1in	S1(38Pin) Cb1in	*	*
7	H FREQ DET							
8	V FREQ DET							

*: Undefined

Bus Control Functions

Write Mode

Register Name	Function	Preset Value
fc HALF	Switches the frequency of bandwidth limit filters for Cb/Cr The cutoff frequency of bandwidth limit filters for Cb/Cr is 1/2 to Y. 0: OFF (same for 3 outputs) 1: ON (1/2 fc for Cb/Cr)	OFF (0)
YCbCrOUT	Selects the output form Y/Cb/Cr OUT (pins 2,4,6). (Y OUT, Cb OUT, Cr OUT)= 0000: Mute (mute, mute, mute) 0001: SY1 (pin 42), SC1 (pin 44), mute 0010: SY2 (pin 60), SC2 (pin 62), mute 0011~0101: Not available 0110: CVBS3 (pin 46), mute, mute 0111: Y1 (pin 40), Cb1 (pin 38), Cr1 (pin 36) (mute, when CbCr PIN1=1) 1000: Y2 (pin 52), Cb2 (pin 50), Cr2 (pin 48) (mute, when CbCr PIN2=1) 1001: Y3 (pin 58), Cb3 (pin 56), Cr3 (pin 54) (mute, when CbCr PIN3=1) 1010: Not available 1011: Cr1(as CVBS) (pin 36), mute, mute(when CbCr PIN1=1) 1100: Cr3(as CVBS) (pin 54), mute, mute(when CbCr PIN3=1) 1101 ~ 1111: Not available Refer also to Function Descriptions.	Mute (0000)
FILPASS	Switches the bandwidth limit filter. 0: OFF (filters active) 1: ON (bypass)	OFF (0)
YC MIX	Mixes Y with C for MONITOR OUT (pin64). 0: OFF (for CVBS) 1: MIX (Y+C)	OFF (0)
MONITOR OUT	Selects the output form MONITOR OUT (pin 64) . When YC MIX=1, a mixed signal is outputted. 0000: Mute 0001: SY1 (pin 42) (+SC1 (pin 44)) 0010: SY2 (pin 60) (+SC2 (pin 62)) 0011~0101: Not available 0110: CVBS3 (pin 46) (+Cr2 (pin 48), when CbCr PIN2=1) 0111: Y1 (pin 40) (+Cb1 (pin 38)) 1000: Y2 (pin 52) (+Cb2 (pin50)) 1001: Y3 (pin 58) (+Cb3 (pin 56)) 1010: Not available 1011: Cr1((CVBS) (pin 36),when CbCr PIN1=1) 1100: Cr3((CVBS) (pin 54) when CbCr PIN3=1) 1101 ~ 1111: Not available Refer also to Function Descriptions.	Mute (0000)
f0 SW	Switches the f0 of bandwidth limit filter for YCbCr(RGB) 0: LOW 1: HIGH	LOW (0)
BANDWIDTH	Switches the f0 of bandwidth limit filter for YCbCr(RGB) and CVBS output form Y/Cb/Cr OUT (pins 2,4,6) 0000000: MIN (low) 1111111: MAX (high)	MIN (0000000)
GCA V timing	0: GCA V timing OFF 1:GCA V timing ON	0: GCA V timing OFF
GCA SW	0: GCA OFF 1:GCA ON	0: GCA OFF
GCA Gain	000000: Gain MAX (high) 111111: Gain MIN (low)	Max (000000)

NOTE: If GCA SW is GCA OFF, set GCA Gain to minimum.

After setting D7=1(SA:04H,12H,13H,14H) and GCA Gain to MIN(3FH), set D7=0(SA:04H,12H,13H,14H).

Register Name	Function	Preset Value
CVBS / Y GAIN	Switches output gain. Gain of CVBS / Y / G OUT outputs (pins 2) is controlled. 00: 0dB 01: -3dB 10: +3dB 11: Not available Remark: GAIN = 01 (-3dB) is recommended for the 1125/50p/60p format since this offers superior frequency characteristics to those of other modes.	
CbCr GAIN	Switches output gain. Gain of CbCr(B/R) OUT outputs (pins 4,6) is controlled. 00: 0dB 01: -3dB 10: +3dB 11: Not available Remark: GAIN = 01 (-3dB) is recommended for the 1125/50p/60p format since this offers superior frequency characteristics to those of other modes.	0dB (00)
CbCr PIN1	Changes CbCr1-IN pins function. 0: Component Cb/Cr input (pin 40: Y/G, pin 38: Cb/B, pin 36: Cr/R) 1: Separated C and CVBS input (pin 40: Y, pin 38: C, pin 36: CVBS) * If "1: Separated C and CVBS input" is selected for CbCr PIN1, then CLAMP1 mode is set for "SYNC TIP CLAMP (for CVBS/Y) & SYNC TIP CLAMP (for CVBS)"	Cb/Cr input (0)
CbCr PIN2	Changes CbCr2-IN pins function. 0: Component Cb/Cr input (pin 52: Y/G, pin 50: Cb/B, pin 48: Cr/R, pin 46: CVBS) 1: Separated C input (pin 52: Y, pin 50: C, pin 48:C,pin 46: Y)	Cb/Cr input (0)
CbCr PIN3	Changes CbCr3-IN pins function. 0: Component Cb/Cr input (pin 58: Y/G, pin 56: Cb/B, pin 54: Cr/R) 1: Separated C and CVBS input t (pin 58: Y, pin 56: C, pin 54: CVBS) * If "1: Separated C and CVBS input" is selected for CbCr PIN3, then CLAMP3 mode is set for "SYNC TIP CLAMP (for CVBS/Y) & SYNC TIP CLAMP (for CVBS)"	Cb/Cr input (0)
CLAMP1(3)	Switches Y1 (3)/G1(G3) & Cr1(3)/R1(3) clamping mode. The clamping mode for pin 40(58) & pin 36(54) is set. 0: SYNC TIP CLAMP (for Y/G with sync) & BIAS (Cr/R) 1: BIAS (for RGB without sync) * If "1: Separated C and CVBS input" is selected for CbCr PIN1(3), then CLAMP mode is set for "SYNC TIP CLAMP (for CVBS/Y) & SYNC TIP CLAMP (for CVBS/Y)"	SYNC TIP (0)
CLAMP2	Switches Y2 clamping mode. The clamping mode for pin 52 is set. 0: SYNC TIP CLAMP (for Y/G with sync) 1: BIAS (for RGB without sync)	SYNC TIP (0)
TEST0	TEST modes for shipping test. Set all to zero.	all 0
AU1(2) OUT	Switches audio outputs from AL/AR1 (2)-OUT (pins 3/5 (13/15)). 0000: MUTE 0001: AL/AR1 (pins28/26) 0010: AL/AR2 (pins32/30) 0011: AL/AR3 (pins35/33) 0100: AL/AR4 (pins39/37) 0101: AL/AR5 (pins43/41) 0110: AL/AR6 (pins 47/45) 0111: AL/AR7 (pins59/57) 1000: AL/AR8 (pins63/61) 1001～1111: Not available	AL/AR1 (0001)

Register Name	Function	Preset Value
HV-SEP1(2)	Switches the separation level. The H/V sync separation level to SYNC1(2)-IN (pin 25 (11)) is switched. 00: LOW 11: HIGH Remark: The separation level is changed according to the ratio of negative sync width per 1H period.	LOW (00)
SYNC LPF1(2)	Turns on the LPF for the sync-tip clamp. SYNC LPF1(2) for SYNC1(2)-IN pin changes the speed of sync-tip clamp response. Turn this function on for no input detection. 0: OFF 1: ON	OFF (0)
A-SYNC	Automatic sync processing mode. Sync processing mode is changed in accordance with the results obtained by the internal format detection circuits. Format detection is performed for SYNC2-IN or HD/VD-IN signal selected by HV DET. The result of detection is returned to H,V FORMAT, H,V FM2 and FORMAT. HV FREQ setting is invalid when this mode is active. 0: OFF (Manual switching mode by HV FREQ setting) 1: ON Remark: SYNC1-IN (pin25) is not available when A-SYNC=1(ON). In this case, format detection and H/V separation are applied to SYNC2-IN (pin11).	OFF (0)
SIG LPF	Turns on the LPF for the sync input pin (pin25; SYNC1-IN). When no input detection for weak strength signals is required, turn this function on to reduce noise on the input. Turn this function off for detections such as H, V FORMAT and H, V FREQ DET. 0: OFF 1: ON	OFF (0)
PS MASK	Switches the mask mode for pseudo-sync. 0: ON (Normal) 1: OFF (for “Sync on G”) (1)OFF mode is used for “Sync on G” input.	ON (0)

Register Name	Function	Preset Value
V-DET	Switches the V format detection mode. 0: 50/60Hz only 1: Full detection	50/60 only (0)
HD WIDTH	Switches the width of HD-OUT (pin 8) from SYNC2-IN (pin11). 0: WIDE 1: NARROW Remark: HD WIDTH = 1 (NARROW) is recommended for the 1125/50p/60p format owing to crosstalk from HD-OUT to video signals so that spike noises on video signals will occur.	WIDE (0)
HV-POL	Switches the polarity of HD/VD output. The polarity of HD/VD OUT (pin 8, 9) is set. 0: Positive 1: Negative	Positive (0)
HV DET	Selects the input for format detection. When A-SYNC=0 (Manual mode) 0: SYNC1-IN (pin 25) 1: HD/VD-IN (pins 23/22) When A-SYNC=1 (Automatic mode) This function is invalid. The input is selected by HV OUT.	SYNC (0)
HV OUT	Switches the outputs from HD/VD-OUT (pin 8/9). 0: SYNC2-IN (pin11) 1: HD/VD-IN (pins 23/22)	SYNC2-IN (0)
H DMY	Outputs the dummy HD when no-input. The dummy HD/VD output's frequency depends on HV FREQ2 setting (when A-SYNC = OFF) or H,V FORMAT (when A-SYNC = ON). No input detection is based on H IN result. 0: OFF 1: ON (Dummy HD output when no-input) NOTE: The HD output does not synchronize with input sync when A-SYNC = OFF and when a sync is input.	OFF (0)
V DMY	Outputs the dummy VD when no-input. The dummy HD/VD output's frequency depends on HV FREQ2 setting (when A-SYNC=OFF) or H,V FORMAT (when A-SYNC=ON). No-input detection is based on V IN result. 0: OFF 1: ON (Dummy VD output when no-input) NOTE: The VD output does not synchronize with input sync when A-SYNC = OFF and when a sync is input.	OFF (0)

Register Name	Function	Preset Value
HV FREQ2	Input format setting. Set the horizontal and vertical mode according to the format that is input. When A-SYNC = ON mode, this setting is invalid. 00000: 15.625 kHz, 50 Hz (625i) 00001: 15.75 kHz, 60 Hz (525i) 00010: 31.25 kHz, 50 Hz (625p) 00011: 31.5 kHz, 60 Hz (525p, VGA @60 Hz) 00100: 28.125 kHz, 50 Hz (1125/50i) 00101: 33.75 kHz, 60 Hz (1125/60i) 00110: 37.5 kHz, 50 Hz (750/50p) 00111: 45 kHz, 60 Hz (750/60p, XGA @60 Hz) 01000: 31.25 kHz, 50 Hz (1250i) 01001: 37.9 kHz, 60 Hz (SVGA @60 Hz) 01010: 64 kHz, 60 Hz (1125/60p, SXGA @60 Hz) 01011: 75 kHz, 60 Hz (UXGA @60 Hz) 01100: 56.25 kHz, 50 Hz (1125/50p) 01101 ~ 01111: Not available 10000: 15.734 kHz, 30 Hz (525/30p) 10001: 27 kHz, 24 Hz (1125/24p) 10010: 28.125 kHz, 25 Hz (1125/25p) 10011: 33.75 kHz, 30 Hz (1125/30p) 10100: 27kHz, 48 Hz (1125/24sf) 10101 ~ 11111: Not available	15.625 kHz, 50 Hz (00000)
H COUNT MAX	Selects H-sync higher threshold count number for the no-input detection. 0000: 32 counts 1111: 62 counts (2 counts / step)	32 counts (0000)
H COUNT MIN	Selects H-sync lower threshold count number for the no-input detection. 000: 16 counts 111: 30 counts (2 counts / step)	16 counts (000)
SIG DET N	Selects the signal detection count number for input existence threshold of the no-input detection. 0000: 1 count 0001: 2 counts ~ 1111: 30 counts (2 counts / step)	1 count (0000)
SIG RESET N	Selects the signal detection count number for input non-existence threshold of the no-input detection. 0000: 1 count 0001: 2 counts ~ 1111: 30 counts (2 counts / step)	1 count (0000)
SIG RESET	Resets the counter for no-input detection. When 1 is sent, the counter for no-input detection is cleared. 0: Normal 1: Reset	Normal (0)
SIG SW	Selects the input to the counter for no-input detection. 0: SYNC2-IN (pin 11) 1: SYNC1-IN (pin 25)	SYNC2-IN (0)
SIG DET IMPE	Changes the internal impedance for no-input detection. The time constant of LPF for no-input detection is changed by this function and the capacitor value of SYNC FILTER (pin10). 00: 20 kΩ 01: 15 kΩ 10: 10 kΩ 11: 6 kΩ	20 kΩ (00)
SIG DET LVL	Changes the threshold for no-input detection. 00: 0.55 V 01: 0.80 V 10: 1.05 V 11: 1.30 V	0.55 V (00)
TEST1,2,3	TEST modes for shipping test. Set all to zero.	all 0

Read Mode

Register Name	Function
POR	Power On Reset 0: Normal 1: Register preset After power on, 1 is returned at first read. 0 is returned at second and subsequent reads.
H FM2	Horizontal format detection 2 0: Known 1: Unknown Detects whether an input is in one of the defined formats or not. This is based on H FORMAT data.
V FM2	Vertical format detection 2 0: Known 1: Unknown Detects whether an input is in one of the defined formats or not. This is based on V FORMAT data.
H IN	Input detection to horizontal syncs 0: No-input 1: Signal detected
V IN	Input detection to vertical syncs 0: No-input 1: Signal detected
V-SYNC-W	V-SYNC width detection 0: Wide 1: Narrow Detects V-SYNC width for detecting 1250i format. Under A-SYNC=1(ON), V-SYNC-W shows 1 when VD width from VD-IN pin is narrower than approx. 69 us, or when V-SYNC width from SYNC-IN pin is narrower than approx. 54 us.
HD-POL	Polarity detection to HD-IN 0: Positive 1: Negative Detects the width from the HD-IN pin to determine whether it is negative or not. When the High level of the input is wider than approx. 13.5 us, HD-POL shows 1.
VD-POL	Polarity detection to VD-IN 0: Positive 1: Negative Detects the width from the VD-IN pin to determine whether it is negative or not. When the High level of the input is wider than approx. 4.5 ms, VD-POL shows 1.
H FORMAT	Horizontal format detection 0000: 15.625/15.75 kHz 0001: 28.125 kHz 0010: 31.25/31.5 kHz 0011: 33.75 kHz 0100: 37.5/37.9 kHz 0101: 45/48 kHz 0110: 56.25 kHz 0111: 64/67.5 kHz 1000: 75 kHz 1001 ~ 1111: Undefined Detects the horizontal format (horizontal frequency).
V FORMAT	Vertical format detection 000: 50 Hz 001: 60 Hz 010: 48 Hz 011: 30 Hz 100: 25 Hz 101: 24 Hz 110 ~ 111: Undefined Detects the vertical format (horizontal frequency) according to V FREQ DET data.
SIG DET	No-input detection. 0: No-input 1: A signal detected The signal to the no-input detection circuit is selected by SIG SW. Refer to relevant functions, H COUNT MAX, H COUNT MIN, SIG DET N, SIG RESET N, SIG RESET, SIG DET IMPE and SIG DET LVL.
HV-OUT FORMAT	Format detection result. H and V dummy output frequencies depend on this result. 00000: 15.625 kHz, 50 Hz (625i) 00001: 15.75 kHz, 60 Hz (525i) 00010: 31.25 kHz, 50 Hz (625p) 00011: 31.5 kHz, 60 Hz (525p, VGA @60 Hz) 00100: 28.125 kHz, 50 Hz (1125/50i) 00101: 33.75 kHz, 60 Hz (1125/60i) 00110: 37.5 kHz, 50 Hz (750/50p) 00111: 45 kHz, 60 Hz (750/60p, XGA @60 Hz) 01000: 31.25 kHz, 50 Hz (1250i) 01001: 37.9 kHz, 60 Hz (SVGA @60 Hz) 01010: 64 kHz, 60 Hz (1125/60p, SXGA @60 Hz) 01011: 75 kHz, 60 Hz (UXGA @60 Hz) 01100: 56.25 kHz, 50 Hz (1125/50p) 01101 ~ 01111: Not available 10000: 15.734 kHz, 30 Hz (525/30p) 10001: 27 kHz, 24 Hz (1125/24p) 10010: 28.125 kHz, 25 Hz (1125/25p) 10011: 33.75 kHz, 30 Hz (1125/30p) 10100: 27 kHz, 48 Hz (1125/24sf) 10101 ~ 11111: Not available

Register Name	Function
DC1 ~ 10	DC voltage detection for D-pin or S-pin 00: Low (0 V) 01: Mid (2.2 V) 10: Undefined 11: High (5 V) Remark1; See below for the relationship between this function number and the pin number. DC1 - pin 1, DC2 - pin 14, DC3 - pin 27, DC4 - pin 29, DC5 - pin 31, DC6 - pin 34, DC7 - pin 49, DC8 - pin 51, DC9 - pin 53, DC10 - pin 55, Remark2; for D-pin SW LINE: 00: Connected 01: ---- 10: ---- 11: Not-connected LINE1: 00: 525 (480) 01: 750 (720) 10: ---- 11: 1125 (1080) LINE2: 00: interlace 01: ---- 10: ---- 11: progressive LINE3: 00: 4:3 01: 4:3 letter box 10: ---- 11: 16:9 Remark3; for S-pin 00: 4:3 01: 4:3 letter box 10: ---- 11: 16:9
S1 ~ 6	Detects if S-pin is connected or not. 0: Low (not-connected) 1: Open (connected) Remark1; An external circuit is necessary to use this function. Refer to Function description. Remark2; See below for the relationship between this function number and the pin number. S1 - pin 38, S2 - pin 44, S3 - pin 48, S4 - pin 50, S5 - pin 56, S6 - pin 62
V FREQ DET	Counts the vertical frequency of an input selected by SYNC SW. When V-DET=0; 00000000: over 3.5 kHz 01001111: 44 Hz or less 01010000～11111111: No input When V-DET=1; 00000000: over 3.5 kHz 10011001: 23 Hz or less 10011010～11111111: No input To calculate the vertical frequency (Y) ; Convert data read from V FREQ DET into decimal value and call it X. Vertical frequency (Y) = $1 \div (X \times 2.8607 \times 10^{-4})$ [Hz] The error range of X is −1 to +1.
H FREQ DET	Counts the horizontal frequency of an input selected by SYNC SW. When for SYNC-IN; 00000001: No input 11111111: over 85kHz When for HD/VD-IN; 00000000: No input 11111111: over 85kHz To calculate the horizontal frequency (Y) ; Convert data read from H FREQ DET into decimal value and call it X. Horizontal frequency (Y) = $1 \div (0.003 \div X)$ [Hz] The error range of X is −1 to +1.

Note 1: In determining the decision algorithms (detection range, detection times and so on) for H/V frequency detection, it is necessary to take into account both previously mentioned cautions and other factors such as signal conditions and I^2CBUS data transmission in the course of prototype TV set evaluation.

Note 2: The READ BUS flags indicate that a certain signal is detected at a given moment. However, the detection result will not be very reliable if only one flag is checked. To obtain accuracy, it is recommended that a judgment will be made on the basis of confirming several times and verifying agreement among the majority of flags read in a sequence and/or at the same time.

Function Descriptions

Output selections

Outputs are switched by I2CBUS registers, as in the following tables.

YCbCr1 OUT

Register settings					Outputs			Available input		
YCbCr OUT	Reserved	CbCr PIN3	CbCr PIN2	CbCr PIN1	CVBS/Y/G OUT (pin 2)	Cb/B OUT (pin 4)	Cr/R OUT (pin 6)	CVBS	YC	YCbCr RGB
0000	*	*	*	*	Mute	Mute	Mute			
0001	*	*	*	*	SY1 (pin 42)	SC1 (pin 44)	Mute	y	y	
0010	*	*	*	*	SY2 (pin 60)	SC2 (pin 62)	Mute	y	y	
0011	*	*	*	*	Not available					
0100	*	*	*	*						
0101	*	*	*	*						
0110	*	*	0	*	CVBS3 (pin46)	Mute	Mute	y		
	*	*	1	*	CVBS3 (pin 46)	Cr2 (pin 48)	Mute	y	y	
0111	*	*	*	0	Y1 (pin 40)	Cb1 (pin 38)	Cr1 (pin 36)	y	y	y
	*	*	*	1	Y1 (pin 40)	Cb1 (pin 38)	Mute	y	y	
1000	*	*	0	*	Y2 (pin 52)	Cb2 (pin 50)	Cr2 (pin 48)	y	y	y
	*	*	1	*	Y2 (pin 52	Cb2 (pin 50)	Mute	y	y	
1001	*	0	*	*	Y3 (pin 58)	Cb3 (pin 56)	Cr3 (pin 54)	y	y	y
	*	1	*	*	Y3 (pin 58)	Cb3 (pin 56)	Mute	y	y	
1010	*	*	*	*	Not available					
1011	*	*	*	*	Cr1 (pin 36)	Mute	Mute	y		
1100	*	*	*	*	Cr3 (pin 54)	Mute	Mute	y		
1101~1111	*	*	*	*	Not available					

*: Don't care

MONITOR OUT

Register settings						Outputs	Available input	
MON OUT	YC MIX	Reserved	CbCr PIN3	CbCr PIN2	CbCr PIN1	MONITOR OUT (pin 64)	CVBS	YC
0000	*	*	*	*	*	Mute		
0001	0	*	*	*	*	SY1 (pin 42)	y	
	1					SY1 (pin 42) + SC1 (pin 44)		y
0010	0	*	*	*	*	SY2 (pin 60)	y	
	1					SY2 (pin 60) + SC2 (pin 62)		y
0011	*	*	*	*	*	Not available	y	
0100	*	*	*	*	*		y	
0101	*	*	*	*	*		y	
0110	*	*	*	0	*	CVBS3 (pin46)	y	
	0	*	*	1	*	CVBS3 (pin 46)	y	
	1					CVBS3 (pin 46) + Cr2 (pin 48)		y
0111	0	*	*	*	*	Y1 (pin 40)	y	
	1					Y1 (pin 40) + Cb1 (pin38)		y
1000	0	*	*	*	*	Y2 (pin 52)	y	
	1					Y2 (pin 52) + Cb2 (pin 50)		y
1001	0	*	*	*	*	Y3 (pin 58)	y	
	1					Y3 (pin 58) + Cb3 (pin 56)		y
1010	*	*	*	*	*	Not available	y	
1011	*	*	*	*	*	Cr1 (pin 36)	y	
1100	*	*	*	*	*	Cr3(pin 54)	y	
1101~1111	*	*	*	*	*	Not available		

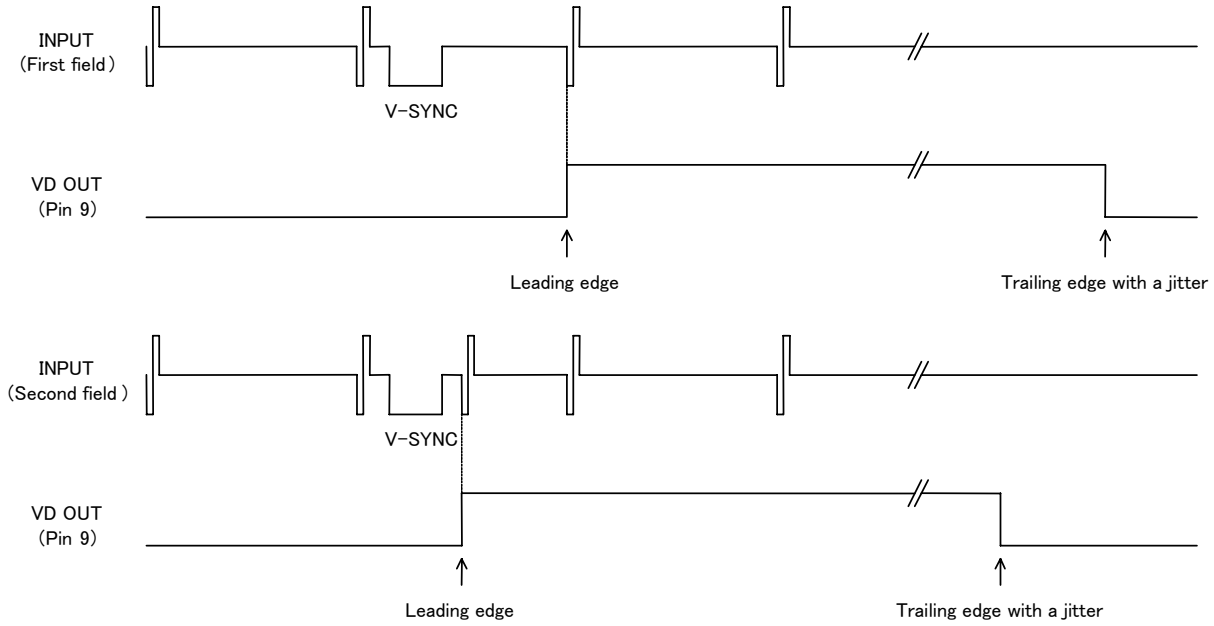
*: Don't care

Vertical sync separation for 1250i/50

When HV FREQ2 = 01000, the vertical sync separation for the 1250i/50 is accomplished through the use of a special circuit. The phase of the VD-out (pin 9) depends on the H-SYNC timing shown in the figure below. There is no VD-out when there is no H-SYNC input.

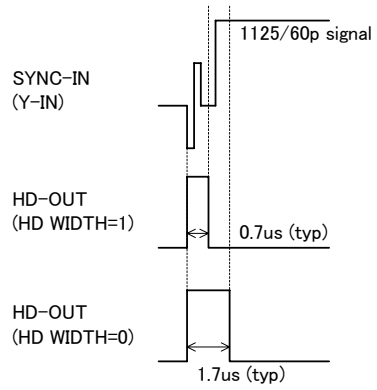
In the manual sync processing mode (A-SYNC = OFF), use READ BUS functions, V-SYNC-W and H, V FORMAT (or H, V FREQ DET) to detect the 1250i/50.

NOTE: The VD-OUT's tailing edge has a jitter. Use the leading edge only.



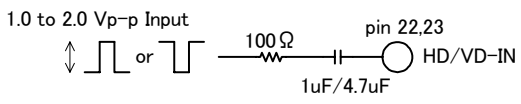
HD width

HD-OUT width is selectable by HD WIDTH as below. HD WIDTH = 1 (NARROW) is recommended for the 1125/50p/60p format owing to crosstalk from HD-OUT to video signals so that spike noises on video signals will occur.

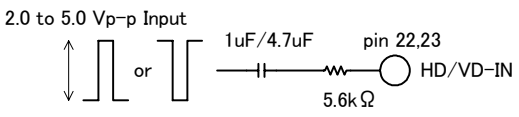


HD/VD input amplitude

When a 5.6 kΩ is added before the input pin as in the following figure, 5.0 Vp-p pulse input is allowed. However, the acceptable minimum amplitude then becomes 2.0 Vp-p.



Normal application



For large input application

Automatic sync processing mode (A-SYNC)

Counted horizontal and vertical frequency data to input signal are returned to READ BUS functions, H,V FREQ DET. Also, the detected format is returned to H, V FORMAT and H, V FM2 when the H/V frequencies are in internally-defined ranges. Input detection results, which indicate whether there is an input or not, for H, V-SYNC or HD,VD, are returned to H,V IN. HV-OUT FORMAT indicates the active mode.

In automatic sync processing mode (when A-SYNC = ON), this device operates as indicated in the following table according to these READ data. SYNC1-IN pin is also not used for detecting format.

INPUT CONDITION	HV-OUT FORMAT, H, V FORMAT status	H, V FM2 status	H, V IN status	HD, VD outputs
Standard format	The format as input	Known	Signal	The separated sync as input
Non-standard format	The status indicates not the current condition but the last detected format.	Unknown	Signal	The separated sync as input
No input	The status indicates not the current condition but the last detected format.	Known: The status indicates not the current condition but the last detected format.	No input	Dummy HD and VD, of which the frequency depends on the HV-OUT FORMAT status

NOTE 3: Dummy HD and VD may become unstable while the mode is changing form one format to another.

Manual sync processing mode (A-SYNC=OFF)

In this mode, SYNC1-IN pin is used only for detecting the input format and SYNC2-IN pin is used only for separating H and V syncs for HD and VD outputs. It is possible to detect some input's formats by means of time-sharing while separating syncs to another input.

The following is an example of how to detect H/V frequency when A-SYNC = OFF.

1. Input the signal from Yvi-OUT pin into SYNC1-IN pin.
2. Read data such as H, V FREQ DET and H, V FORMAT.
3. Detect the H/V frequency by microprocessor or similar means, depending on the data obtained.
4. Input the detected signal into SYNC2-IN pin and set HV FREQ2 and so on for SYNC2-IN pin to the detected mode.
5. Continue to monitor the obtained data for SYNC1-IN pin such as H, V FREQ DET and H, V FORMAT. When any alterations are recognized, re-set HV FREQ2 and so on for SYNC2-IN pin.

Decision algorithms (for detection range, detection times and so on) for H/V frequency detection should be determined taking into account the above-mentioned errors in measuring H/V frequencies and other factors such as signal conditions and I^2CBUS data transmission in the course of prototype TV set evaluation.

Note also, in A-SYNC = OFF and H, V DMY = ON mode, dummy HD and VD are output according to HV FREQ2 setting when there is no input.

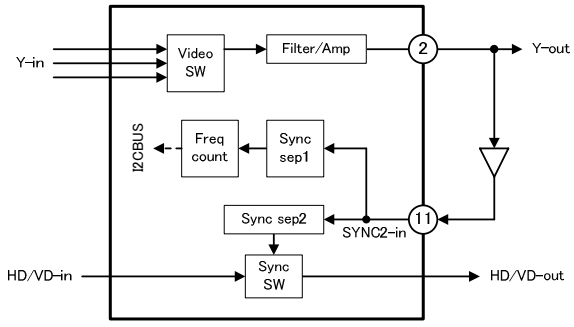


Fig. The signal route when A-SYNC = ON

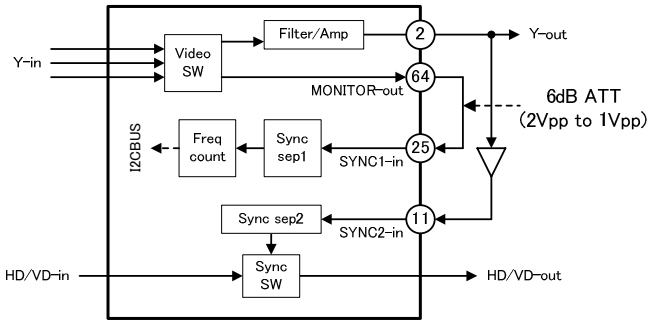


Fig. The signal route when A-SYNC = OFF

Sync separation level

The sync separation level is changed according to the ratio of H-sync width to one line. Typical sync separation levels for each format are as follows.

HV-SEP data	00	01	10	11
625/50i	18	26	31	43
525/60i	18	26	31	43
625/50p	19	27	32	44
525/60p	19	27	32	44
1125/50i	27	34	40	52
1125/60i	25	33	38	50
750/50p	25	32	38	50
750/60p	24	31	36	49
1250/50i	22	30	36	48
1125/50p	28	36	41	52
1125/60p	27	34	39	52
525/30p	18	26	31	43
1125/24p	27	34	40	52
1125/25p	27	34	40	52
1125/30p	26	32	38	50
1125/24sf	28	34	40	52
VGA/60	20	26	32	43
SVGA/60	20	27	33	44
XGA/60	20	27	33	44
SXGA/60	22	29	34	45

Unit [%] ; where 286 mVp-p sync for 525/60i and 300 mVp-p sync for others

Format detection and sync separation performance are affected by the separation level set by HV-SEP setting and the value of the connected coupling capacitor. Careful evaluation is required to set the separation level under consideration of expected input conditions such as a suppressed sync input, an input with V-sag and APL (Average Picture Level) fluctuations.

For “Sync on G” signal, HD-OUT is not output during V-sync period because there is no H-sync during V-sync period.

No input detection

This function detects if there is an input or not. It is useful for detecting no-input of 525i or 625i, including signals of weakened strength.

(1)0 (no-input) → 1 (detected)

When Nmin ≦ N1≦ Nmax, and when N2 ≧ Ndet, SIG DET returns 1.

Where, Nmin: the number set by H COUNT MIN

Nmax: the number set by H COUNT MAX

Ndet: the number set by SIG DET N

N1: the number of H-sync into the counter during an internal window (approx. 2ms)

N2: the number of condition where "Nmin ≦ N1 ≦ Nmax" is detected

(2) 1 (detected) → 0 (no-input)

When N1 ≦ Nmin, N1 ≧ Nmax, and when N3 ≧ Nreset, SIG DET returns 0.

Where, Nreset: the number set by SIG RESET N

N3: the number of condition where "N1 ≦ Nmin and N1 ≧ Nmax" is detected

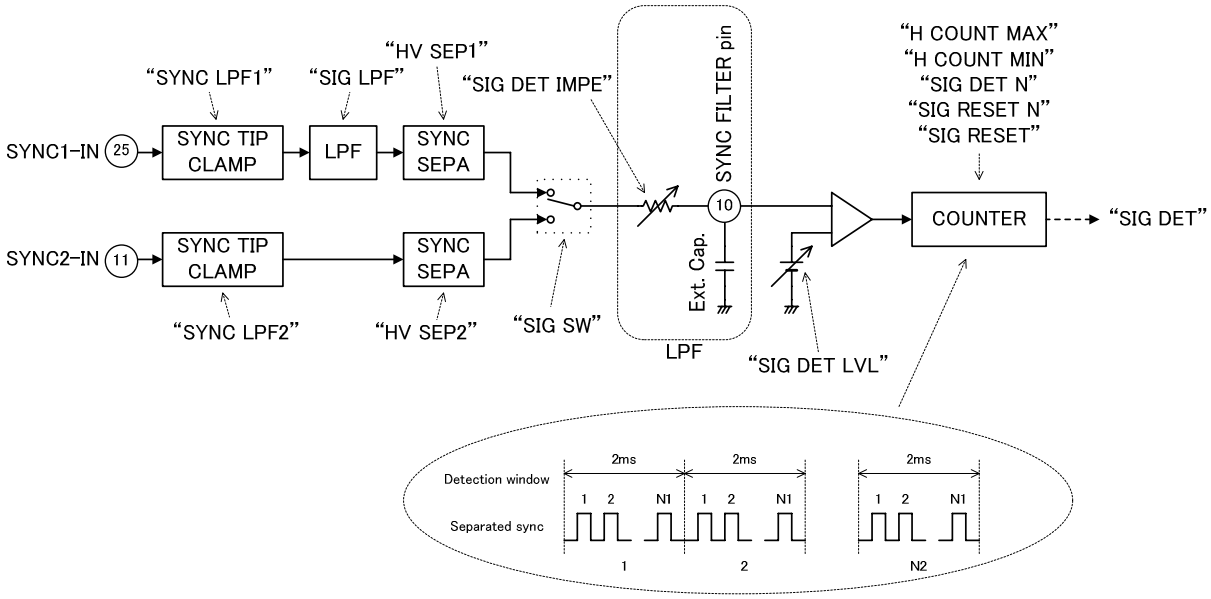


Fig. block diagram of no-input detection

Determine the use of no-input detection following sufficient evaluations using a prototype TV set.

S-pin insertion detection

C-IN pins detect DC level to recognize if S-pin is inserted or not.

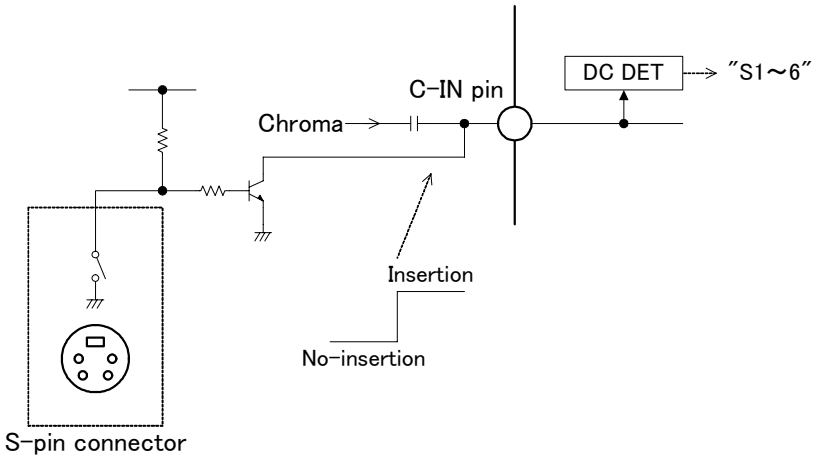


Fig. an application of S-pin insertion detection

V Freq detection

Counts the vertical frequency of an input selected by SYNC SW.

When V-DET=0;
00000000: over 3.5 kHz 01001111: 44 Hz or less
01010000～11111111: No input

When V-DET=1;
00000000: over 3.5 kHz 10011001: 23 Hz or less
10011010～11111111: No input

To calculate the vertical frequency (Y) ;

Convert data read from V FREQ DET into decimal value and call it X.

Vertical frequency (Y) = $1 \div (X \times 2.8607 \times 10^{-4})$ [Hz]

The error range of X is −1 to +1.

BIN	DEC	HEX	Fregency[Hz] V-det=0	Fregency[Hz] V-det=1	BIN	DEC	HEX	Fregency[Hz] V-det=0	Fregency[Hz] V-det=1
0	0	0	Over 3500	Over 3500	1010000～1101110	～		No Input	～
1～110110	～				1101111	111	6F	No Input	31.5
110111	55	37	63.6	63.6	1110000	112	70	No Input	31.2
111000	56	38	62.4	62.4	1110001	113	71	No Input	30.9
111001	57	39	61.3	61.3	1110010	114	72	No Input	30.7
111010	58	3A	60.3	60.3	1110011	115	73	No Input	30.4
111011	59	3B	59.2	59.2	1110100	116	74	No Input	30.1
111100	60	3C	58.3	58.3	1110101	117	75	No Input	29.9
111101	61	3D	57.3	57.3	1110110	118	76	No Input	29.6
111110	62	3E	56.4	56.4	1110111	119	77	No Input	29.4
111111	63	3F	55.5	55.5	1111000	120	78	No Input	29.1
1000000	64	40	54.6	54.6	1111001	121	79	No Input	28.9
1000001	65	41	53.8	53.8	1111010	122	7A	No Input	28.7
1000010	66	42	53.0	53.0	1111011～10000110	～		No Input	～
1000011	67	43	52.2	52.2	10000111	135	87	No Input	25.9
1000100	68	44	51.4	51.4	10001000	136	88	No Input	25.7
1000101	69	45	50.7	50.7	10001001	137	89	No Input	25.5
1000110	70	46	49.9	49.9	10001010	138	8A	No Input	25.3
1000111	71	47	49.2	49.2	10001011	139	8B	No Input	25.1
1001000	72	48	48.6	48.6	10001100	140	8C	No Input	25.0
1001001	73	49	47.9	47.9	10001101	141	8D	No Input	24.8
1001010	74	4A	47.2	47.2	10001110	142	8E	No Input	24.6
1001011	75	4B	46.6	46.6	10001111	143	8F	No Input	24.4
1001100	76	4C	46.0	46.0	10010000	144	90	No Input	24.3
1001101	77	4D	45.4	45.4	10010001～10011000	～		No Input	～
1001110	78	4E	44.8	44.8	10011001	153	99	No Input	23Hz or less
1001111	79	4F	44Hz or less	44.2	10011010～11111111	154～255	9A～FF	No Input	No Input

H Freq detection

Counts the horizontal frequency of an input selected by SYNC SW.

When for SYNC-IN;
00000001: No input 11111111: over 85kHz

When for HD/VD-IN;
00000000: No input 11111111: over 85kHz

To calculate the horizontal frequency (Y) ;

Convert data read from H FREQ DET into decimal value and call it X.

Horizontal frequency (Y) = 1 ÷ (0.003 ÷ X) [Hz]

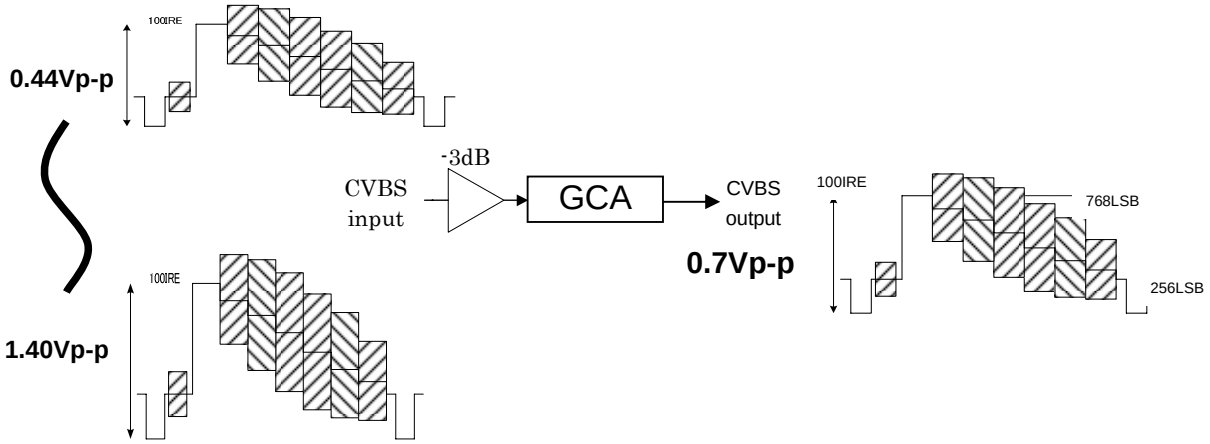
The error range of X is −1 to +1.

BIN	DEC	HEX	Fregency[kHz] Sync IN	Fregency[kHz] HD/VD IN
0	0	0	–	No Input
1	1	1	No Input	0.33
10～101100			～	
101101	45	2D	15.00	15.00
101110	46	2E	15.33	15.33
101111	47	2F	15.67	15.67
110000～1010011			～	
1010100	84	54	28.00	28.00
1010101	85	55	28.33	28.33
1010110	86	56	28.67	28.67
1010111～1011100			～	
1011101	93	5D	31.00	31.00
1011110	94	5E	31.33	31.33
1011111	95	5F	31.67	31.67
1100000	96	60	32.00	32.00
1100001	97	61	32.33	32.33
1100010	98	62	32.67	32.67
1100011	99	63	33.00	33.00
1100100	100	64	33.33	33.33
1100101	101	65	33.67	33.67
1100110～1101110			～	
1101111	111	6F	37.00	37.00
1110000	112	70	37.33	37.33
1110001	113	71	37.67	37.67
1110010	114	72	38.00	38.00
1110011	115	73	38.33	38.33
1110100～10000100			～	

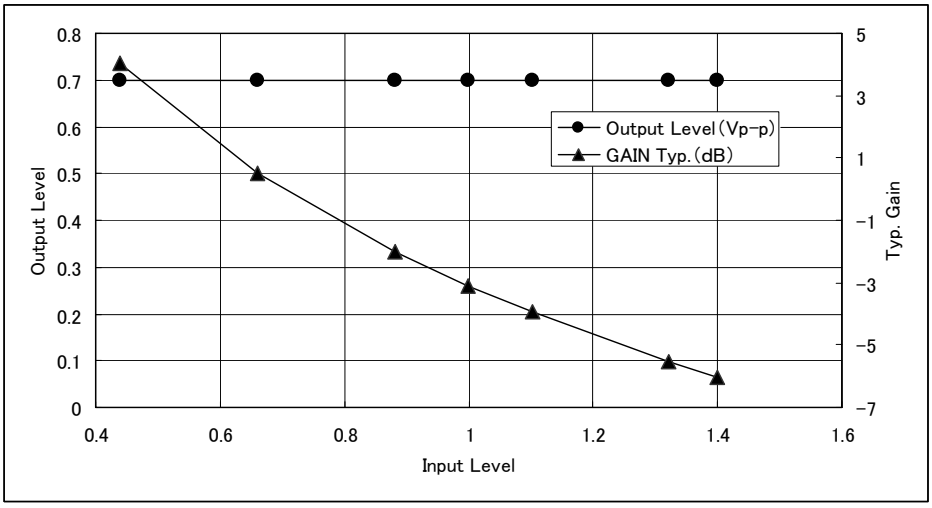
BIN	DEC	HEX	Fregency[kHz] Sync IN	Fregency[kHz] HD/VD IN
10000101	133	85	44.33	44.33
10000110	134	86	44.67	44.67
10000111	135	87	45.00	45.00
10001000	136	88	45.33	45.33
10001001	137	89	45.67	45.67
10001010～10100101			～	
10100110	166	A6	55.33	55.33
10100111	167	A7	55.67	55.67
10101000	168	A8	56.00	56.00
10101001	169	A9	56.33	56.33
10101010	170	AA	56.67	56.67
10101011～10111101			～	
10111110	190	BE	63.33	63.33
10111111	191	BF	63.67	63.67
11000000	192	C0	64.00	64.00
11000001	193	C1	64.33	64.33
11000010	194	C2	64.67	64.67
11000011～11011110			～	
11011111	223	DF	74.33	74.33
11100000	224	E0	74.67	74.67
11100001	225	E1	75.00	75.00
11100010	226	E2	75.33	75.33
11100011	227	E3	75.67	75.67
11100100～11111110			～	
11111111	255	FF	Over 85	Over 85

GCA gain

GCA gain is controlled by Y/G/CVBS OUT gain, and controls only CVBS Input signal. GCA gain is controlled by a 6bit I2C-Bus, and this LSI does not have an Input level detection circuit.. In order to perform GCA control, it is necessary to input CVBS/Y/G OUT to SYNC2 IN. By doing so, V latch starts with a Vsepa signal and GCA control becomes possible. In this case, the BUS must be set as CVBS/Y GAIN=1 (-3dB).



The following figure shows typical GCA gain characteristics.



	Min		Typ				Max
Input Level(Vp-p)	0.44	0.6605	0.881	0.9998	1.1015	1.3221	1.4
Output Level(Vp-p	0.7	0.7	0.7	0.7	0.7	0.7	0.7
GAIN Typ.(dB)	4.0329	0.5043	−1.998	−3.096	−3.938	−5.523	−6.0206
Bin	000000	001101	011010	100001	100111	110100	111111
Dec	0	13	26	33	39	52	63
Hex	00	0D	1A	21	27	34	3F

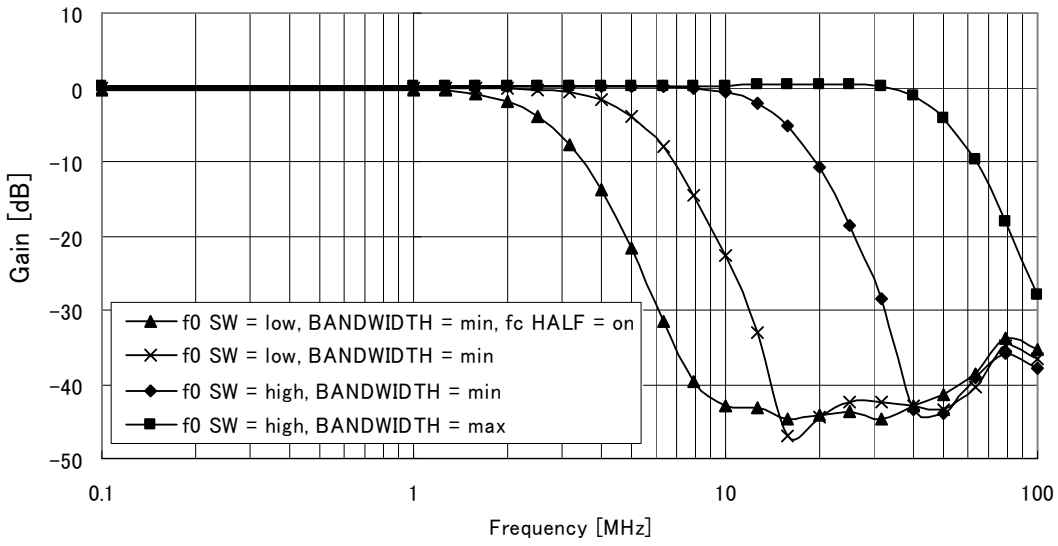


Fig. Typical pre-filter frequency characteristics

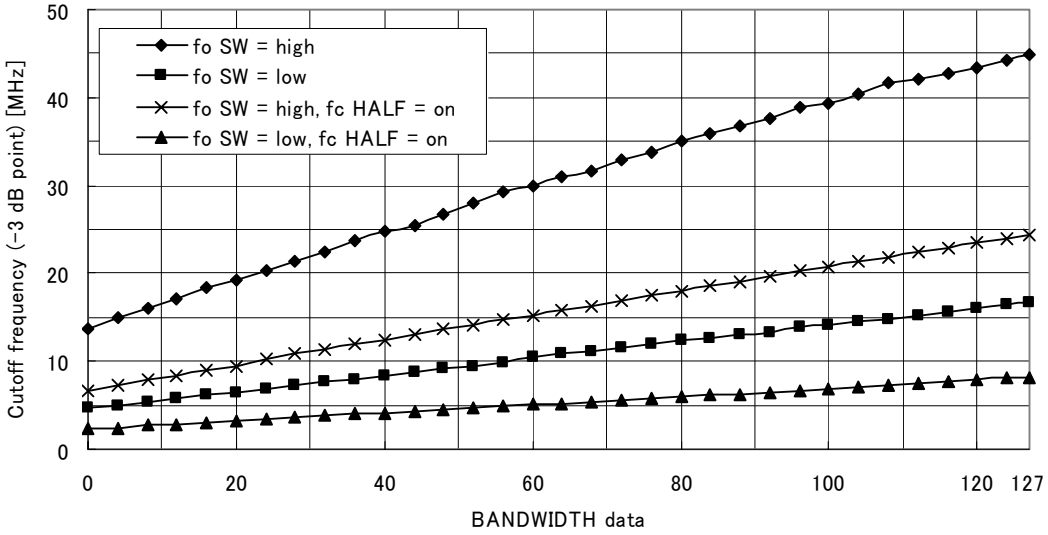


Fig. Typical cutoff frequency characteristics of pre-filter (-3 dB point)

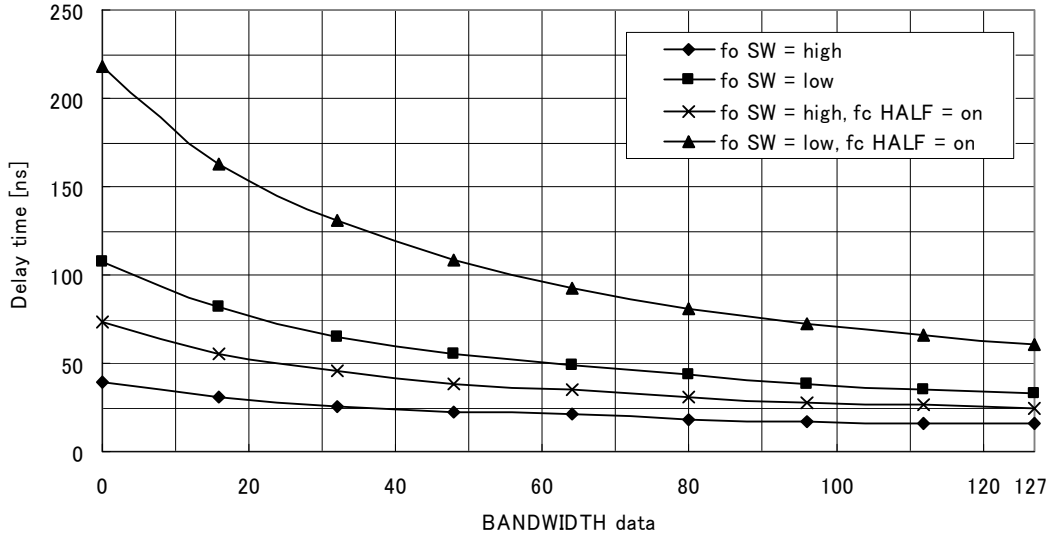


Fig. Typical delay-time characteristics of pre-filter (group delay @ 1MHz)

Recommended crystal oscillator

When a connected crystal oscillator is used for the XO, the following oscillation specifications are required.

Oscillation frequency (fundamental): 3.579545MHz (for NTSC decoding)

Frequency tolerance: +/- 50ppm

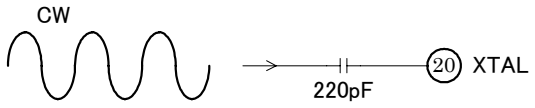
External CW input into crystal oscillator pin

Instead of connecting a crystal oscillator, it is possible to input an external CW (Continual Wave) into pin 28 through a capacitor as below.

The required specs on the CW are as follows.

Input frequency (fundamental): 3.579545MHz +/- 50ppm

Input amplitude: 1.0Vp-p +/- 0.5Vp-p



How to deal with unused pins

Unused pins should be dealt with as below. Pins not mentioned below should be connected properly.

Pin No.	Pin Name	Procedure	Pin No.	Pin Name	Procedure
1	DC1(S2)	Procedure 2	38	Cb1/B1 IN	Procedure 1
2	CVBS/Y/G OUT	Procedure 3	39	AL4 IN	Procedure 1
3	AL1 OUT	Procedure 3	40	Y1/G1 IN	Procedure 1
4	Cb/B OUT	Procedure 3	41	AR5 IN	Procedure 1
5	AR1 OUT	Procedure 3	42	SY1 IN	Procedure 1
6	Cr/R OUT	Procedure 3	43	AL5 IN	Procedure 1
8	HD OUT	Procedure 3	44	SC1 IN	Procedure 1
9	VD OUT	Procedure 3	45	AR6 IN	Procedure 1
10	SYNC FILTER	Procedure 3	46	CVBS3 IN	Procedure 1
11	SYNC2 IN	Procedure 1	47	AL6 IN	Procedure 1
13	AL2 OUT	Procedure 3	48	Cr2/R2 IN	Procedure 1
14	DC2(S1)	Procedure 2	49	DC7(SW LINE2)	Procedure 2
15	AR2 OUT	Procedure 3	50	Cb2/B2 IN	Procedure 1
22	VD IN	Procedure 4	51	DC8(LINE3-2)	Procedure 2
23	HD IN	Procedure 4	52	Y2/G2 IN	Procedure 1
25	SYNC1 IN	Procedure 1	53	DC9(LINE2-2)	Procedure 2
26	AR1 IN	Procedure 1	54	Cr3/R3 IN	Procedure 1
27	DC3(SW LINE1)	Procedure 2	55	DC10(LINE1-2)	Procedure 2
28	AL1 IN	Procedure 1	56	Cb3/B3 IN	Procedure 1
29	DC4(LINE3-1)	Procedure 2	57	AR7 IN	Procedure 1
30	AR2 IN	Procedure 1	58	Y3/G3 IN	Procedure 1
31	DC5(LINE2-1)	Procedure 2	59	AL7 IN	Procedure 1
32	AL2 IN	Procedure 1	60	SY2 IN	Procedure 1
33	AR3 IN	Procedure 1	61	AR8 IN	Procedure 1
34	DC6(LINE1-1)	Procedure 2	62	SC2 IN	Procedure 1
35	AL3 IN	Procedure 1	63	AL8 IN	Procedure 1
36	Cr1/R1 IN	Procedure 1	64	MONITOR OUT	Procedure 3
37	AR4 IN	Procedure 1	–	–	–

Procedure 1: Connect a 0.01 μF capacitor between this pin and GND.
Procedure 2: Connect to GND.
Procedure 3: Leave open.
Procedure 4: Connect a 10 kΩ resistor between this pin and GND.

How To Start I^2CBUS

The following describes how to send bus data after power on. Use software to handle the procedure.

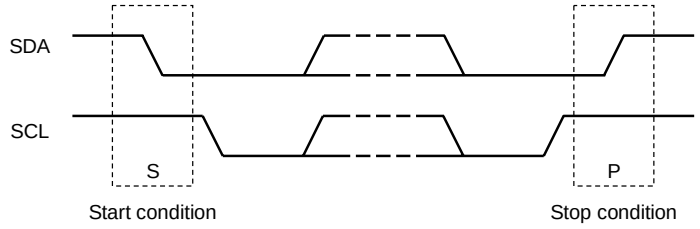
1. Turn power on.
2. Transmit all write data.

How To Transmit/Receive Via I^2CBUS

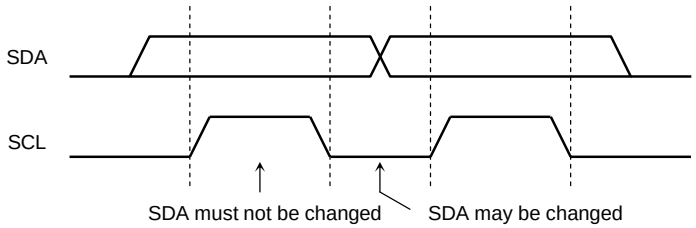
Slave Address: DE_H / DF_H

A6	A5	A4	A3	A2	A1	A0	W/R
1	1	0	1	1	1	1	0/1

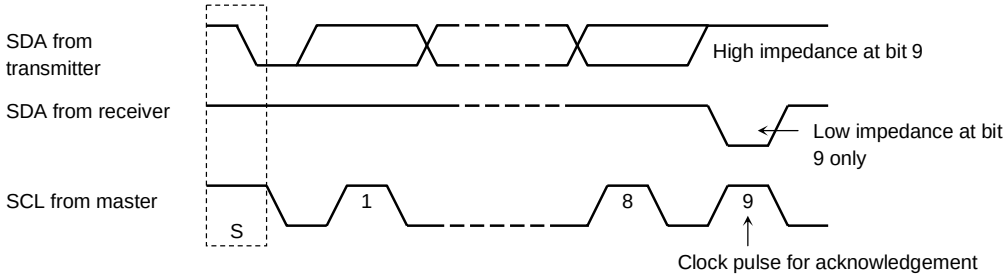
Start and Stop Conditions



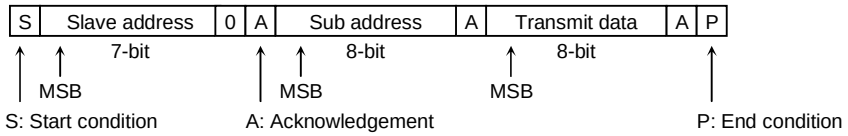
Bit Transmission



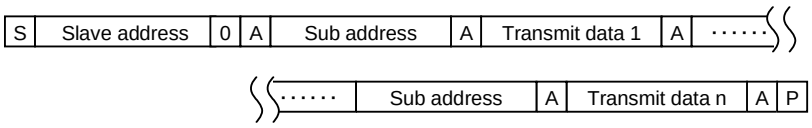
Acknowledgement



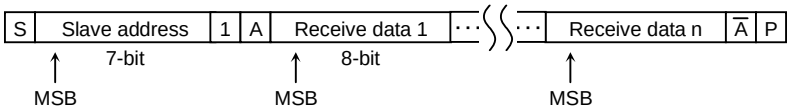
Data Transmit Format 1



Data Transmit Format 2



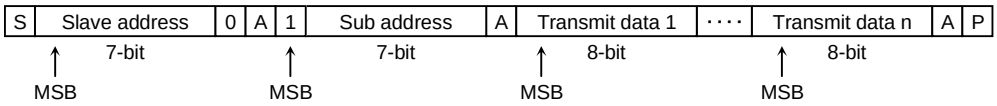
Data Receive Format



To receive data, the master transmitter changes to a receiver immediately after the first acknowledgement. The slave receiver changes to a transmitter.

The end condition is always created by the master.

Optional Data Transmit Format (Automatic Increment Mode)



In this way, sub addresses are automatically incremented from the specified sub address and data are set.

I^2CBUS Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Low level input voltage	V_{IL}	0	–	1.1	V
High level input voltage	V_{IH}	2.4	–	V/S-Vcc	V
Hysteresis of Schmitt trigger inputs	V_{hys}	–	0.7	–	V
Low level output voltage at 3 mA sink current	V_{OL1}	0	–	0.4	V
Input current each I/O pin with an input voltage between 0.1 VDD and 0.9 VDD	I_i	-10	–	10	μA
Capacitance for each I/O pin	C_i	–	–	10	pF
SCL clock frequency	f_{SCL}	0	–	400	kHz
Hold time START condition	$t_{HD;STA}$	0.6	–	–	μs
Low period of SCL clock	t_{LOW}	1.3	–	–	μs
High period of SCL clock	t_{HIGH}	0.6	–	–	μs
Set-up time for a repeated START condition	$t_{SU;STA}$	0.6	–	–	μs
Data hold time	$t_{HD;DAT}$	0	–	–	ns
Data set-up time	$t_{SU;DAT}$	100	–	–	ns
Set-up time for STOP condition	$t_{SU;STO}$	0.6	–	–	μs
Bus free time between a STOP and START condition	t_{BUF}	1.3	–	–	μs

NOTE: These parameters are not tested during production and are provided only as information to assist the design of applications.

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Supply voltage	9V Vcc	V_{CCmax9}	12.0	V
	5V Vcc	V_{CCmax5}	6.0	
	3.3V Vcc	V_{CCmax3}	6.0	
Input pin voltage		V_{in}	GND − 0.3 ~ Vcc + 0.3	V
Y or Sync input amplitude (pin 22,23,25,36,38,40,42,46,48,50,52,54,56,58,60)		Y_{in}	2.0	Vp-p
Power dissipation		P_D(Note 4)	1388	mW
Power dissipation reduction rate		1/θja	11.1	mW/°C
Operating temperature		T_{opr}	−20 ~ 75	°C
Storage temperature		T_{stg}	−55 ~ 150	°C

Note 4: Refer to the figure below. However, these conditions apply only to the case where the device is mounted on a board (50 x 50 mm). Mount the device on a board which is larger than this.

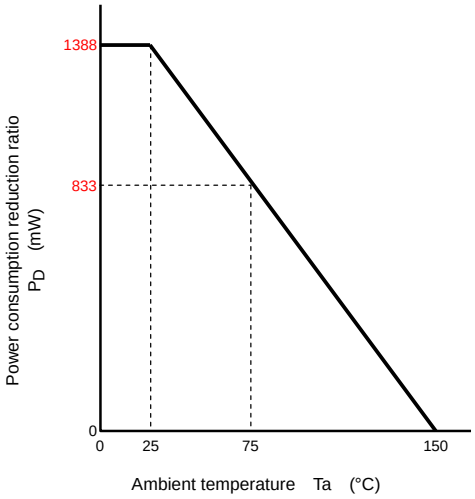


Figure P_D - Ta Curve

Note 5: Pins of this product are sensitive to electrostatic discharge. When handling this product, protect the environment to avoid electrostatic discharge.

Note 6: Install the product correctly. Otherwise, it may result in break down, damage and/or degration to the product or equipment.

The absolute maximum ratings of a semiconductor device are a set of specified parameter values, which must not be exceeded during operation, even for an instant.

If any of these ratings are exceeded during operation, the electrical characteristics of the device may be irreparably altered and the reliability and lifetime of the device can no longer be guaranteed.

Moreover, operation when these ratings are exceeded may cause break down, damage and/or degradation to any other equipment. Applications using the device should be designed such that each maximum rating will never be exceeded under any operating conditions.

Before using, creating and/or producing designs, refer to and comply with the precautions and conditions set forth in this document.

Operating conditions

Characteristic		Description		Min.	Typ.	Max.	Unit
Supply voltage (V_{CC})		Pin 16		8.5	9.0	9.5	V
		Pin 7		4.7	5.0	5.3	
		Pin 21; Supply power from V/S Vcc (pin 7) via a resistor.		3.1	3.3	3.5	
Y/G signal input amplitude		Pins40,52,58; with sync		–	1.0	–	V_{p-p}
CVBS/SY input amplitude		Pins42,46,60,(36,54); with sync		–	1.0	–	V_{p-p}
Y/G signal input frequency		Pins 40,52,58		0	-	60	MHz
CVBS/SY input frequency		Pins 42,46,60,(36,54)		0	-	8	MHz
SC (Chroma) signal input amplitude		Pin 44,62(38,48,50,56)		–	–	2	V_{p-p}
Cb, Cr, Pb, Pr signal input amplitude		Pins36,38,48,50,54,56; 100% color bar signal		–	0.7	–	V_{p-p}
Cb, Cr, Pb, Pr signal input frequency		Pins 36,38,48,50,54,56		0	-	60	MHz
R, G, B signal input amplitude		Pins36,38,40,48,50,52,54,56,58; 100% white signal without sync		–	0.7	–	V_{p-p}
R, G, B signal input frequency		Pins 36,38,40,48,50,52,54,56,58		0	—	60	MHz
HD, VD signal input amplitude		Pins 22,23		1.0	-	2.0	V_{p-p}
HD input frequency		Pins 23 for freq counter		0	—	85	kHz
VD input frequency		Pins 22 for freq counter		23	—	3500	Hz
DC detection input voltage	DC1~10	Pins 1,14,27,29,31,34,49,51,53,55	H	3.5	—	V/S Vcc	V
			M	1.4	2.2	2.4	
			L	GND	—	0.6	
	S1~6	Pins 38,44,48,50,56,62	L	GND	—	0.6	V
SDA input current		Pins 17		–	–	3	mA

Remark: Supply power to all Vcc pins (pin 7,16,21).

Electrical Characteristics

(Unless otherwise specified, AU V_{CC} = 9 V, V/S V_{CC} = 5 V, V_{dd} = 3.3 V, Ta = 25°C, I^2CBUS data: preset values)

Current Consumption (f0 SW1/2 = 1, BANDWIDTH1/2 = max)

Pin Name	Symbol	Test Conditions	Min	Typ.	Max	Unit
AU V_{CC} (pin16)	I_{CCAU}	–	6.1	7.8	10.3	mA
V/S V_{CC} (pin7)	I_{CCVS}	–	54.3	67.9	89.6	
V_{dd} (pin21)	I_{CCD}	Resistance to 5 V; R = 180 Ω	6.2	9.3	12.7	

Pin Voltage (test condition: no signal input)

Pin No.	Pin Name	Symbol	Test Conditions	Min	Typ.	Max	Unit
1	DC1(S2)	V_1	–	–	0.1	–	V
2	CVBS/Y1/G1 OUT	V_2	–	1.0	1.3	1.6	
3	AL1 OUT	V_3	–	3.8	4.1	4.4	
4	Cb1/B1 OUT	V_4	–	1.0	1.3	1.6	
5	AR1 OUT	V_5	–	3.8	4.1	4.4	
6	Cr1/R1 OUT	V_6	–	1.0	1.3	1.6	
10	SYNC FILTER	V_{10}	–	3.0	3.3	3.6	
11	SYNC2 IN	V_{11}	–	1.5	1.8	2.1	
13	AL2 OUT	V_{13}	–	3.8	4.1	4.4	
14	DC2(S1)	V_{14}	–	–	0.1	–	
15	AR2 OUT	V_{15}	–	3.8	4.1	4.4	
20	XTAL	V_{20}	–	3.8	4.05	4.3	
22	VD IN	V_{22}	–	1.2	1.5	1.8	
23	HD IN	V_{23}	–	1.2	1.5	1.8	
25	SYNC1 IN	V_{25}	–	1.5	1.8	2.1	
26	AR1 IN	V_{26}	–	4.2	4.4	4.6	
27	DC3(SWLINE1)	V_{27}	–	–	0.2	–	
28	AL1 IN	V_{28}	–	4.2	4.4	4.6	
29	DC4(LINE3-1)	V_{29}	–	–	0.2	–	
30	AR2 IN	V_{30}	–	4.2	4.4	4.6	
31	DC5(LINE2-1)	V_{31}	–	–	0.1	–	
32	AL2 IN	V_{32}	–	4.2	4.4	4.6	
33	AR3 IN	V_{33}	–	4.2	4.4	4.6	
34	DC6(LINE1-1)	V_{34}	–	–	0.1	–	
35	AL3 IN	V_{35}	–	4.2	4.4	4.6	
36	Cr1/R1 IN	V_{36}	–	2.6	2.9	3.2	
37	AR4 IN	V_{37}	–	4.2	4.4	4.6	
38	Cb1/B1 IN	V_{38}	–	2.6	2.9	3.2	
39	AL4 IN	V_{39}	–	4.2	4.4	4.6	
40	Y1/G1 IN	V_{40}	–	2.0	2.3	2.6	
41	AR5 IN	V_{41}	–	4.2	4.4	4.6	
42	SY1 IN	V_{42}	–	2.0	2.3	2.6	

Pin No.	Pin Name	Symbol	Test Conditions	Min	Typ.	Max	Unit
43	AL5 IN	V_{43}	–	4.2	4.4	4.6	V
44	SC1 IN	V_{44}	–	2.6	2.9	3.2	
45	AR6 IN	V_{45}	–	4.2	4.4	4.6	
46	CVBS3 IN	V_{46}	–	2.0	2.3	2.6	
47	AL6 IN	V_{47}	–	4.2	4.4	4.6	
48	Cr2/R2 IN	V_{48}	–	2.6	2.9	3.2	
49	DC7(SWLINE2)	V_{49}	–	–	0.1	–	
50	Cb2/B2 IN	V_{50}	–	2.6	2.9	3.2	
51	DC8(LINE3-2)	V_{51}	–	–	0.1	–	
52	Y2/G2 IN	V_{52}	–	2.0	2.3	2.6	
53	DC9(LINE2-2)	V_{53}	–	–	0.1	–	
54	Cr3/R3 IN	V_{54}	–	2.6	2.9	3.2	
55	DC10(LINE1-2)	V_{55}	–	–	0.1	–	
56	Cb3/B3 IN	V_{56}	–	2.6	2.9	3.2	
57	AR7 IN	V_{57}	–	4.2	4.4	4.6	
58	Y3/G3 IN	V_{58}	–	2.0	2.3	2.6	
59	AL7 IN	V_{59}	–	4.2	4.4	4.6	
60	SY2 IN	V_{60}	–	2.0	2.3	2.6	
61	AR8 IN	V_{61}	–	4.2	4.4	4.6	
62	SC2 IN	V_{62}	–	2.6	2.9	3.2	
63	AL8 IN	V_{63}	–	4.2	4.4	4.6	
64	MONITOR OUT	V_{64}	–	0.9	1.2	1.5	

Audio Block

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
I/O gain (AL/AR1, AL/AR2,)	Gauf	input = 2.8Vp-p, 1 kHz, input resistance 5.6 kΩ	-1.0	0	1.0	dB
I/O frequency characteristic	Fau	-3 dB point, NOTE A	100	—	—	kHz
Total harmonic distortion (AL/AR1, AL/AR2,)	thd	input = 2.8 Vp-p 1 kHz, NOTE A	—	0.02	0.05	%
Input dynamic range	Vdyau	NOTE A, NOTE B	5.6	6.5	—	Vp-p
Output offset voltage	Vauswof	Offset on AU1(2) OUT between AU1(2) OUT = 0000 to 1000	-30	0	+30	mV
Ripple rejection ratio	Vrrr	100Hz and 100mVp-p ripple is added to AU Vcc, NOTE A	30	45	—	dB
Mute mode attenuation	Gaumute	input = 2.8Vp-p, 1 kHz, NOTE A	75	85	—	dB
Crosstalk among inputs	Gaucrs	input = 2.8Vp-p, 1 kHz, NOTE A	75	85	—	dB
S/N ratio	Gausn	input = 2.8Vp-p, 1 kHz, NOTE A	80	90	—	dB
Input impedance of input pins	Imau	Pins 26,28,30,32,33,35,37,39,41,43,45,47 ,57,59,61,63	65	87	109	kΩ

NOTE A: These parameters are not tested during production and are provided only as information to assist the design of applications.

NOTE B: Input = 1kHz, the amplitude at which the total harmonic distortion becomes 1%.

Video Block

Characteristic		Symbol	Test Conditions	Min	Typ.	Max	Unit
Input dynamic range	Sync-tip clamp mode	Vdsync	FILPASS = 0, BANDWIDTH = max, Sine wave input for Bias mode, Y with sync for others.	1.5	1.7	–	Vp-p
	Sync-tip clamp GCA mode	Vdsyncgca		1.5	1.7	–	
	Bias mode	Vdbias		1.4	2.1	–	
	Monitor out	Vdmoni		1.35	1.5	–	
I/O gain	GAIN = -3dB	G-3	YCbCr-OUT FILPASS = 0/1, input = 0.2Vp-p 10 kHz, BANDWIDTH = cnt, f0 SW = 1	-3.5	-3.0	-2.5	dB
	GAIN = 0dB	G0		-0.5	0	0.5	
	GAIN = +3dB	G+3		2.5	3.0	3.5	
	GAIN = +6dB	G+6	MONITOR OUT	5.5	6.0	6.5	
	GCA min	Gmin	Input = 0.2Vpp 10kHz BUS setting Y/CVBS GAIN=-3dB	–	–	-6.5	
	GCA cnt	Gcnt		–	-3.3	–	
	GCA max	Gmax		4.5	–	–	
YC MIX gain		Gycmy	SY-IN to MONITOR-OUT, No input into SC-IN, YC MIX = 1	5.5	6.0	6.5	dB
		Gycmc	SC-IN to MONITOR-OUT, No input into SY-IN, YC MIX = 1	5.5	6.0	6.5	

Characteristic		Symbol	Test Conditions	Min	Typ.	Max	Unit
I/O frequency characteristic 1-1 (YCbCr)	YCbCr GAIN = -3dB	fg-3	FILPASS = 1, 0.2 Vp-p input, -3 dB point, NOTE A	80	100	–	MHz
	YCbCr GAIN = 0dB	Fg0		80	100	–	
	YCbCr GAIN = +3dB	fg+3		80	100	–	
I/O frequency characteristic 1-2 (YCbCr)	BANDWIDTH = max	fLmax	FILPASS = 0, GAIN = 00, f0 SW =0, 0.2 Vp-p input, -3 dB point, NOTE A	14.0	16.5	18.0	MHz
	BANDWIDTH = cnt	fLcnt		9.5	10.5	11.5	
	BANDWIDTH = min	fLmin		4.0	4.5	5.0	
I/O frequency characteristic 1-3 (YCbCr)	BANDWIDTH = max	fHmax	FILPASS = 0, GAIN = 00, f0 SW = 1, 0.2 Vp-p input, -3 dB point, NOTE A	41	46	51	MHz
	BANDWIDTH = cnt	fHcnt		27	30.3	34	
	BANDWIDTH = min	fHmin		12	13.4	15	
I/O frequency characteristic 1-4 (CbCr)	BANDWIDTH = max	fhfLmax	FILPASS = 0, GAIN = 00, f0 SW = 0, fc HALF = 1, -3 dB point, NOTE A	7.4	8.3	9.1	MHz
	BANDWIDTH = cnt	fhfLcnt		4.6	5.2	5.8	
	BANDWIDTH = min	fhfLmin		2.1	2.4	2.6	
I/O frequency characteristic 1-5 (CbCr)	BANDWIDTH = max	fhfHmax	FILPASS = 0, GAIN = 00, f0 SW = 1, fc HALF = 1, 0.2 Vp-p input, -3 dB point, NOTE A	21	24.1	27	MHz
	BANDWIDTH = cnt	fhfHcnt		14	15.7	18	
	BANDWIDTH = min	fhfHmin		6.0	6.8	8.0	
Differential 1-1 of frequency characteristic among YCbCr outputs	YCbCr GAIN = -3dB	Fdg-3	FILPASS = 1, 0.2 Vp-p input, -3 dB point, NOTE A	–	0	–	MHz
	YCbCr GAIN = 0dB	Fdg0		–	0	–	
	YCbCr GAIN = +3dB	Fdg+3		–	0	–	
Differential 1-2 of frequency characteristic among YCbCr outputs	BANDWIDTH = max	fdHmax	FILPASS = 0, f0 SW = 0, 0.2 Vp-p input, -3 dB point, NOTE A	-0.90	0	0.90	MHz
	BANDWIDTH = cnt	fdLcnt		-0.5	0	0.5	
	BANDWIDTH = min	fdHmin		-0.23	0	0.23	
Differential 1-3 of frequency characteristic among YCbCr outputs	BANDWIDTH = max	fdHmax	FILPASS = 0, f0 SW = 1, 0.2 Vp-p input, -3 dB point, NOTE A	-3.2	0	3.2	MHz
	BANDWIDTH = cnt	fdHcnt		-1.05	0	1.05	
	BANDWIDTH = min	fdHmin		-0.70	0	0.70	
I/O delay time 1-1 (YCbCr)	YCbCr GAIN = -3dB	TdL-3	FILPASS = 1, 1 MHz, NOTE A	–	4	10	ns
	YCbCr GAIN = 0dB	TdL0		–	4	10	
	YCbCr GAIN = +3dB	TdL+3		–	4	10	
I/O delay time 1-2 (YCbCr)	BANDWIDTH = max	TdLmax	FILPASS = 0, GAIN = 00, f0 SW = 0, 1 MHz, NOTE A	28	33	38	ns
	BANDWIDTH = cnt	TdLcnt		45	48	55	
	BANDWIDTH = min	TdLmin		96	107	120	
I/O delay time 1-3 (YCbCr)	BANDWIDTH = max	TdHmax	FILPASS = 0, GAIN = 00, f0 SW = 1, 1 MHz, NOTE A	10	16	20	ns
	BANDWIDTH = cnt	TdHcnt		15	20	25	
	BANDWIDTH = min	TdHmin		35	39	45	

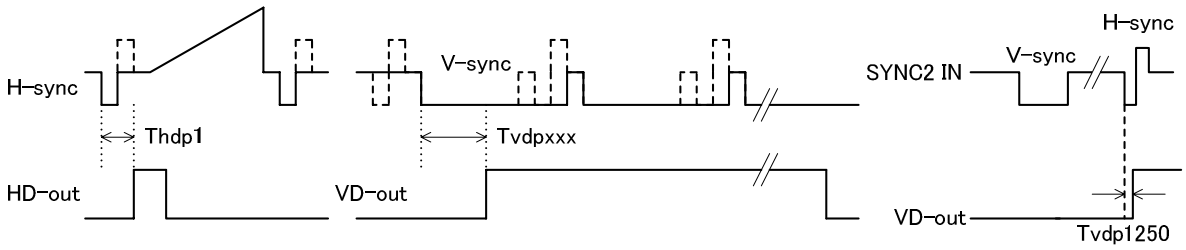
Characteristic		Symbol	Test Conditions	Min	Typ.	Max	Unit
I/O delay time 1-4 (CbCr)	BANDWIDTH = max	TdhfLmax	FILPASS = 0, GAIN = 00, f0 SW = 0, fc HALF = 1, 1 MHz, NOTE A	55	60	65	ns
	BANDWIDTH = cnt	TdhfLcnt		80	91	100	
	BANDWIDTH = min	TdhfLmin		190	220	260	
I/O delay time 1-5 (CbCr)	BANDWIDTH = max	TdhfHmax	FILPASS = 0, GAIN = 00, f0 SW = 1, fc HALF = 1, 1 MHz, NOTE A	20	24	30	ns
	BANDWIDTH = cnt	TdhfHcnt		29	34	39	
	BANDWIDTH = min	TdhfHmin		66	72	80	
Differential 1-1 of delay time among YCbCr outputs	YCbCr GAIN = -3dB	Tddg-3	FILPASS = 1, 1 MHz, NOTE A	-10	0	10	ns
	YCbCr GAIN = 0dB	Tddg0		-10	0	10	
	YCbCr GAIN = +3dB	Tddg+3		-10	0	10	
Differential 1-2 of delay time among YCbCr outputs	BANDWIDTH = max	TddHmax	FILPASS = 0, f0 SW = 0, 1 MHz, NOTE A	-10	0	10	ns
	BANDWIDTH = cnt	TddHcnt		-10	0	10	
	BANDWIDTH = min	TddHmin		-10	0	10	
Differential 1-3 of delay time between Y and Cb/Cr outputs	BANDWIDTH = max	TddHmax	FILPASS = 0, f0 SW = 1, fc HALF = 1, 1 MHz, NOTE A	0	8	20	ns
	BANDWIDTH = cnt	TddHcnt		5	14	20	
	BANDWIDTH = min	TddHmin		25	33	45	
Differential 1-4 of delay time between Cb and Cr outputs	BANDWIDTH = max	TddHmax	FILPASS = 0, f0 SW = 0, fc HALF = 1, 1 MHz, NOTE A	-10	0	10	ns
	BANDWIDTH = cnt	TddHcnt		-10	0	10	
	BANDWIDTH = min	TddHmin		-20	0	20	
I/O frequency characteristic 2 (CVBS,GCA)	GCA GAIN = min	fdgcamin	FILPASS = 1, 0.2 Vp-p input, -3 dB point, NOTE A	–	30	–	MHz
	GCA GAIN = cnt	fdgcacnt		–	30	–	
	GCA GAIN = max	fdgcamax		–	30	–	
I/O delay time 2 (CVBS,GCA)	GCA GAIN = min	TgdLmin	FILPASS = 1, 1 MHz, NOTE A	–	10	20	ns
	GCA GAIN = cnt	TgdLcnt		–	10	20	
	GCA GAIN = max	TgdLmax		–	10	20	
I/O frequency characteristic 3 (MONITOR)		fgm	0.2 Vp-p input, -3 dB point, NOTE A	60	80	–	MHz
Mute mode attenuation		Gmute	5 MHz sin wave input, NOTE A	–	-70	-60	dB
Crosstalk	Among input channels	Gcrschs	5 MHz sin wave input, NOTE A	–	-70	-60	dB
	Among inputs in a channel	Gcrsins		–	-60	-55	
	HD/VD/ SYNC-in to Video-out	Gcrsync	BANDWIDTH=min, NOTE A	–	3.4	–	mV

Synchronization Block (Test condition: A-SYNC = 1 (ON))

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
H/V-sync separation level	525/60i	Vsep100	HV-SEP = 00, NOTE A, NOTE C	12	18	24	%
		Vsep101	HV-SEP = 01, NOTE A, NOTE C	20	26	32	
		Vsep110	HV-SEP = 10, NOTE A, NOTE C	26	31	38	
		Vsep111	HV-SEP = 11, NOTE A, NOTE C	38	43	50	
	1125/60i	Vsep200	HV-SEP = 00, NOTE A, NOTE C	20	25	30	%
		Vsep201	HV-SEP = 01, NOTE A, NOTE C	27	33	38	
		Vsep210	HV-SEP = 10, NOTE A, NOTE C	33	38	45	
		Vsep211	HV-SEP = 11, NOTE A, NOTE C	45	50	55	
	SVGA/60	Vsep300	HV-SEP = 00, NOTE A, NOTE C	14	20	26	%
		Vsep301	HV-SEP = 01, NOTE A, NOTE C	21	27	33	
		Vsep310	HV-SEP = 10, NOTE A, NOTE C	25	33	39	
		Vsep311	HV-SEP = 11, NOTE A, NOTE C	37	44	50	
Threshold amplitude for HD input		VthHD	HV OUT = 1	0.8	–	–	Vp-p
Threshold amplitude for VD input		VthVDn	HV OUT = 1	0.9	–	–	Vp-p
HD-OUT voltage		VhdH	High level	1.0	1.2	1.4	V
		VhdL	Low level	–	0.1	0.4	
HD-OUT width		Thdw0	HD WIDTH = 0	-	1.7	-	us
		Thdw1	HD WIDTH = 1	-	0.7	-	
HD-OUT phase	H sync-in to HD-out	Thdp1	HV OUT = 0, 1125/60p input, NOTE D	-	90	-	ns
	HD-in to HD-out	Thdp2	HV OUT = 1, NOTE A	-	20	-	ns
VD-OUT voltage		VvdH	High level	1.0	1.2	1.4	V
		VvdL	Low level	–	0.1	0.4	
VD-OUT width	Sync sep	Tvdws	Separated VD-OUT	–	290	–	us
	1250i ODD	Tvdwodd	When 1250i input	–	285	–	us
	1250i EVEN	Tvdweven		–	270	–	
	Free-run 1	Tvdwfi	Free-run VD-OUT in interlace mode	–	4	–	H
	Free-run 2	Tvdwfp	Free-run VD-OUT in progressive mode	–	8	–	
VD-OUT phase	V sync-in to VD-out	Tvdp	Except 1250/50i input, NOTE D	–	0.20	–	H
	H sync-in to VD-out	Tvdp1250	1250/50i input, H sync-in to VD-out, NOTE D	–	320	–	ns
	VD-in to VD-out	Tvdphv	HV OUT = 1, NOTE A	–	20	–	ns

NOTE C: 286 mVp-p sync input for 525/60i, 0.3 Vp-p sync input for 1125/60i and SVGA/60.

NOTE D: See the following figures.



Characteristic	Symbol	Test Conditions	Min	Typ.	Max	Unit
Dummy HD-OUT frequency	fh156	HV FREQ2 = 00000, H DMY = 1	–	15.564	–	kHz
	fh157/60i	HV FREQ2 = 00001, H DMY = 1	–	15.701	–	
	fh312	HV FREQ2 = 00010, H DMY = 1	–	31.401	–	
	fh315	HV FREQ2 = 00011, H DMY = 1	–	31.401	–	
	fh281/50i	HV FREQ2 = 00100, H DMY = 1	–	27.966	–	
	fh337/60i	HV FREQ2 = 00101, H DMY = 1	–	33.771	–	
	fh375	HV FREQ2 = 00110, H DMY = 1	–	37.288	–	
	fh450	HV FREQ2 = 00111, H DMY = 1	–	44.746	–	
	fh1250	HV FREQ2 = 01000, H DMY = 1	–	31.401	–	
	fh379	HV FREQ2 = 01001, H DMY = 1	–	37.288	–	
	fh640	HV FREQ2 = 01010, H DMY = 1	–	66.288	–	
	fh750	HV FREQ2 = 01011, H DMY = 1	–	74.577	–	
	fh562	HV FREQ2 = 01100, H DMY = 1	–	55.932	–	
	fh157/30p	HV FREQ2 = 10000, H DMY = 1	–	15.700	–	
	fh270	HV FREQ2 = 10001, H DMY = 1	–	27.117	–	
	fh281/25p	HV FREQ2 = 10010, H DMY = 1	–	27.965	–	
	fh337/30p	HV FREQ2 = 10011, H DMY = 1	–	33.769	–	
	fh270/48sf	HV FREQ2 = 10100, H DMY = 1	–	27.117	–	
Dummy VD-OUT frequency	fv625i	HV FREQ2 = 00000, V DMY = 1	–	312.5	–	H
	fv525i	HV FREQ2 = 00001, V DMY = 1	–	262.5	–	
	fv625p	HV FREQ2 = 00010, V DMY = 1	–	625	–	
	fv525p	HV FREQ2 = 00011, V DMY = 1	–	525	–	
	fv1125i50	HV FREQ2 = 00100, V DMY = 1	–	562.5	–	
	fv1125i60	HV FREQ2 = 00101, V DMY = 1	–	562.5	–	
	fv750p50	HV FREQ2 = 00110, V DMY = 1	–	750	–	
	fv750p60	HV FREQ2 = 00111, V DMY = 1	–	750	–	
	fv1250iO	HV FREQ2 = 01000, V DMY = 1, ODD	–	624.5	–	
	fv1250iE	HV FREQ2 = 01000, V DMY = 1, EVEN	–	625.5	–	
	fvsvga	HV FREQ2 = 01001, V DMY = 1	–	628	–	
	fvsxga	HV FREQ2 = 01010, V DMY = 1	–	1066	–	
	fvuxga	HV FREQ2 = 01011, V DMY = 1	–	1250	–	
	fv1125p50	HV FREQ2 = 01100, V DMY = 1	–	1125	–	
	fv525p30	HV FREQ2 = 10000, V DMY = 1	–	525	–	
	fv1125p24	HV FREQ2 = 10001, V DMY = 1	–	1125	–	
	fv1125p25	HV FREQ2 = 10010, V DMY = 1	–	1125	–	
	fv1125p30	HV FREQ2 = 10011, V DMY = 1	–	1125	–	
	fv1125s24	HV FREQ2 = 10100, V DMY = 1	–	562.5	–	

Other Blocks

Characteristic		Symbol	Test Conditions	Min	Typ.	Max	Unit
XTAL oscillation amplitude		Vosc	NOTE A, NOTE E	–	0.4	–	Vp-p
No signal detection filter		tnsfil1	SIG LPF = 1, NOTE F, NOTE A	0.5	1.5	2.0	μs
Impedance for no signal detection filter		Imnsfil200	SIG DET IMPE = 00, NOTE G	14	20	26	kΩ
		Imnsfil201	SIG DET IMPE = 01, NOTE G	11	15	19	
		Imnsfil210	SIG DET IMPE = 10, NOTE G	7	10	13	
		Imnsfil211	SIG DET IMPE = 11, NOTE G	4.2	6.0	7.8	
No signal detection threshold voltage		Vthns00	SIG DET LVL = 00, NOTE H	0.45	0.55	0.65	V
		Vthns01	SIG DET LVL = 01, NOTE H	0.70	0.80	0.90	
		Vthns10	SIG DET LVL = 10, NOTE H	0.90	1.05	1.15	
		Vthns11	SIG DET LVL = 11, NOTE H	1.15	1.30	1.40	
DC detection threshold (DC)	L⇔M	VdcthLM	Pins 1,14,27,29,31,34,49,51,53,55	0.8	1.0	1.2	V
	M⇔H	VdcthMH		2.8	3.0	3.2	
DC detection threshold (S)		VdcthS	Pins 38,44,48,50,56,62	0.8	1.0	1.2	V
Input impedance of DC detection pins		Imdc	Pins 1,14,27,29,31,34,49,51,53,55	100	150	-	kΩ

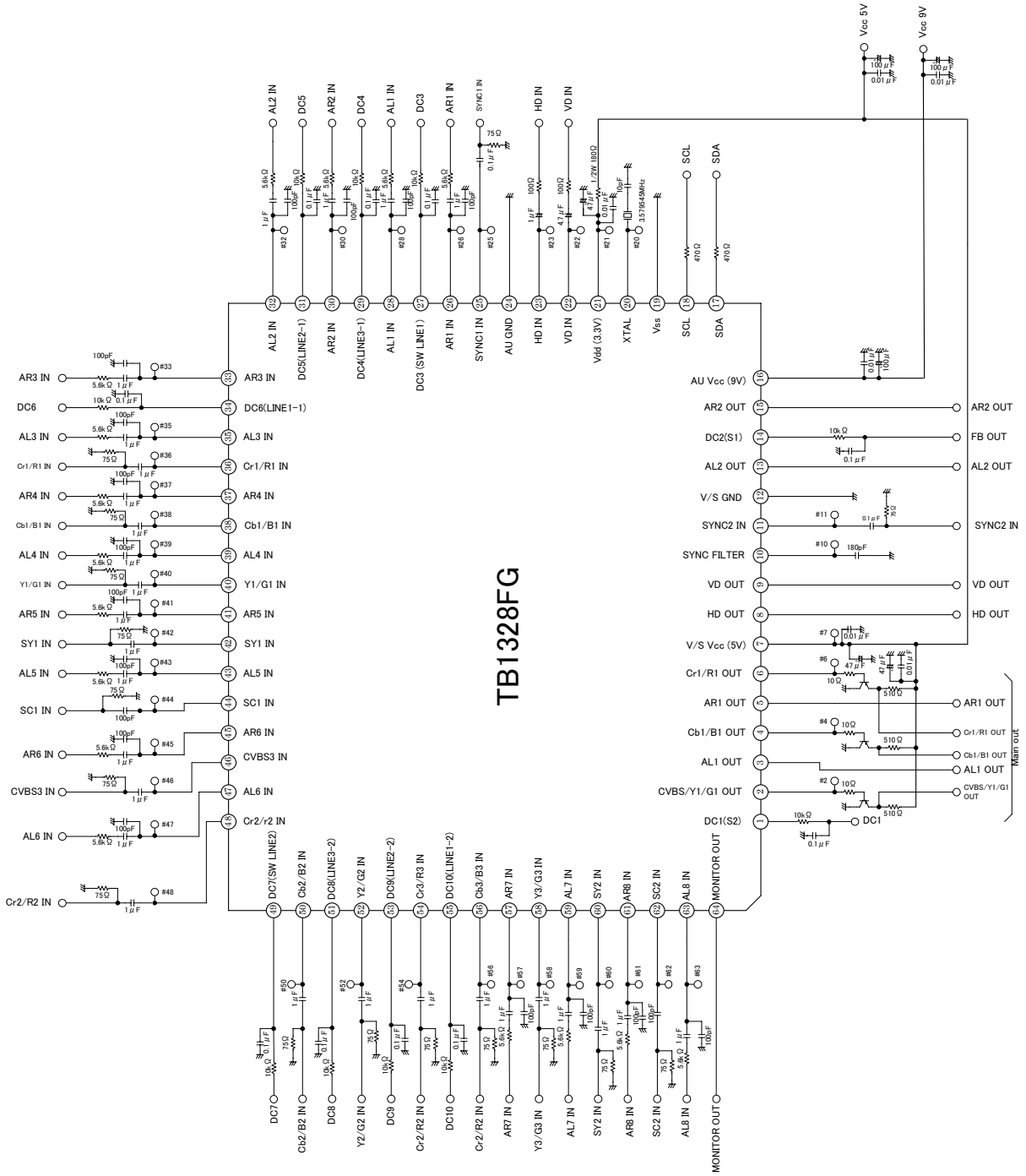
NOTE E: The amplitude of oscillation wave at the point between the crystal and the series capacitor.

NOTE F: Remove the external capacitor connected to SYNC FILTER pin (pin 10), HV SEP1 = 00, SIG DET SW = 1(SYNC-1IN), SIG DET IMPE=11. The delay time from SYNC1-IN input (525/60i) to SYNC FILTER wave form.

NOTE G: Remove the external capacitor connected to SYNC FILTER pin (pin 10). Connect 10 kΩ resistor between SYNC FILTER pin and GND. No input into SYNC1-IN. Measure the current (Ir) on the resistor. Imnsfil2xx = 3.3 / Ir - 10kΩ.

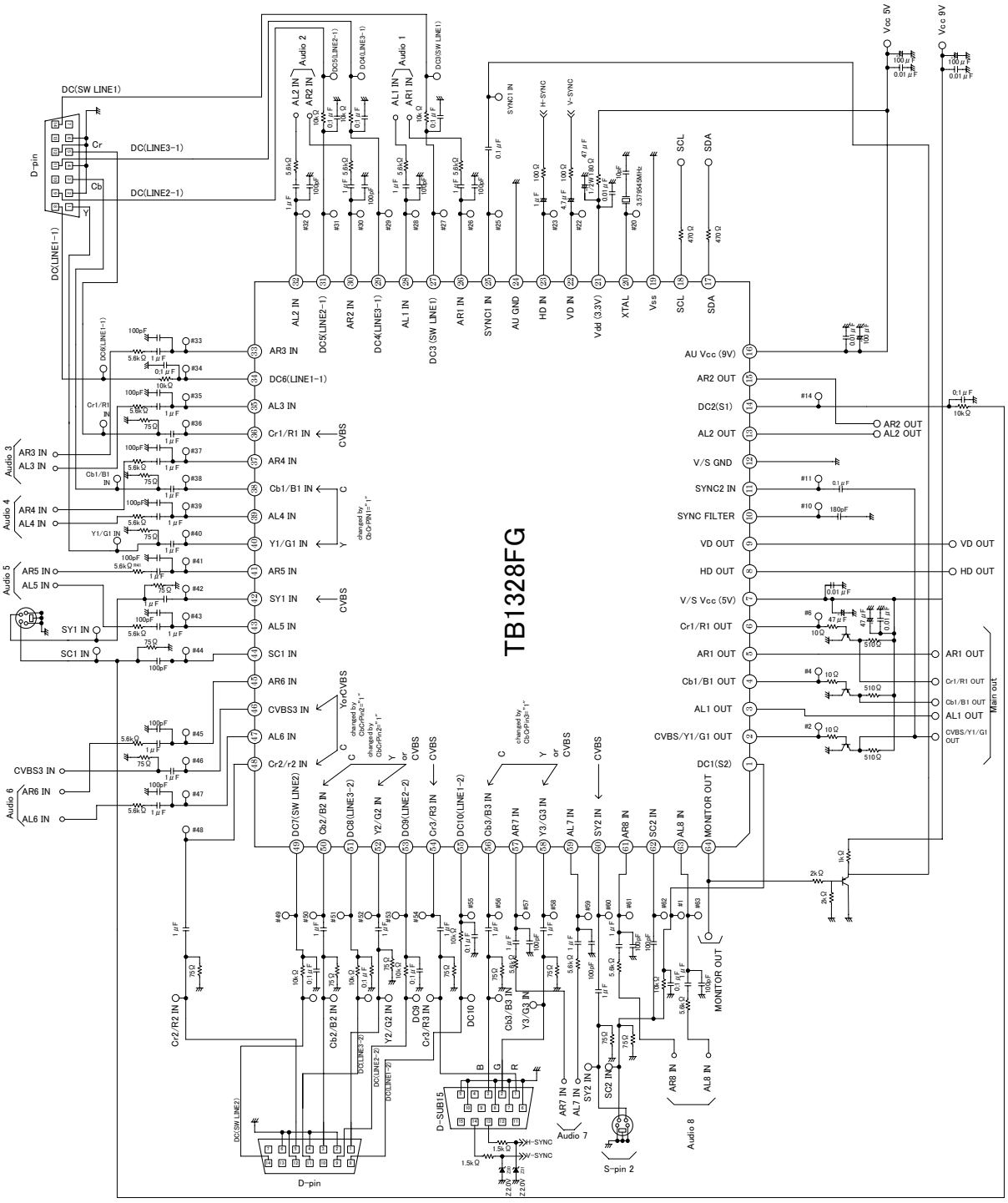
NOTE H: Remove the external capacitor connected to SYNC FILTER pin (pin 10). Input a 0V - Vthnsxx [V] pulse of 15.7 kHz into SYNC FILTER pin. The pulse voltage when SIG DET status changes.

Test circuit



Components in the test circuits are only used to obtain and confirm the device characteristics. These components and circuits do not warrant to prevent the application equipment from malfunction or failure.

Application circuit 1 (Typical values)



Input video signals, which are driven with low impedance.

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required especially in the mass production design phase.
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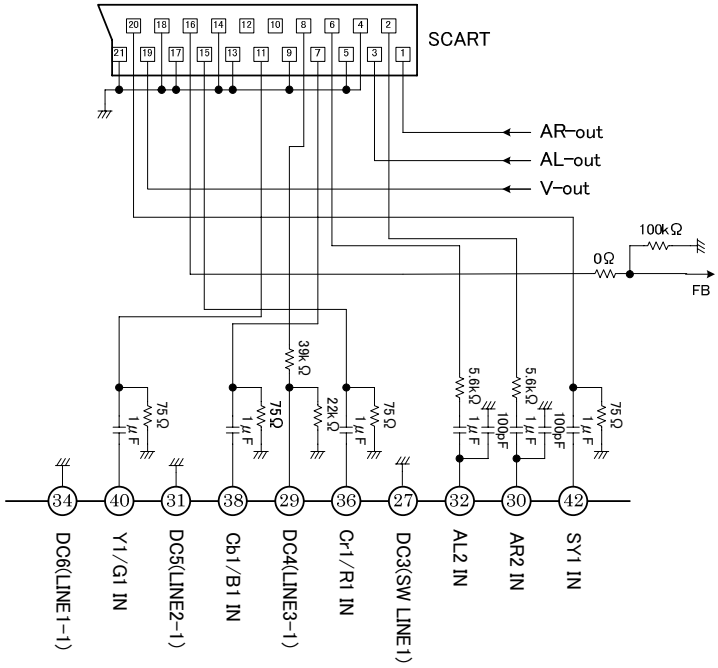
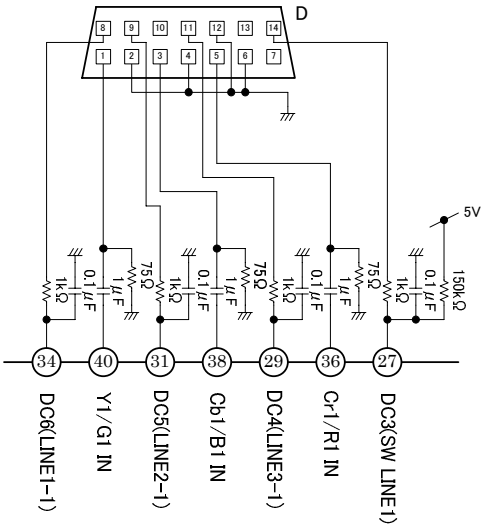
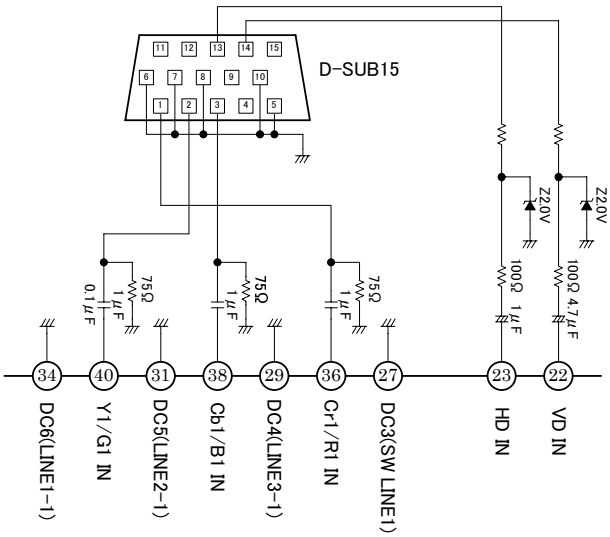
Application circuit 2 (Examples of Connectors)



SCART



D-pin



D-SUB15

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required especially in the mass production design phase.
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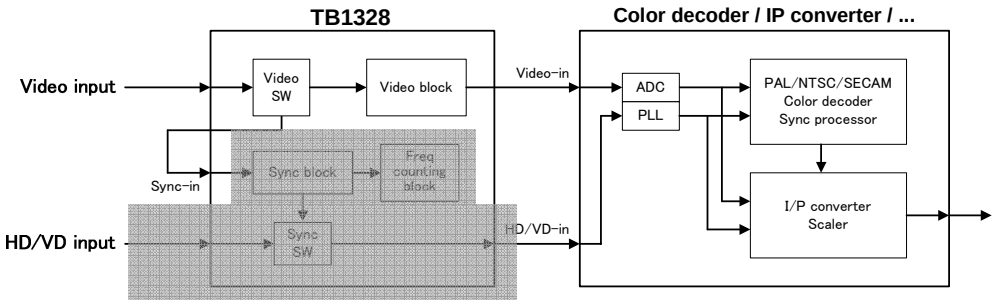
Application circuit 3 (system configuration)

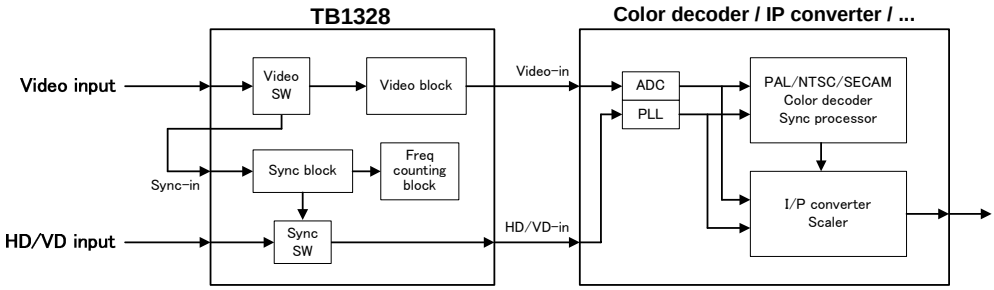
(1) For non-standard signals such as CVBS, YC (S-video), 525i, 625i, etc.



The TB1328FG cannot be used for non-standard signals such as weak strength signals, ghost signals, etc. Therefore, these signals should be dealt with through the use of another device such as a color-decoder which is capable of handling these signals. In such cases, the signal switcher and the video circuits of the TB1328FG can be used. Exceptionally, “the no signal detection” can be also used for those signals.

The TB1328FG cannot distinguish between component and RGB video. The different kinds of input signal should be separated through the use of different signal-specific input pins; for example, specific-purpose pins for RGB video input only or component video input only.

(2) For standard component video (SMPTE STANDARD) and standard RGB video (VESA STANDARD)



The TB1328FG can detect the format type of standard signal inputs.

The application circuits shown in this document are examples provided for reference purposes only. Thorough evaluation is required especially in the mass production design phase.
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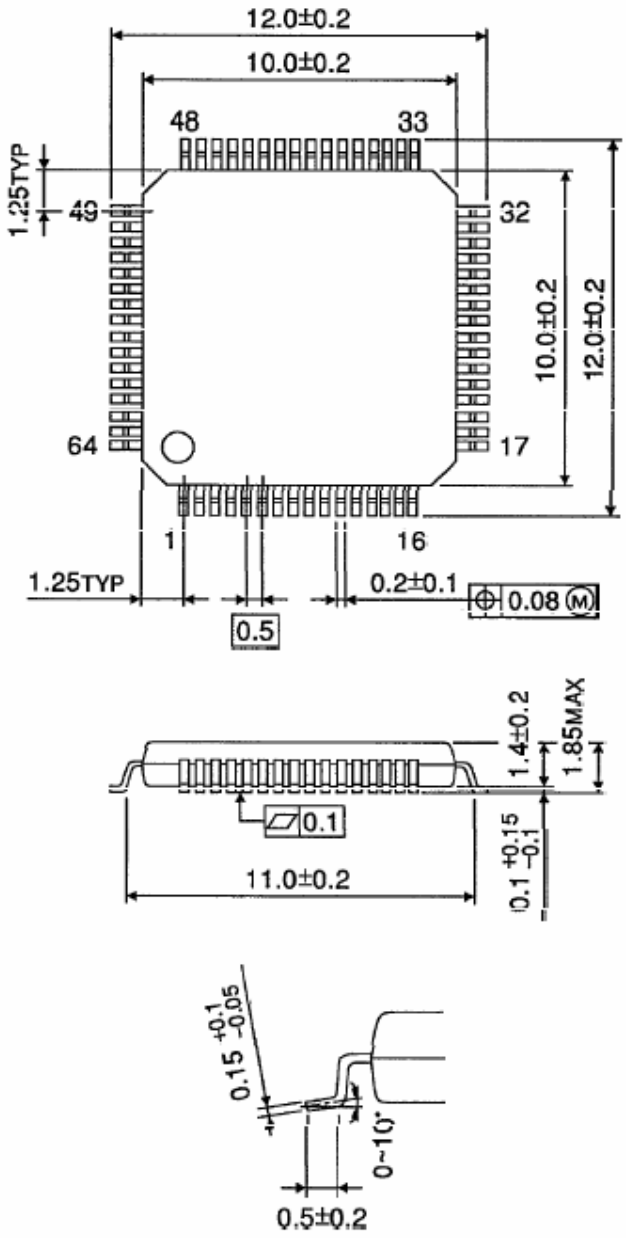
Package dimensions

LQFP64-P-1010-0.50A Unit: mm



Weight: 0.34 g (Typ.)

About solderability, following conditions were confirmed

- Solderability

  (1) Use of Sn-37Pb solder Bath
  - solder bath temperature = 230°C
  - dipping time = 5 seconds
  - the number of times = once
  - use of R-type flux

  (2) Use of Sn-3.0Ag-0.5Cu solder Bath
  - solder bath temperature = 245°C
  - dipping time = 5 seconds
  - the number of times = once
  - use of R-type flux

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060116EBA

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