MOTOROLA

MCM4517

16,384-BIT DYNAMIC RAM

The MCM4517 is a 16,384-bit, high-speed, dynamic Random-Access Memory. Organized as 16,384 one-bit words and fabricated using HMOS high-performance, N-channel, silicon-gate technology. This new breed of 5-volt only dynamic RAM combines high performance with low cost and improved reliability.

By multiplexing row- and column-address inputs, the MCM4517 requires only seven address lines and permits packaging in standard 16-pin dual-in-line packages. Complete address decoding is done on chip with address latches incorporated. Data out is controlled by $\overline{CAS}$ allowing for greater system flexibility.

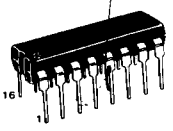
All inputs and outputs, including clocks, are fully TTL compatible. The MCM4517 incorporates a one-transistor cell design and dynamic storage techniques.

- Organized as 16,384 Words of 1 Bit
- Single +5 Volt Operation
- Fast 100 ns Operation
- Low Power Dissipation:
  170 mW Maximum (Active)
  14 mW Maximum (Standby)
- Maximum Access Time
  MCM4517-10 – 100 ns
  MCM4517-12 – 120 ns
  MCM4517-15 – 150 ns
  MCM4517-20 – 200 ns
- Three-State Data Output
- Internal Latches for Address and Data Input
- Early-Write Common I/O Output Capability
- 64K Compatible 128-cycle, 2 ms Refresh
- $\overline{RAS}$-only Refresh Mode
- $\overline{CAS}$ Controlled Output
- Upward Pin Compatibility from the 16K RAM (MCM4116) to the 64K RAM (MCM6664)
- Allows Undershoot V_{IL} min = −2 V
- Hidden $\overline{RAS}$ Only Refresh Capability

MOS

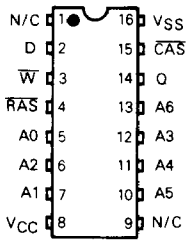
(N-CHANNEL, SILICON-GATE)

16,384-BIT DYNAMIC RAM



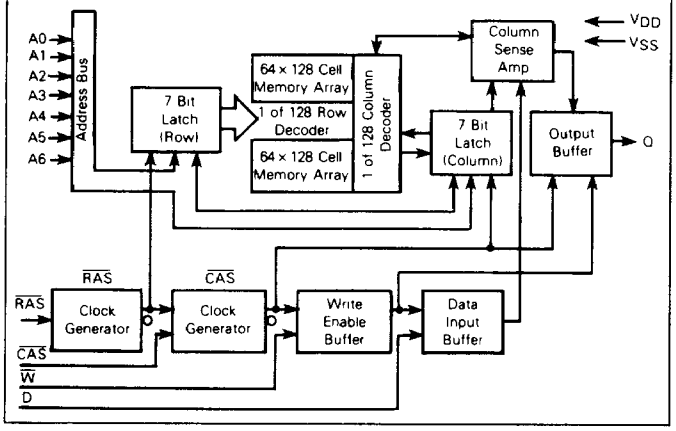
P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



PIN NAMES	
A0-A6	Address Input
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5 V)
V_{SS}	Ground

BLOCK DIAGRAM



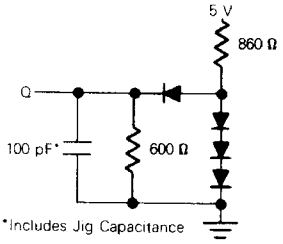
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_{in}, V_{out}	−2 to +7	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Power Dissipation	P_D	1.0	W
Data Out Current	I_{out}	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

FIGURE 1 — OUTPUT LOAD



DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full Operating Voltage and Temperature Range Unless Otherwise Noted.)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	V_{CC} V_{SS}	4.5 0	5.0 0	5.5 0	V	1
Logic 1 Voltage, All Inputs	V_{IH}	2.4	–	V_{CC}+1	V	1
Logic 0 Voltage, All Inputs	V_{IL}	−2.0	–	0.8	V	1

DC CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Units	Notes
V_{CC} Supply Current (Standby)	I_{CC1}	–	1.8	2.5	mA	5
V_{CC} Supply Current (Operating) 4517-10, t_{RC} = 235 4517-12, t_{RC} = 270 4517-15, t_{RC} = 320 4517-20, t_{RC} = 350	I_{CC2}	– – – –	22 20 18 16	31 28 25 23	mA	4
V_{CC} Supply Current (RAS-Only Cycle) 4517-10, t_{RC} = 235 4517-12, t_{RC} = 270 4517-15, t_{RC} = 320 4517-20, t_{RC} = 350	I_{CC3}	– – – –	14 12 11 10	23 21 19 18	mA	4
V_{CC} Standby Current (Standby, Output Enable) ($\overline{CAS}$ at V_{IL}, $\overline{RAS}$ at V_{IH})	I_{CC4}	–	2	5	mA	
V_{CC} Supply Current (Page Mode Cycle Only) 4517-10, t_{RC} = 235 4517-12, t_{RC} = 270 4517-15, t_{RC} = 320 4517-20, t_{RC} = 350	I_{CC5}	– – – –	17 15 13 10	23 21 18 15	mA	
Input Leakage Current (Any Input) ($V_{SS} \le V_{in} \le V_{CC}$)	$I_{I(L)}$	–	–	10	μA	
Output Leakage Current ($0 \le V_{out} \le 5.5$) ($\overline{CAS}$ at Logic 1)	$I_{O(L)}$	–	–	10	μA	
Output Logic 1 Voltage@I_{out} = −4 mA	V_{OH}	2.4	–	–	V	
Output Logic 0 Voltage@I_{out} = 4 mA	V_{OL}	–	–	0.4	V	

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full Operating Voltage and Temperature Range Unless Otherwise Noted)

(See Notes 2, 3, 9, 14 and Figure 1)

Parameter	Symbol	MCM4517-10		MCM4517-12		MCM4517-15		MCM4517-20		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	235	–	270	–	320	–	360	–	ns	8, 9
Read-Modify-Write Cycle Time	t_{RWC}	285	–	320	–	410	–	440	–	ns	8, 9
Access Time from Row Address Strobe	t_{RAC}	–	100	–	120	–	150	–	200	ns	10, 12
Access Time from Column Address Strobe	t_{CAC}	–	55	–	65	–	80	–	120	ns	11, 12
Output Buffer and Turn-Off Delay	t_{OFF}	0	45	0	50	0	60	0	70	ns	18
Row Address Strobe Precharge Time	t_{RP}	110	–	120	–	135	–	150	–	ns	
Row Address Strobe Pulse Width	t_{RAS}	115	10000	140	10000	175	10000	200	10000	ns	19
Column Address Strobe Pulse Width	t_{CAS}	55	10000	65	10000	95	10000	120	10000	ns	19
Row to Column Strobe Lead Time	t_{RCD}	25	45	25	55	25	70	30	80	ns	13
Row Address Setup Time	t_{ASR}	0	–	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	15	–	15	–	20	–	25	–	ns	
Column Address Setup Time	t_{ASC}	0	–	0	–	0	–	0	–	ns	
Column Address Hold Time	t_{CAH}	15	–	15	–	20	–	20	–	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}	60	–	70	–	90	–	140	–	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	ns	6

AC OPERATING CONDITIONS AND CHARACTERISTICS (Continued)

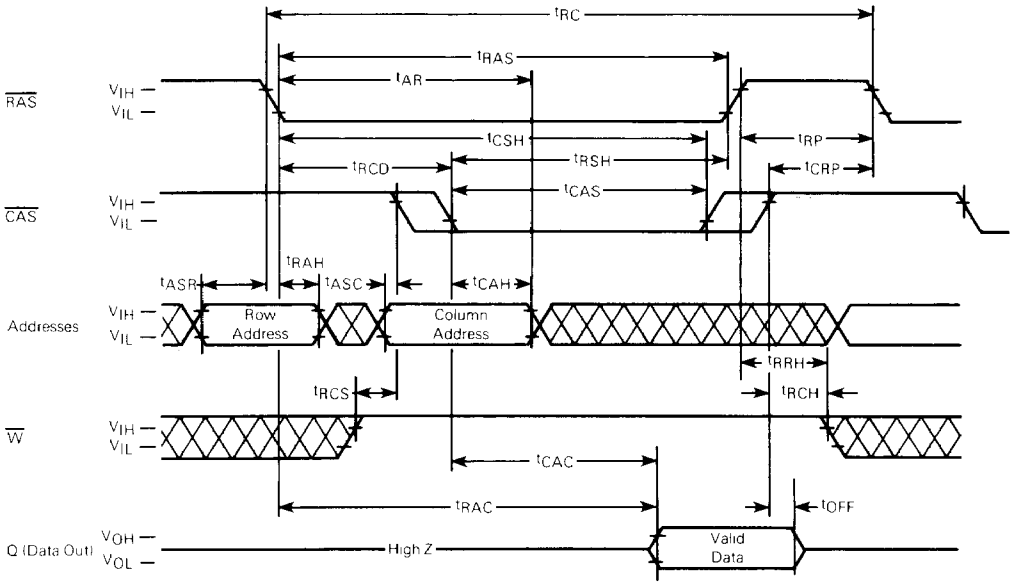
Parameter	Symbol	MCM4517-10		MCM4517-12		MCM4517-15		MCM4517-20		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Command Setup Time	t_{RCS}	0	–	0	–	0	–	0	–	ns	
Read Command Hold Time	t_{RCH}	0	–	0	–	0	–	0	–	ns	14
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	20	–	25	–	35	–	40	–	ns	14
Write Command Hold Time	t_{WCH}	25	–	30	–	45	–	60	–	ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}	70	–	85	–	115	–	140	–	ns	
Write Command Pulse Width	t_{WP}	25	–	30	–	50	–	50	–	ns	
Write Command to Row Strobe Lead Time	t_{RWL}	60	–	65	–	110	–	110	–	ns	
Write Command to Column Strobe Lead Time	t_{CWL}	45	–	50	–	100	–	100	–	ns	
Data in Setup Time	t_{DS}	0	–	0	–	0	–	0	–	ns	15
Data in Hold Time	t_{DH}	25	–	30	–	45	–	60	–	ns	15
Data in Hold Time Referenced to $\overline{RAS}$	t_{DHR}	70	–	85	–	115	–	140	–	ns	
Column to Row Strobe Precharge Time	t_{CRP}	0	–	0	–	0	–	0	–	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	70	–	85	–	105	–	120	–	ns	
Refresh Period	t_{RFSH}	–	2.0	–	2.0	–	2.0	–	2.0	ms	
Write Command Setup Time	t_{WCS}	0	–	0	–	0	–	0	–	ns	16
$\overline{CAS}$ to $\overline{WRITE}$ Delay	t_{CWD}	55	–	65	–	80	–	100	–	ns	16
$\overline{RAS}$ to $\overline{WRITE}$ Delay	t_{RWD}	100	–	120	–	150	–	160	–	ns	16
$\overline{CAS}$ Hold Time	t_{CSH}	100	–	120	–	165	–	200	–	ns	
$\overline{CAS}$ Precharge, Non Page Mode	t_{CPN}	50	–	55	–	70	–	90	–	ns	
RMW Cycle $\overline{RAS}$ Pulse Width	t_{RRW}	135	10000	160	10000	195	10000	220	10000	ns	
RMW Cycle $\overline{CAS}$ Pulse Width	t_{CRW}	95	10000	110	10000	130	10000	140	10000	ns	
Page Mode Cycle Time	t_{PC}	125	–	145	–	190	–	260	–	ns	
Page Mode Cycle Time (Read-Modify-Write)	t_{PCM}	175	–	200	–	280	–	360	–	ns	
$\overline{CAS}$ Precharge Time (Page Mode Cycle Only)	t_{CP}	60	–	70	–	85	–	105	–	ns	
$\overline{RAS}$ Pulse Width (Page Mode Cycle Only)	t_{RPM}	115	10000	140	10000	175	10000	235	10000	ns	

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = +5 V. Periodically sampled rather than 100% tested.)

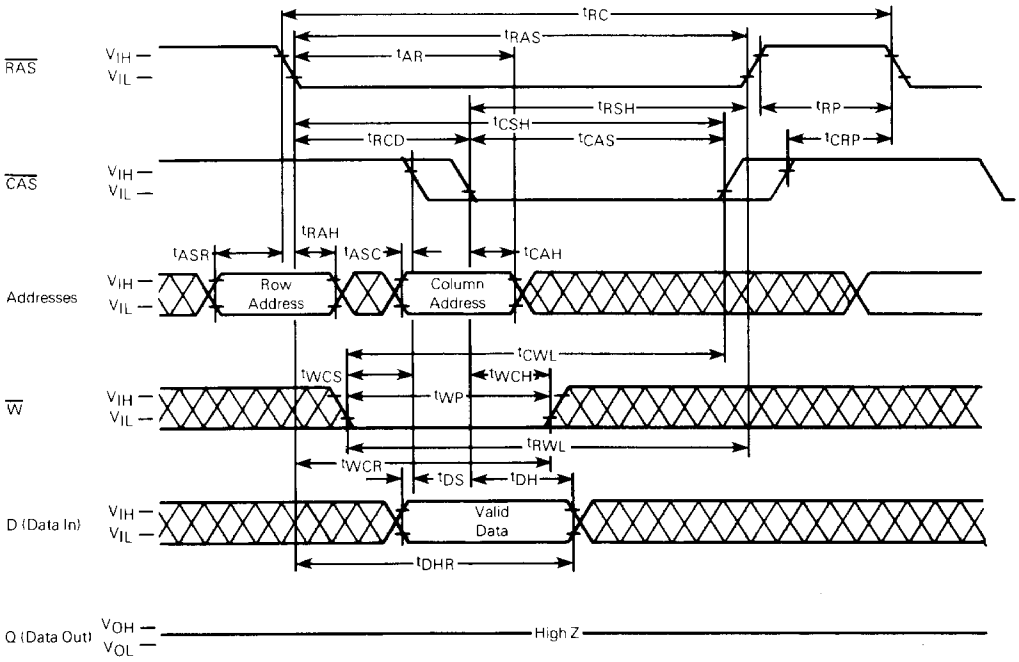
Parameter	Symbol	Typ	Max	Units	Notes
Input Capacitance (A0-A6), D_{in}	C_{I1}	4.0	5.0	pF	7
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{I2}	5.0	7.0	pF	7

NOTES:
1. All voltages referenced to V_{SS}.
2. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
3. An initial pause of 100 µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation guaranteed.
4. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
5. Output is disabled (open-circuit) and $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1.
6. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transmit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
7. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I_{\Delta t}/\Delta V$
8. The specifications for t_{RC} (min), and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
9. AC measurements assume t_T = 5.0 ns.
10. Assumes that $t_{RCD} \leq t_{RCD}$ (Max)
11. Assumes that $t_{RCD} \geq t_{RCD}$ (Max)
12. Measured with a current load equivalent to 2 TTL loads (+200 µA, −4 mA) and 100 pF (V_{OH} = 2.0 V, V_{OL} = 0.8 V).
13. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
16. t_{WCS}, t_{CWD}, and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
17. Addresses, data-in and $\overline{WRITE}$ are don't care. Data-out depends on the state of $\overline{CAS}$. If $\overline{CAS}$ remains low, the previous output will remain valid. $\overline{CAS}$ is allowed to make an active to inactive transition during the $\overline{RAS}$-only refresh cycle. When $\overline{CAS}$ is brought high, the output will assume a high-impedance state.
18. t_{off} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
19. For read and write cycles only.

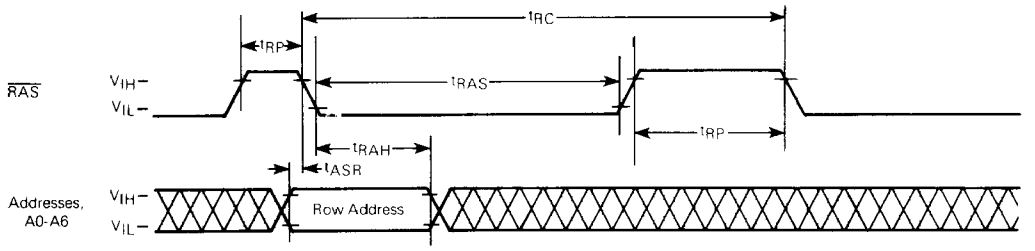
READ CYCLE TIMING



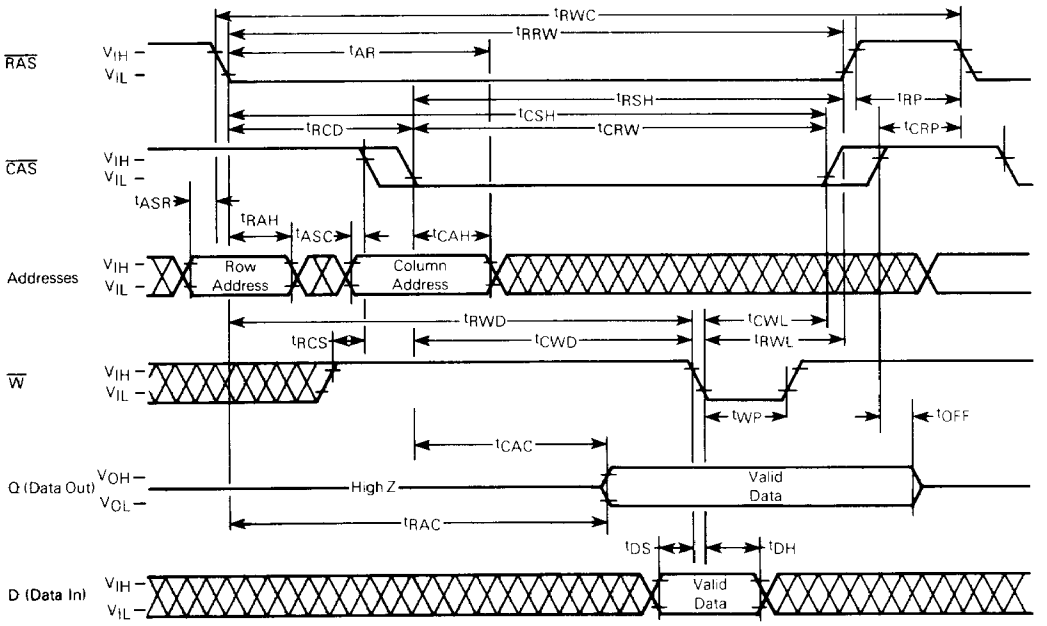
WRITE CYCLE TIMING



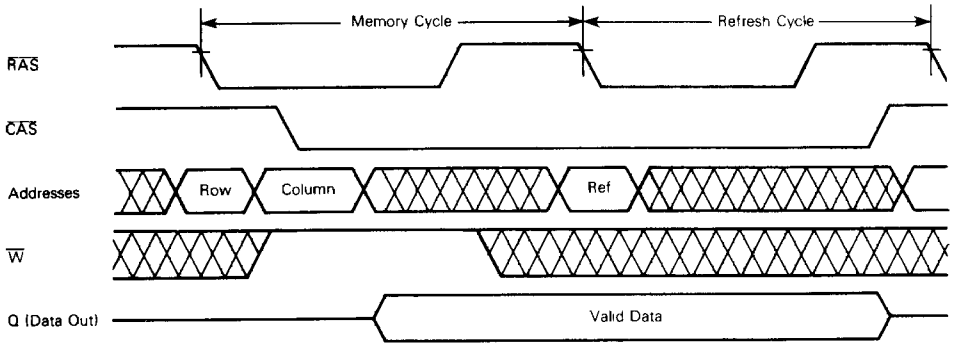
RAS-ONLY REFRESH CYCLE
(Data-In and Write are Don't Care, CAS is HIGH)



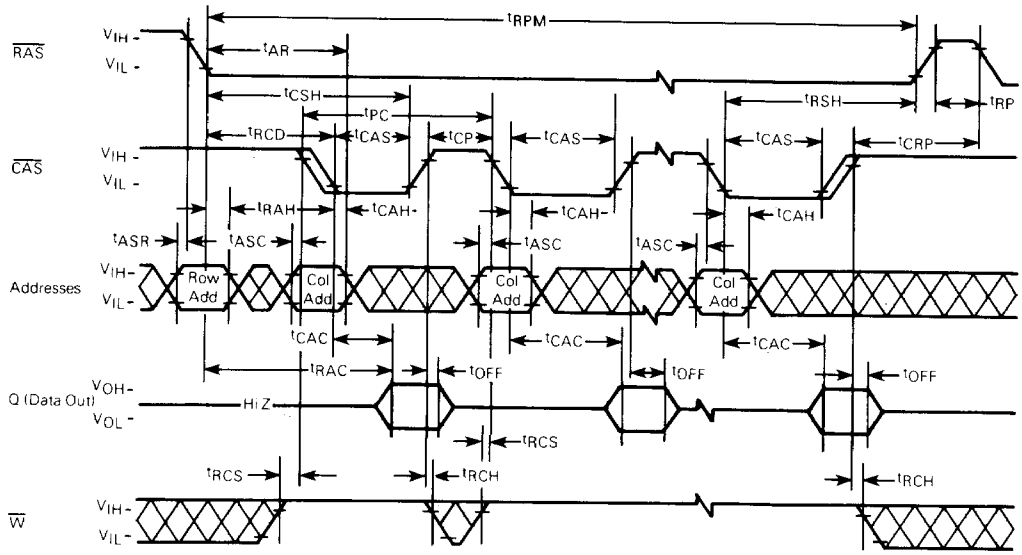
READ-WRITE/READ-MODIFY-WRITE CYCLE



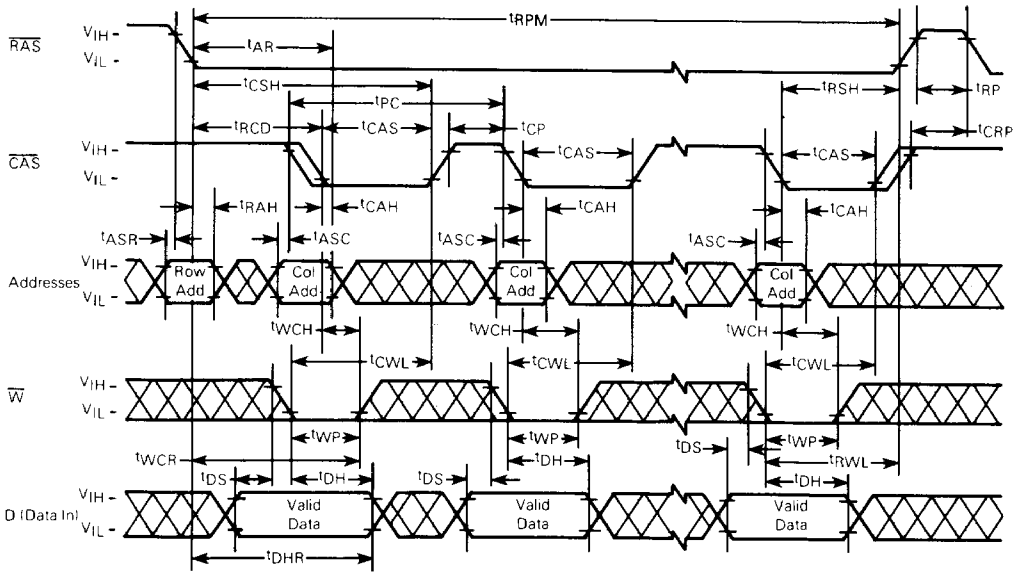
HIDDEN RAS-ONLY REFRESH CYCLE



PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



PAGE MODE READ-MODIFY-WRITE CYCLE