34 X 34 3.2 GBIT/S DIFFERENTIAL CROSSPOINT SWITCH S2080

FEATURES

- SiGe BiCMOS Technology
- 34 x 34 differential crosspoint switch
- Broadcast and multicast switching capability
- Differential 200 mV to 2200 mV input data (AC coupled input)
- Differential 400 mV to 1400 mV programmable output swing
- Up to 3.2 Gbps NRZ data rate
- LVTTL configuration controls
- Internal 100 Ω line-to-line terminations on high speed differential inputs
- Reconfigurable without disturbing operation
- Single +3.3 V supply or +2.7 V supply
- 6.5 W typical power dissipation with 800 mV output swing
- Compact 25 mm x 32.5 mm 474 pin CBGA package
- Complies with Bellcore and ITU–T standards

APPLICATIONS

- Dense Wavelength Division Multiplexing (DWDM) systems
- Internet switches
- Digital video
- Digital demultiplexing
- Microwave or fiber-optic data distribution
- High-speed automatic test equipment
- Datacom or telecom switching

GENERAL DESCRIPTION

The S2080 is a high speed 34 x 34 differential crosspoint switch with both full broadcast and multicast capability. Any of its 34 differential LVPECL input signal pairs can be connected to any or all of its 34 differential CML output signal pairs.

The differential logic data path makes the part ideal for high-speed applications. The differential nature of the data path is retained throughout the crosspoint structure to minimize data distortion and to handle NRZ data rates up to 3.2 gigabits per second. The high speed serial inputs to the S2080 are internally biased and have internal 100 Ω line-to-line terminations.

LVTTL configuration controls simplify interfacing to slower speed circuitry. Once a new configuration has been entered into the configuration register file, the S2080 can be completely reconfigured by pulsing the CONFIGN input.

Figure 1 shows a system block diagram incorporating the S2080 with other AMCC devices. Figure 2 shows the basic operation of the switch.

Figure 1. System Block Diagram

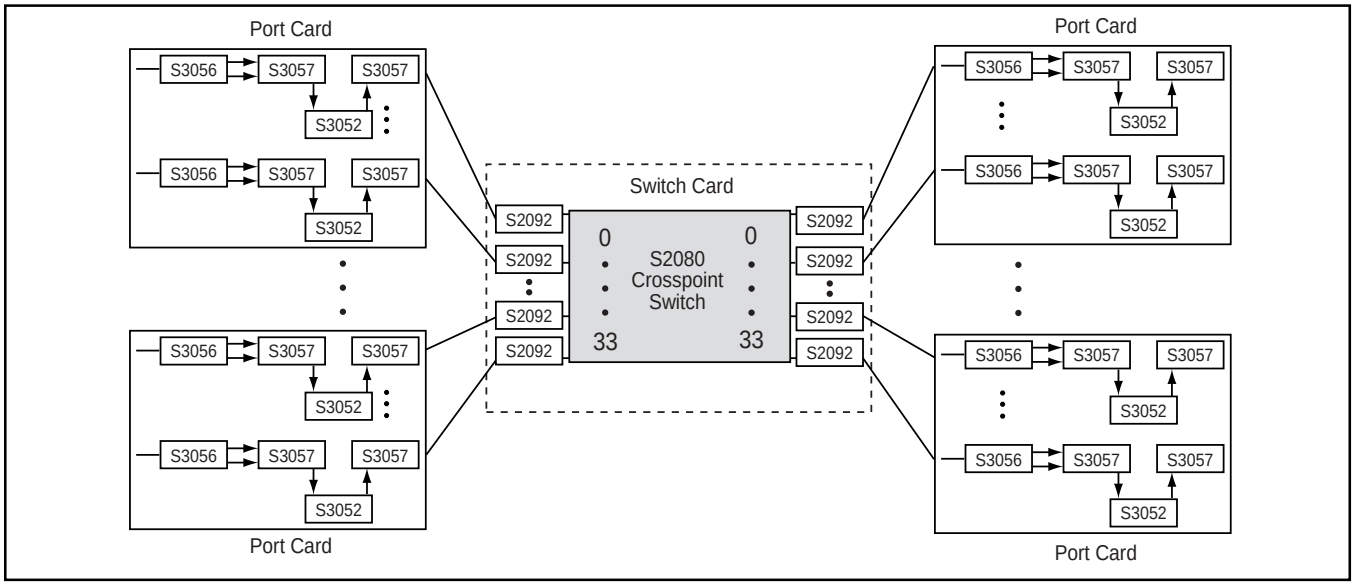


Figure 2. Functional Block Diagram

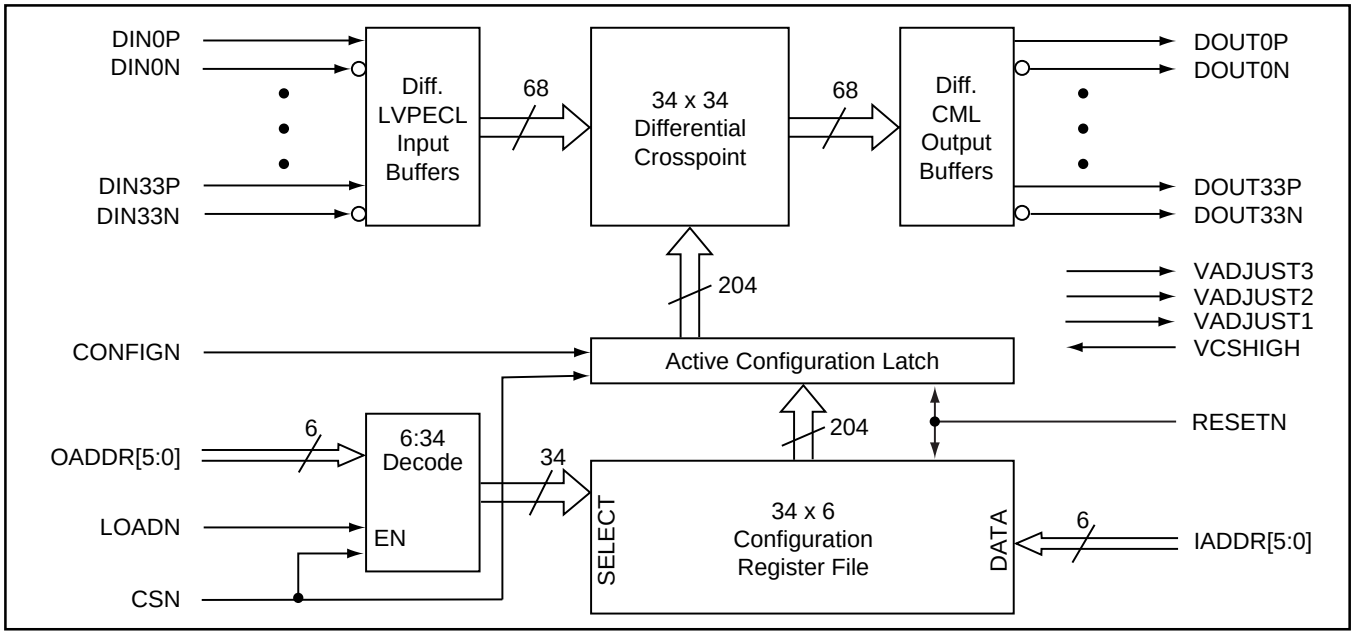


Table 1. Input/Output Address of S2080

DIFF INPUT	IADDR5	IADDR4	IADDR3	IADDR2	IADDR1	IADDR0	DIFF OUTPUT	OADDR5	OADDR4	OADDR3	OADDR2	OADDR1	OADDR0
DIN0	0	0	0	0	0	0	**DOUT0**	0	0	0	0	0	0
DIN1	0	0	0	0	0	1	**DOUT1**	0	0	0	0	0	1
DIN2	0	0	0	0	1	0	**DOUT2**	0	0	0	0	1	0
DIN3	0	0	0	0	1	1	**DOUT3**	0	0	0	0	1	1
DIN4	0	0	0	1	0	0	**DOUT4**	0	0	0	1	0	0
DIN5	0	0	0	1	0	1	**DOUT5**	0	0	0	1	0	1
DIN6	0	0	0	1	1	0	**DOUT6**	0	0	0	1	1	0
DIN7	0	0	0	1	1	1	**DOUT7**	0	0	0	1	1	1
DIN8	0	0	1	0	0	0	**DOUT8**	0	0	1	0	0	0
DIN9	0	0	1	0	0	1	**DOUT9**	0	0	1	0	0	1
DIN10	0	0	1	0	1	0	**DOUT10**	0	0	1	0	1	0
DIN11	0	0	1	0	1	1	**DOUT11**	0	0	1	0	1	1
DIN12	0	0	1	1	0	0	**DOUT12**	0	0	1	1	0	0
DIN13	0	0	1	1	0	1	**DOUT13**	0	0	1	1	0	1
DIN14	0	0	1	1	1	0	**DOUT14**	0	0	1	1	1	0
DIN15	0	0	1	1	1	1	**DOUT15**	0	0	1	1	1	1
DIN16	0	1	0	0	0	0	**DOUT16**	0	1	0	0	0	0
DIN17	0	1	0	0	0	1	**DOUT17**	0	1	0	0	0	1
DIN18	0	1	0	0	1	0	**DOUT18**	0	1	0	0	1	0
DIN19	0	1	0	0	1	1	**DOUT19**	0	1	0	0	1	1
DIN20	0	1	0	1	0	0	**DOUT20**	0	1	0	1	0	0
DIN21	0	1	0	1	0	1	**DOUT21**	0	1	0	1	0	1
DIN22	0	1	0	1	1	0	**DOUT22**	0	1	0	1	1	0
DIN23	0	1	0	1	1	1	**DOUT23**	0	1	0	1	1	1
DIN24	0	1	1	0	0	0	**DOUT24**	0	1	1	0	0	0
DIN25	0	1	1	0	0	1	**DOUT25**	0	1	1	0	0	1
DIN26	0	1	1	0	1	0	**DOUT26**	0	1	1	0	1	0
DIN27	0	1	1	0	1	1	**DOUT27**	0	1	1	0	1	1
DIN28	0	1	1	1	0	0	**DOUT28**	0	1	1	1	0	0
DIN29	0	1	1	1	0	1	**DOUT29**	0	1	1	1	0	1
DIN30	0	1	1	1	1	0	**DOUT30**	0	1	1	1	1	0
DIN31	0	1	1	1	1	1	**DOUT31**	0	1	1	1	1	1
DIN32	1	0	0	0	0	0	**DOUT32**	1	0	0	0	0	0
DIN33	1	x	x	x	x	1	**DOUT33**	1	x	x	x	x	1

Note: "x" denotes don't care.

DATA TRANSFER

For each configured connection between a differential input pair and an enabled output pair, any data appearing at the input pair will be passed immediately through to the output pair.

CONFIGURATION

The S2080 can be selectively configured one output pair at a time, or any number of output pairs simultaneously. Configuration data is stored in 34 registers, one register for each output pair. The data in these 34 registers make up the configuration register file. As shown in Figure 2, the configuration data is passed in parallel from all 34 registers to a latch, which holds the active switch configuration. This two-stage arrangement allows one or more output pairs to be configured simultaneously. A Chip Select pin (CSN) is provided to simplify interfacing this switch to the system microprocessor. When CSN is inactive, both the LOADN and CONFIGN signals will be ignored. Therefore, no new addresses or configurations will occur at the configuration register file or the active matrix. When CSN is active, the crosspoint will operate as specified.

The S2080 minimizes the configuration time through the use of the active configuration latch. While the switch is operational, and prior to the time at which it must be reconfigured, a new configuration is loaded into the configuration register file. Once the configuration register file contains the desired connection information, the contents of the registers are transferred in parallel to the active configuration latch by the CONFIGN strobe.

To connect an output to a given input, the output to be configured is selected using the OADDR[5:0] (OADDR5 = MSB) inputs. See Table 1. With the output configuration register selected, the desired input selection must be provided in the IADDR[5:0]I (IADDR5 = MSB) inputs. The IADDR[5:0] information is stored into the selected output configuration register by the LOADN strobe. The configuration process is described by the flow chart in Figure 5.

The active configuration latch can be made transparent by activating the CONFIGN input. When this is done, changes strobed into the output pair configuration registers by the LOADN input pair will be passed immediately to the switch.

The S2080 supports both broadcast and multicast operations: any of the 34 differential input pairs can be connected to any or all of the 34 differential output pairs.

OUTPUT SWING ADJUST

The S2080 output swing can be adjusted by connecting one or more of the VADJUSTx pins to the VCSHIGH pin according to Tables 2 and 3. Note that as the output swing is increased, the power dissipated by the part is proportionally increased (see Tables 13 and 14). The output swing range for +3.3 power supply is from 400 mVpp differential up to 1275 mVpp differential per Table 2. The output swing range for +2.7 V power supply is from 350 mVpp differential up to 1095 mVpp differential per Table 3.

Table 2. Output Swing Adjust Pin Settings (+3.3 V)

Output Setting #	VADJUST1	VADJUST2	VADJUST3	DOUTxx (mVpp Diff.)
1	O	T	O	400
2	T	T	O	580
3	O	O	T	765
4	T	O	T	940
5	O	T	T	1110
6	T	T	T	1275

Note: T = Ties pin(s) VADJUSTx to pin VCSHIGH
O = Open

Table 3. Output Swing Adjust Pin Settings (+2.7 V)

Output Setting #	VADJUST1	VADJUST2	VADJUST3	DOUTxx (mVpp Diff.)
1	O	T	O	350
2	T	T	O	510
3	O	O	T	670
4	T	O	T	820
5	O	T	T	960
6	T	T	T	1095

Note: T = Ties pin(s) VADJUSTx to pin VCSHIGH
O = Open

Figure 3. Data Transfer Waveforms

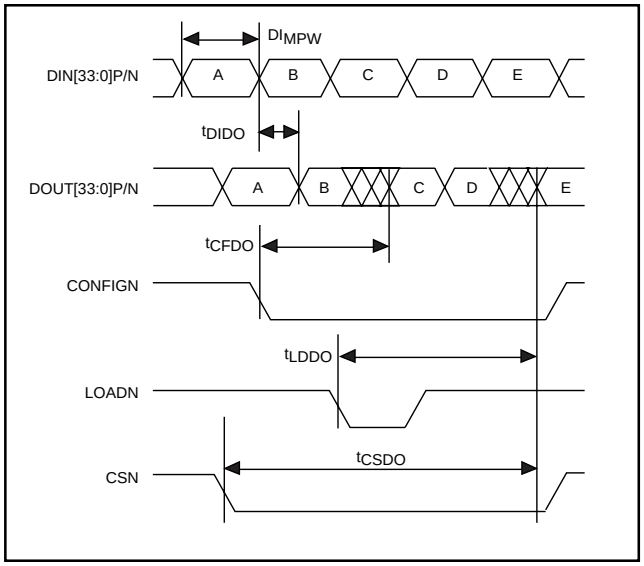
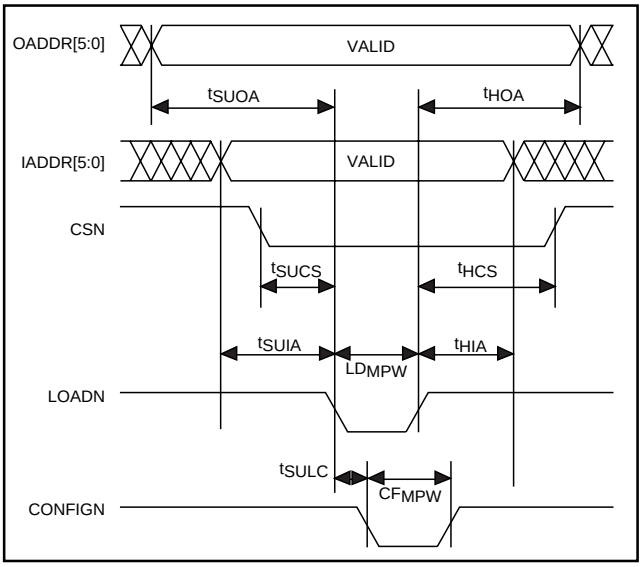


Figure 4. Reconfiguration Waveforms



RESET BEHAVIOR

During a RESETN assertion, the active configuration latch will be cleared of all existing data and will assume a configuration where the DIN0 input will go to all the outputs (DOUT0 through DOUT33, broadcast configuration). The configuration register file will retain its configuration information and is not affected by the RESETN assertion. The IC will remain in full broadcast mode until the inputs and outputs are explicitly reconfigured to be enabled.

POWER UP

Upon power up, the crosspoint will default to full broadcast mode (DINxx to all the outputs, DOUT0 through DOUT33). DINxx is determined by the state of the bits on IADDR[5:0] at the moment the device is powered up. The active configuration latch and the configuration register file will both have this configuration. The OADDR[5:0] bits will not have any affect on the configuration of the switch at power up. The IC will remain in full broadcast mode until the inputs and outputs are explicitly reconfigured to be enabled.

Figure 5. S2080 Configuration Flow Chart

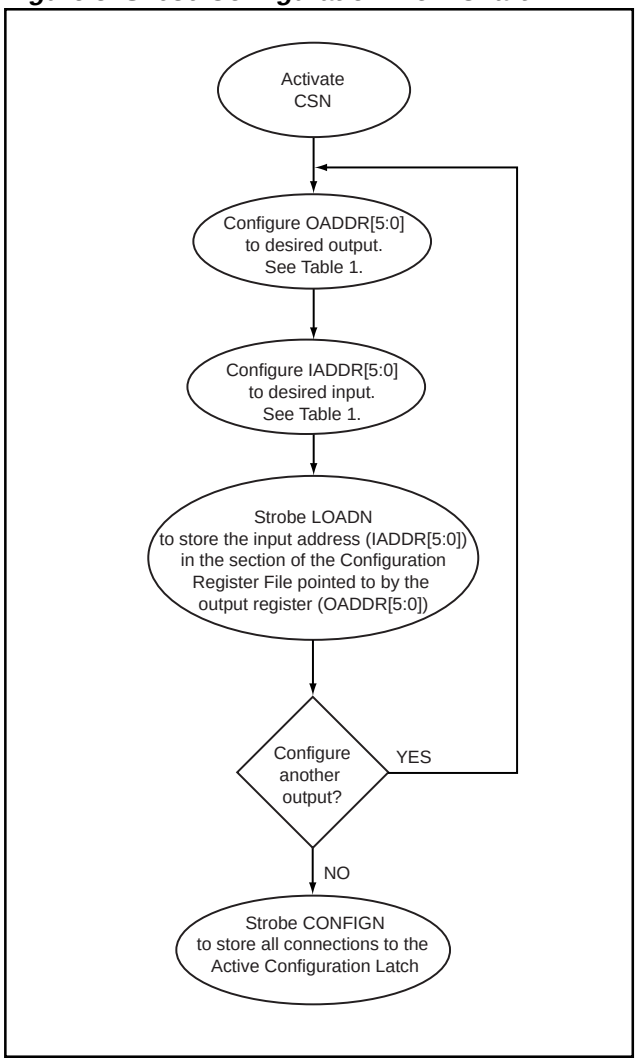


Table 4. Data Transfer Timing[1,2,3] (+3.3 V supply)

Parameter	Description	Min	Typ	Max	Units	Conditions
t_{DIDO}	Propagation delay from DIN[33:0]P/N to DOUT[33:0]P/N			2	ns	
t_{CFDO}	Propagation delay from falling edge of CONFIGN to DOUT[33:0]P/N valid			5	ns	
t_{LDDO}	Propagation delay from falling edge of LOADN to DOUT[33:0]P/N valid (when CONFIGN is held Low)			5	ns	
T_{CSDO}	Propagation delay from falling edge of CSN to DOUT[33:0]P/N valid (when CONFIGN is held Low)			6	ns	
F_{MAX}	Data Rate			3.2	Gbps	
T_{JITTER} RMS	Random jitter accumulation, any input to any output at: 3.2 Gbps 2.5 Gbps 1.5 Gbps 1.0 Gbps		 1.9 1.95 1.95 2.2	 2.8 2.8 2.8 2.8	 ps ps ps ps	RMS output jitter accumulated with K28.7 code. Tested on a sample basis.
T_{JITTER} DJ	Deterministic jitter accumulation, any input to any output at: 3.2 Gbps 2.5 Gbps 1.5 Gbps 1.0 Gbps		 17 17 17 17	 30 30 31 31	 ps ps ps ps	Deterministic output jitter accumulated with K28.5 pattern. Tested on a sample basis. Peak-to-peak.
T_{JITTER} CTK	Deterministic jitter accumulation due to crosstalk, any input to any output at: 3.2 Gbps 2.5 Gbps 1.5 Gbps 1.0 Gbps		 2.6 3.6 3.6 3.6	 4 4 5 5	 ps ps ps ps	Deterministic output jitter accumulated with K28.5 pattern. Tested on a sample basis. Peak-to-peak.
Skew [31:0]	Skew between paths from one or multiple inputs (DIN[31:0]) to multiple outputs (DOUT[33:0]). **Excludes DIN[33:32]**			85	ps	
Skew [33:0]	Skew between paths from multiple inputs (DIN[33:0]) to multiple outputs (DOUT[33:0]). **Includes DIN[33:32]**			460	ps	
$T_{r(out)}$, $T_{f(out)}$	Output Edge Rate (20% to 80%)			125	ps	100 Ω line-to-line.

1. All data transfer timing measured from the crossing point of the differential inputs to the crossing point of the differential outputs.
2. All LVTTL signals measured at the 1.5 V point.
3. All data measured with output setting # 3.

Table 5. Reconfiguration Timing[1] (+3.3 V supply)

Parameter	Description	Min	Typ	Max	Units
t_{SUIA}	Setup time of IADDR[5:0] before falling edge of LOADN	1			ns
t_{HIA}	Hold time of IADDR[5:0] after rising edge of LOADN	1			ns
t_{SUOA}	Setup time of OADDR[5:0] before falling edge of LOADN	2			ns
t_{HOA}	Hold time of OADDR[5:0] after rising edge of LOADN	2			ns
t_{SULC}	Setup time of LOADN to CONFIGN so that the falling edge of CONFIGN will start reconfiguration	2			ns
t_{SUCS}	Setup time of CSN before falling edge of LOADN	2			ns
t_{HCS}	Hold time of CSN after rising edge of LOADN	2			ns
LD_{MPW}	Pulse width Low of LOADN	2			ns
CF_{MPW}	Pulse width Low of CONFIGN	2			ns
$RESETN_{MPW}$	Pulse width Low of RESETN	4			ns
F_{MAX}	LOAD, CONFIGN			100	MHz

1. All reconfiguration timing measured from the 1.5 V point on the LVTTL signals.

Table 6. Data Transfer Timing[1,2,3] (+2.7 V supply)

Parameter	Description	Min	Typ	Max	Units	Conditions
t_{DIDO}	Propagation delay from DIN[33:0]P/N to DOUT[33:0]P/N			2	ns	
t_{CFDO}	Propagation delay from falling edge of CONFIGN to DOUT[33:0]P/N valid			5	ns	
t_{LDDO}	Propagation delay from falling edge of LOADN to DOUT[33:0]P/N valid (when CONFIGN is held Low)			5	ns	
T_{CSDO}	Propagation delay from falling edge of CSN to DOUT[33:0]P/N valid (when CONFIGN is held Low)			6	ns	
F_{MAX}	Data Rate			3.2	Gbps	
T_{JITTER} RMS	Random jitter accumulation, any input to any output at: 3.2 Gbps 2.5 Gbps 1.5 Gbps 1.0 Gbps		 1.95 2.0 2.0 2.1	 3.0 3.0 3.0 3.0	 ps ps ps ps	RMS output jitter accumulated with K28.7 code. Tested on a sample basis.
T_{JITTER} DJ	Deterministic jitter accumulation, any input to any output at: 3.2 Gbps 2.5 Gbps 1.5 Gbps 1.0 Gbps		 16 17 17 17	 30 31 35 35	 ps ps ps ps	Deterministic output jitter accumulated with K28.5 pattern. Tested on a sample basis. Peak-to-peak.
T_{JITTER} CTK	Deterministic jitter accumulation due to crosstalk, any input to any output at: 3.2 Gbps 2.5 Gbps 1.5 Gbps 1.0 Gbps		 1.2 2.0 2.0 2.0	 4 4 5 5	 ps ps ps ps	Deterministic output jitter accumulated with K28.5 pattern. Tested on a sample basis. Peak-to-peak.
Skew [31:0]	Skew between paths from one input (DIN[31:0]) to multiple outputs (DOUT[33:0]). **Excludes DIN[33:32]**			100	ps	
Skew [33:0]	Skew between paths from multiple inputs (DIN[33:0]) to multiple outputs (DOUT[33:0]). **Includes DIN[33:32]**			500	ps	
$T_{r(out)}$, $T_{f(out)}$	Output Edge Rate (20% to 80%)			135	ps	100 Ω line-to-line.

1. All data transfer timing measured from the crossing point of the differential inputs to the crossing point of the differential outputs.
2. All LVTTL signals measured at the 1.5 V point.
3. All data measured with output setting # 3.

Table 7. Reconfiguration Timing[1] (+2.7 V supply)

Parameter	Description	Min	Typ	Max	Units
t_{SUIA}	Setup time of IADDR[5:0] before falling edge of LOADN	1			ns
t_{HIA}	Hold time of IADDR[5:0] after rising edge of LOADN	1			ns
t_{SUOA}	Setup time of OADDR[5:0] before falling edge of LOADN	2			ns
t_{HOA}	Hold time of OADDR[5:0] after rising edge of LOADN	2			ns
t_{SULC}	Setup time of LOADN to CONFIGN so that the falling edge of CONFIGN will start reconfiguration	2			ns
t_{SUCS}	Setup time of CSN before falling edge of LOADN	2			ns
t_{HCS}	Hold time of CSN after rising edge of LOADN	2			ns
LD_{MPW}	Pulse width Low of LOADN	2			ns
CF_{MPW}	Pulse width Low of CONFIGN	2			ns
$RESETN_{MPW}$	Pulse width Low of RESETN	4			ns
F_{MAX}	LOAD, CONFIGN			100	MHz

1. All reconfiguration timing measured from the 1.5 V point on the LVTTL signals.

Table 8. Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
DIN33P	Diff. LVPECL	I	P2	Input data. Differential. Internally biased and terminated with 100 Ω line-to-line.
DIN33N			P3	
DIN32P			N1	
DIN32N			N2	
DIN31P			M2	
DIN31N			M3	
DIN30P			L1	
DIN30N			L2	
DIN29P			K2	
DIN29N			K3	
DIN28P			J1	
DIN28N			J2	
DIN27P			H2	
DIN27N			H3	
DIN26P			G1	
DIN26N			G2	
DIN25P			F2	
DIN25N			F3	
DIN24P			E1	
DIN24N			E2	
DIN23P			D2	
DIN23N			D3	
DIN22P			C1	
DIN22N			C2	
DIN21P			A3	
DIN21N			B3	
DIN20P			B4	
DIN20N			C4	
DIN19P			A5	
DIN19N			B5	
DIN18P			B6	
DIN18N			C6	
DIN17P			A7	
DIN17N			B7	
DIN16P			B8	
DIN16N			C8	
DIN15P			AE9	
DIN15N			AD9	
DIN14P			AD8	
DIN14N			AC8	
DIN13P			AE7	
DIN13N			AD7	
DIN12P			AD6	
DIN12N			AC6	
DIN11P			AE5	
DIN11N			AD5	
DIN10P			AD4	
DIN10N			AC4	
DIN9P			AE3	
DIN9N			AD3	
DIN8P			AC1	
DIN8N			AC2	
DIN7P			AB2	
DIN7N			AB3	
DIN6P			AA1	
DIN6N			AA2	
DIN5P			Y2	
DIN5N			Y3	

Table 8. Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
DIN4P DIN4N DIN3P DIN3N DIN2P DIN2N DIN1P DIN1N DIN0P DIN0N	Diff. LVPECL	I	W1 W2 V2 V3 U1 U2 T2 T3 R1 R2	Input data. Differential. Internally biased and terminated with 100 Ω line-to-line.
OADDR5 OADDR4 OADDR3 OADDR2 OADDR1 OADDR0	LVTTL	I	N7 N6 N5 M7 M6 M5	Output Address. Used to select an output configuration register in the configuration register file. See Table 1.
IADDR5 IADDR4 IADDR3 IADDR2 IADDR1 IADDR0	LVTTL	I	U7 U6 U5 T7 T6 T5	Input Address. IADDR[5:0] selects the input pair to connect to the output pair selected by OADDR[5:0]. See Table 1.
LOADN	LVTTL	I	J6	Load strobe. Active Low. When active, stores the configuration data in IADDR[5:0] into the configuration register file.
CONFIGN	LVTTL	I	J7	Configuration strobe. Active Low. When active, parallel loads the contents of the configuration register file into the active configuration latch.
RESETN	LVTTL	I	H5	Reset. Active Low. Clears the active configuration file of existing data and the configuration register file retains its configuration information. The default configuration will be broadcast on the active configuration file. The configuration register file is not affected by reset.
VCSHIGH		I	N14	Output Voltage Swing Adjust. Tied to VADJUSTx pin(s) to set the output voltage swing. See Tables 2 and 3 for details.
VADJUST1 VADJUST2 VADJUST3		O	P15 N15 M15	Voltage Adjust. These three pins, selectively tied to VCSHIGH, create a coded output which sets the output voltage swing. Tables 2 and 3 describe the settings for adjustable output swings at different power supplies.
CSN	LVTTL	I	J5	Chip Select. Active Low. When inactive, both the LOADN and CONFIGN signals will be ignored. New addresses and configurations will not be allowed. When active, the S2080 will operate as specified.

Table 8. Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
DOUT33P	Diff. CML	O	N19	Output data. Differential.
DOUT33N			N18	
DOUT32P			M18	
DOUT32N			M17	
DOUT31P			L19	
DOUT31N			L18	
DOUT30P			K18	
DOUT30N			K17	
DOUT29P			J19	
DOUT29N			J18	
DOUT28P			H18	
DOUT28N			H17	
DOUT27P			G19	
DOUT27N			G18	
DOUT26P			F18	
DOUT26N			F17	
DOUT25P			E19	
DOUT25N			E18	
DOUT24P			D18	
DOUT24N			D17	
DOUT23P			C19	
DOUT23N			C18	
DOUT22P			A17	
DOUT22N			B17	
DOUT21P			B16	
DOUT21N			C16	
DOUT20P			A15	
DOUT20N			B15	
DOUT19P			B14	
DOUT19N			C14	
DOUT18P			A13	
DOUT18N			B13	
DOUT17P			B12	
DOUT17N			C12	
DOUT16P			A11	
DOUT16N			B11	
DOUT15P			AD12	
DOUT15N			AC12	
DOUT14P			AE13	
DOUT14N			AD13	
DOUT13P			AD14	
DOUT13N			AC14	
DOUT12P			AE15	
DOUT12N			AD15	
DOUT11P			AD16	
DOUT11N			AC16	
DOUT10P			AE17	
DOUT10N			AD17	
DOUT9P			AC19	
DOUT9N			AC18	
DOUT8P			AB18	
DOUT8N			AB17	

Table 8. Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
DOUT7P DOUT7N DOUT6P DOUT6N DOUT5P DOUT5N DOUT4P DOUT4N DOUT3P DOUT3N DOUT2P DOUT2N DOUT1P DOUT1N DOUT0P DOUT0N	Diff. CML	O	AA19 AA18 Y18 Y17 W19 W18 V18 V17 U19 U18 T18 T17 R19 R18 P18 P17	Output data. Differential.

Table 9. Power and Ground Signals

Pin Name	Quantity	Pin #	Description
VCCINPUT	24	A2, A9, B1, C3, C5, C7, C9, E3, G3, J3, L3, N3, R3, U3, W3, AA3, AB10, AC3, AC5, AC7, AC9, AD1, AD10, AE2	+3.3 V or +2.7 V Power supply. Power for high speed circuitry inputs.
GNDINPUT	37	A4, A6, A8, B2, B9, D1, D4, D6, D8, D9, F1, F4, H1, H4, K1, K4, M1, M4, P1, P4, T1, T4, V1, V4, Y1, Y4, AB1, AB4, AB6, AB8, AB9, AC10, AD2, AE4, AE6, AE8, AE10	Ground for high speed circuitry inputs.
VCCOUTPUT	24	A18, B10, B19, C11, C13, C15, C17, D10, E17, G17, J17, L17, N17, R17, U17, W17, AA17, AC11, AC13, AC15, AC17, AD19, AE11, AE18	+3.3 V or +2.7 V Power supply. Power for high speed circuitry outputs.
GNDOUTPUT	37	A10, A12, A14, A16, B18, C10, D11, D12, D14, D16, D19, F16, F19, H16, H19, K16, K19, M16, M19, P16, P19, T16, T19, V16, V19, Y16, Y19, AB11, AB12, AB14, AB16, AB19, AD11, AD18, AE12, AE14, AE16	Ground for high speed circuitry outputs.
VCCTTL	28	E5, E7, E9, F6, F8, G5, G7, H6, H8, K6, K8, L5, L7, M8, P6, P8, R5, R7, T8, V6, V8, W5, W7, Y6, Y8, AA5, AA7, AA9	+3.3 V or +2.7 V Power supply. Power for LVTTL inputs.

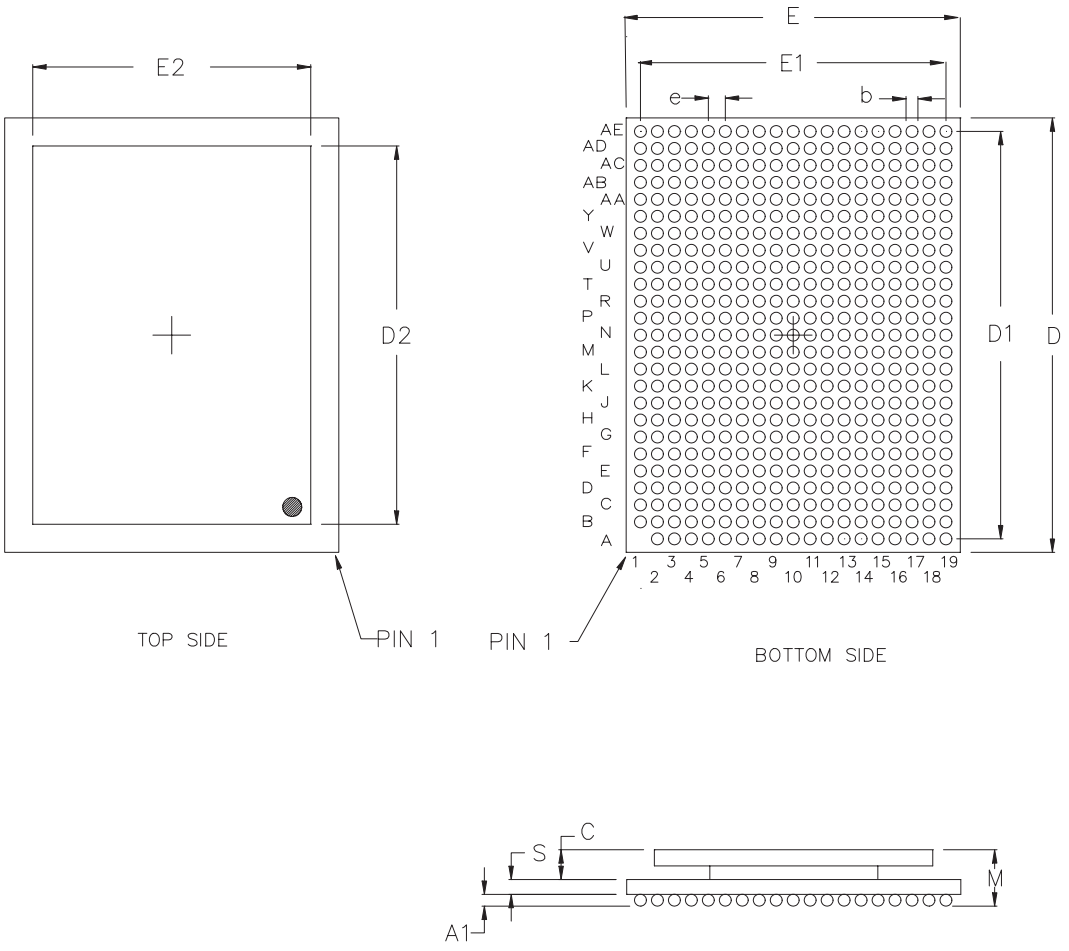
Table 9. Power and Ground Signals (Continued)

Pin Name	Quantity	Pin #	Description
GNDTTL	39	D5, D7, E4, E6, E8, F5, F7, G4, G6, G8, H7, J4, J8, K5, K7, L4, L6, L8, N4, N8, P5, P7, R4, R6, R8, U4, U8, V5, V7, W4, W6, W8, Y5, Y7, AA4, AA6, AA8, AB5, AB7	Ground for LVTTL inputs.
VCCCORE	68	E11, E13, E15, F9, F10, F11, F12, F13, F14, G15, H9, H10, H11, H12, H13, H14, J9, J10, J11, J12, J13, J15, K9, K10, K11, K12, K13, K14, L15, M9, M10, M11, M12, M13, P9, P10, P11, P12, P13, R15, T9, T10, T11, T12, T13, T14, U9, U10, U11, U12, U13, U15, V9, V10, V11, V12, V13, V14, W15, Y9, Y10, Y11, Y12, Y13, Y14, AA11, AA13, AA15	+3.3 V or +2.7 V Power supply. Power for core circuitry.
GNDCORE	58	D13, D15, E10, E12, E14, E16, F15, G9, G10, G11, G12, G13, G14, G16, H15, J14, J16, K15, L9, L10, L11, L12, L13, L14, L16, M14, N9, N10, N11, N12, N13, N16, P14, R9, R10, R11, R12, R13, R14, R16, T15, U14, U16, V15, W9, W10, W11, W12, W13, W14, W16, Y15, AA10, AA12, AA14, AA16, AB13, AB15	Ground for core circuitry.

Figure 6. S2080 Pinout (Top View) (Note: A1 is located at bottom right corner)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
AE		VCC OUTPUT	DOUT10P	GND OUTPUT	DOUT12P	GND OUTPUT	DOUT14P	GND OUTPUT	VCC OUTPUT	GNDINPUT	DIN15P	GNDINPUT	DIN13P	GNDINPUT	DIN11P	GNDINPUT	DIN9P	VCCINPUT	
AD	VCC OUTPUT	GND OUTPUT	DOUT10N	DOUT11P	DOUT12N	DOUT13P	DOUT14N	DOUT15P	GND OUTPUT	VCCINPUT	DIN15N	DIN14P	DIN13N	DIN12P	DIN11N	DIN10P	DIN9N	GNDINPUT	VCCINPUT
AC	DOUT9P	DOUT9N	VCC OUTPUT	DOUT11N	VCC OUTPUT	DOUT13N	VCC OUTPUT	DOUT15N	VCC OUTPUT	GNDINPUT	VCCINPUT	DIN14N	VCCINPUT	DIN12N	VCCINPUT	DIN10N	VCCINPUT	DIN8N	DIN8P
AB	GND OUTPUT	DOUT8P	DOUT8N	GND OUTPUT	GNDCORE	GND OUTPUT	GNDCORE	GND OUTPUT	GND OUTPUT	VCCINPUT	GNDINPUT	GNDINPUT	GNDTTL	GNDINPUT	GNDTTL	GNDINPUT	DIN7N	DIN7P	GNDINPUT
AA	DOUT7P	DOUT7N	VCC OUTPUT	GNDCORE	VCCCORE	GNDCORE	VCCCORE	GNDCORE	VCCCORE	GNDCORE	VCCTTL	GNDTTL	VCCTTL	GNDTTL	VCCTTL	GNDTTL	VCCINPUT	DIN6N	DIN6P
Y	GND OUTPUT	DOUT6P	DOUT6N	GND OUTPUT	GNDCORE	VCCCORE	VCCCORE	VCCCORE	VCCCORE	VCCCORE	VCCCORE	VCCTTL	GNDTTL	VCCTTL	GNDTTL	GNDINPUT	DIN5N	DIN5P	GNDINPUT
W	DOUT5P	DOUT5N	VCC OUTPUT	GNDCORE	VCCCORE	GNDCORE	GNDCORE	GNDCORE	GNDCORE	GNDCORE	GNDCORE	GNDTTL	VCCTTL	GNDTTL	VCCTTL	GNDTTL	VCCINPUT	DIN4N	DIN4P
V	GND OUTPUT	DOUT4P	DOUT4N	GND OUTPUT	GNDCORE	VCCCORE	VCCCORE	VCCCORE	VCCCORE	VCCCORE	VCCCORE	VCCTTL	GNDTTL	VCCTTL	GNDTTL	GNDINPUT	DIN3N	DIN3P	GNDINPUT
U	DOUT3P	DOUT3N	VCC OUTPUT	GNDCORE	VCCCORE	GNDCORE	VCCCORE	VCCCORE	VCCCORE	VCCCORE	VCCCORE	GNDTTL	IADDR5	IADDR4	IADDR3	GNDTTL	VCCINPUT	DIN2N	DIN2P
T	GND OUTPUT	DOUT2P	DOUT2N	GND OUTPUT	GNDCORE	VCCCORE	VCCCORE	VCCCORE	VCCCORE	VCCCORE	VCCCORE	VCCTTL	IADDR2	IADDR1	IADDR0	GNDINPUT	DIN1N	DIN1P	GNDINPUT
R	DOUT1P	DOUT1N	VCC OUTPUT	GNDCORE	VCCCORE	GNDCORE	GNDCORE	GNDCORE	GNDCORE	GNDCORE	GNDCORE	GNDTTL	VCCTTL	GNDTTL	VCCTTL	GNDTTL	VCCINPUT	DIN0N	DIN0P
P	GND OUTPUT	DOUT0P	DOUT0N	GND OUTPUT	VADJUST 1	GNDCORE	VCCCORE	VCCCORE	VCCCORE	VCCCORE	VCCCORE	VCCTTL	GNDTTL	VCCTTL	GNDTTL	GNDINPUT	DIN33N	DIN33P	GNDINPUT
N	DOUT33P	DOUT33N	VCC OUTPUT	GNDCORE	VADJUST 2	VCSHIGH	GNDCORE	GNDCORE	GNDCORE	GNDCORE	GNDCORE	GNDTTL	OADDR5	OADDR4	OADDR3	GNDTTL	VCCINPUT	DIN32N	DIN32P
M	GND OUTPUT	DOUT32P	DOUT32N	GND OUTPUT	VADJUST 3	GNDCORE	VCCCORE	VCCCORE	VCCCORE	VCCCORE	VCCCORE	VCCTTL	OADDR2	OADDR1	OADDR0	GNDINPUT	DIN31N	DIN31P	GNDINPUT
L	DOUT31P	DOUT31N	VCC OUTPUT	GNDCORE	VCCCORE	GNDCORE	GNDCORE	GNDCORE	GNDCORE	GNDCORE	GNDCORE	GNDTTL	VCCTTL	GNDTTL	VCCTTL	GNDTTL	VCCINPUT	DIN30N	DIN30P
K	GND OUTPUT	DOUT30P	DOUT30N	GND OUTPUT	GNDCORE	VCCCORE	VCCCORE	VCCCORE	VCCCORE	VCCCORE	VCCCORE	VCCTTL	GNDTTL	VCCTTL	GNDTTL	GNDINPUT	DIN29N	DIN29P	GNDINPUT
J	DOUT29P	DOUT29N	VCC OUTPUT	GNDCORE	VCCCORE	GNDCORE	VCCCORE	VCCCORE	VCCCORE	VCCCORE	VCCCORE	GNDTTL	CONFIGN	LOADN	CSN	GNDTTL	VCCINPUT	DIN28N	DIN28P
H	GND OUTPUT	DOUT28P	DOUT28N	GND OUTPUT	GNDCORE	VCCCORE	VCCCORE	VCCCORE	VCCCORE	VCCCORE	VCCCORE	VCCTTL	GNDTTL	VCCTTL	RESETN	GNDINPUT	DIN27N	DIN27P	GNDINPUT
G	DOUT27P	DOUT27N	VCC OUTPUT	GNDCORE	VCCCORE	GNDCORE	GNDCORE	GNDCORE	GNDCORE	GNDCORE	GNDCORE	GNDTTL	VCCTTL	GNDTTL	VCCTTL	GNDTTL	VCCINPUT	DIN26N	DIN26P
F	GND OUTPUT	DOUT26P	DOUT26N	GND OUTPUT	GNDCORE	VCCCORE	VCCCORE	VCCCORE	VCCCORE	VCCCORE	VCCCORE	VCCTTL	GNDTTL	VCCTTL	GNDTTL	GNDINPUT	DIN25N	DIN25P	GNDINPUT
E	DOUT25P	DOUT25N	VCC OUTPUT	GNDCORE	VCCCORE	GNDCORE	VCCCORE	GNDCORE	VCCCORE	GNDCORE	VCCTTL	GNDTTL	VCCTTL	GNDTTL	VCCTTL	GNDTTL	VCCINPUT	DIN24N	DIN24P
D	GND OUTPUT	DOUT24P	DOUT24N	GND OUTPUT	GNDCORE	GND OUTPUT	GNDCORE	GND OUTPUT	GND OUTPUT	VCC OUTPUT	GNDINPUT	GNDINPUT	GNDTTL	GNDINPUT	GNDTTL	GNDINPUT	DIN23N	DIN23P	GNDINPUT
C	DOUT23P	DOUT23N	VCC OUTPUT	DOUT21N	VCC OUTPUT	DOUT19N	VCC OUTPUT	DOUT17N	VCC OUTPUT	GND OUTPUT	VCCINPUT	DIN16N	VCCINPUT	DIN18N	VCCINPUT	DIN20N	VCCINPUT	DIN22N	DIN22P
B	VCC OUTPUT	GND OUTPUT	DOUT22N	DOUT21P	DOUT20N	DOUT19P	DOUT18N	DOUT17P	DOUT16N	VCC OUTPUT	GNDINPUT	DIN16P	DIN17N	DIN18P	DIN19N	DIN20P	DIN21N	GNDINPUT	VCCINPUT
A		VCC OUTPUT	DOUT22P	GND OUTPUT	DOUT20P	GND OUTPUT	DOUT18P	GND OUTPUT	DOUT16P	GND OUTPUT	VCCINPUT	GNDINPUT	DIN17P	GNDINPUT	DIN19P	GNDINPUT	DIN21P	VCCINPUT	

Figure 7. Compact 25 mm x 32.5 mm 474 Pin CBGA Package



DIMENSIONS (are in millimeters)

UNIT	A_1	S	C	M	D	D_1	D_2	E	E_1	E_2	b	e
MIN	0.80	2.00	2.60		32.30	30.28	30.25	24.80	22.66	23.25		1.27 BASIC
NOM	0.90		2.75		32.50	30.48	30.50	25.00	22.86	23.00	0.89	
MAX	1.00	2.30	2.90	6.20	32.70	30.68	30.75	25.20	23.06	22.75		

THERMAL MANAGEMENT

The S2080 requires thermal management. An example is provided on how to select the proper heat sink for specific system requirements (see page 18). The heat sink used in the example is available from:

Name: Aavid/Thermalloy
Address: 2021 W. Valley View Lane
City, State Zip: Dallas, TX 75234

Phone: (858) 271-0333
Fax: (949) 888-3321
Email: jaldridge@englishsales.com
Web: www.englishsales.com

Airflow requirement is determined by

$Pd = (T_{j\ max} - T_{a\ max}) / \theta_{ja}$, $\theta_{ja} = \theta_{jc} + \theta_{ca}$

$\theta_{sa\ (required)} = \theta_{ja} - \theta_{jc} - \theta_{cs}$

where $T_{j\ max}$ is the maximum junction temperature
$T_{a\ max}$ is the maximum ambient temperature
θ_{ja} is the thermal resistance from junction to ambient
θ_{jc} is the thermal resistance from junction to case
θ_{ca} is the thermal resistance from case to ambient (if a heat sink is used, this is θ_{sa} - sink to ambient)
θ_{cs} is the thermal resistance from case to sink.
θ_{sa} is the thermal resistance from sink to ambient.

Tables 10 and 11 show the max package power vs. airlfow (with and without heat sink), calculated using the equation above with $T_{j\ max}$ = 125 ˚C and $T_{a\ max}$ = 70 ˚C. In order to successfully use the S2080, the max package power must exceed the specified max power dissipation of the device, which is determined by the output swing setting (see Tables 13 and 14). The dimensions of the heat sink are provided in Table 11.

Table 10. S2080 Power Dissipation vs. Air Flow, No Heat Sink

Max Package Power (W)	Air Flow (LFPM)	θ_{ja} (ºC/W)	θ_{jc} (ºC/W)
4.23	0	13	0.88
4.70	100	11.7	0.88
5.24	200	10.5	0.88
5.79	300	9.5	0.88
6.32	400	8.7	0.88
7.14	600	7.7	0.88

A sample of system requirements given:
Possibly will use output settings # 2, 3, 5, or 6: max power dissipations are 10.8, 11.6, 12.38, or 13.88 W respectively.

Ambient temperature: 70 ˚C

Dimensions of heat sink: less than 45 mm x 45 mm

Heat sink height: less than 0.75 inches

Eg. for output setting # 2

θ_{jc} = 0.88 ˚C/W
θ_{cs} = 0.54 ˚C/W (Ther-A-Grip 1070; assumption)
θ_{ja} (required) = $(T_{j\ max} - T_{a\ max})/Pd = \theta_{ja}$
125 - 70/10.8 = 5.09 ˚C/W
θ_{sa} (required) = $\theta_{ja} - \theta_{jc} - \theta_{cs}$
5.09 - 0.88 - 0.54 = 3.67 ˚C/W

Table 11 provides the θ_{sa} for different airflows for the Aavid/Thermalloy 2332B Heat sink.

Table 11. S2080 Power Dissipation vs. Air Flow, # 2332B Heat Sink (41.28 mm x 43.18 mm x 16.51 mm)

Max Device Power (W)	Air Flow (LFPM)	θ_{ja} (required)	θ_{sa} (required)	θ_{sa} (# 2332B) (ºC/W)
10.8 (Output Setting #2)	200	5.09	3.67	3.1
11.6 (Output Setting #3)	200	4.74	3.32	3.1
12.38 (Output Setting #5)	300	4.44	3.02	2.5
13.88 (Output Setting #6)	400	3.96	2.54	2.0

Table 12. Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
Storage Temperature	-65		150	˚C
Voltage on any Power Pin w.r.t. GND	-0.5		4	V
Voltage on any LVTTL Input Pin	-0.5		V_{CC} +0.5	V
Voltage on any LVPECL Input Pin	0		V_{CC}	V
High Speed CML Output Source Current			30	mA

Electrostatic Discharge (ESD) Ratings

The S2080 is rated to the following ESD voltages based on the human body model:

1. All pins are rated at 100 V.

Table 13. Recommended Operating Conditions (+3.3 V supply)

Parameter	Min	Typ	Max	Units
Ambient Temperature Under Bias	0		70	˚C
Junction Temperature Under Bias			125	˚C
Voltage on any Power Pin w.r.t. GND	3.13	3.3	3.47	V
Voltage on any LVTTL Input Pin	0		3.47	V
Voltage on any LVPECL Input Pin	1.9		V_{CC} -0.3	V
I_{CC} Supply Current (with output setting #1)		2.31	2.88	A
I_{CC} Supply Current (with output setting #2)		2.50	3.11	A
I_{CC} Supply Current (with output setting #3)		2.69	3.34	A
I_{CC} Supply Current (with output setting #4)		2.88	3.57	A
I_{CC} Supply Current (with output setting #5)		3.06	3.79	A
I_{CC} Supply Current (with output setting #6)		3.24	4.0	A
Power Dissipation (with output setting #1)		7.61	10.0	W
Power Dissipation (with output setting #2)		8.25	10.8	W
Power Dissipation (with output setting #3)		8.88	11.6	W
Power Dissipation (with output setting #4)		9.49	12.38	W
Power Dissipation (with output setting #5)		10.10	13.16	W
Power Dissipation (with output setting #6)		10.69	13.88	W

Table 14. Recommended Operating Conditions (+2.7 V supply)

Parameter	Min	Typ	Max	Units
Ambient Temperature Under Bias	0		70	˚C
Junction Temperature Under Bias			125	˚C
Voltage on any Power Pin w.r.t. GND	2.565	2.7	2.835	V
Voltage on any LVTTL Input Pin	0		V_{CC}	V
Voltage on any LVPECL Input Pin	1.9		V_{CC} -0.3	V
I_{CC} Supply Current (with output setting #1)		1.91	2.4	A
I_{CC} Supply Current (with output setting #2)		2.08	2.61	A
I_{CC} Supply Current (with output setting #3)		2.26	2.82	A
I_{CC} Supply Current (with output setting #4)		2.43	3.02	A
I_{CC} Supply Current (with output setting #5)		2.59	3.22	A
I_{CC} Supply Current (with output setting #6)		2.74	3.41	A
Power Dissipation (with output setting #1)		5.15	6.8	W
Power Dissipation (with output setting #2)		5.63	7.4	W
Power Dissipation (with output setting #3)		6.10	8.0	W
Power Dissipation (with output setting #4)		6.55	8.57	W
Power Dissipation (with output setting #5)		7.00	9.13	W
Power Dissipation (with output setting #6)		7.41	9.67	W

Table 15. Input/Output Characteristics (+3.3 V supply)

Parameter	Description	Min	Typ	Max	Units	Conditions
LVTTL Inputs						
V_{IH}	Input High Voltage	2		3.47	V	Vcc = Max
V_{IL}	Input Low Voltage	0		0.8	V	Vcc = Max
I_{IH}	Input High Current			50	µA	VIN = 2.4 V
I_{IL}	Input Low Current	-500			µA	VIN = 0.5 V
ΔV_{HYST}	Magnitude of hysteresis		120		mV	
LVPECL Inputs						
V_{ID}	Differential Input Voltage Swing	200		1600	mV	See Figure 8.
V_{ID}	Differential Input Voltage Swing	1601		2200	mV	See Figure 8. Must be AC coupled input. Junction temperature must not exceed 100˚ C.
V_I	Input Voltage Range	1.9		V_{CC} -0.3	V	See Figure 15. Only used when DC coupling to the inputs.
$V_{INOFFSET}$	Inherent DC offset voltage between the P and N of each input		10		mV	
I_{IH}	Input High Current			10	mA	V_{ID} = Max
I_{IL}	Input Low Current	-10			mA	V_{ID} = Max
R_{DIFF}	Differential Input Resistance	80	100	120	Ω	
CML Outputs						
V_{OH}	CML Output High Voltage (with output setting #1)	V_{CC} -0.22		V_{CC} -0.013	V	100 Ω line-to-line. (Without AC coupling caps.)
V_{OL}	CML Output Low Voltage (with output setting #1)	V_{CC} -0.60		V_{CC} -0.037	V	100 Ω line-to-line. (Without AC coupling caps.)
V_{OH}	CML Output High Voltage (with output setting #2)	V_{CC} -0.30		V_{CC} -0.051	V	100 Ω line-to-line. (Without AC coupling caps.)
V_{OL}	CML Output Low Voltage (with output setting #2)	V_{CC} -0.82		V_{CC} -0.13	V	100 Ω line-to-line. (Without AC coupling caps.)
V_{OH}	CML Output High Voltage (with output setting #3)	V_{CC} -0.37		V_{CC} -0.083	V	100 Ω line-to-line. (Without AC coupling caps.)
V_{OL}	CML Output Low Voltage (with output setting #3)	V_{CC} -0.98		V_{CC} -0.24	V	100 Ω line-to-line. (Without AC coupling caps.)
V_{OH}	CML Output High Voltage (with output setting #4)	V_{CC} -0.44		V_{CC} -0.11	V	100 Ω line-to-line. (Without AC coupling caps.)

Table 15. Input/Output Characteristics (+3.3 V supply) (Continued)

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{OL}	CML Output Low Voltage (with output setting #4)	V_{CC} -1.175		V_{CC} -0.32	V	100 Ω line-to-line. (Without AC coupling caps.)
V_{OH}	CML Output High Voltage (with output setting #5)	V_{CC} -0.52		V_{CC} -0.13	V	100 Ω line-to-line. (Without AC coupling caps.)
V_{OL}	CML Output Low Voltage (with output setting #5)	V_{CC} -1.43		V_{CC} -0.34	V	100 Ω line-to-line. (Without AC coupling caps.)
V_{OH}	CML Output High Voltage (with output setting #6)	V_{CC} -0.58		V_{CC} -0.17	V	100 Ω line-to-line. (Without AC coupling caps.)
V_{OL}	CML Output Low Voltage (with output setting #6)	V_{CC} -1.62		V_{CC} -0.42	V	100 Ω line-to-line. (Without AC coupling caps.)
V_{OD}	CML Serial Output Differential Voltage Swing (output setting #1)	298	398	497	mV	100 Ω line-to-line. See Table 2 for output swing settings. See Figure 9. Peak-to-peak.
V_{OD}	CML Serial Output Differential Voltage Swing (output setting #2)	443	583	723	mV	100 Ω line-to-line. See Table 2 for output swing settings. See Figure 9. Peak-to-peak.
V_{OD}	CML Serial Output Differential Voltage Swing (output setting #3)	589	765	940	mV	100 Ω line-to-line. See Table 2 for output swing settings. See Figure 9. Peak-to-peak.
V_{OD}	CML Serial Output Differential Voltage Swing (output setting #4)	724	940	1156	mV	100 Ω line-to-line. See Table 2 for output swing settings. See Figure 9. Peak-to-peak.
V_{OD}	CML Serial Output Differential Voltage Swing (output setting #5)	857	1112	1368	mV	100 Ω line-to-line. See Table 2 for output swing settings. See Figure 9. Peak-to-peak.
V_{OD}	CML Serial Output Differential Voltage Swing (output setting #6)	1073	1278	1482	mV	100 Ω line-to-line. See Table 2 for output swing settings. See Figure 9. Peak-to-peak.
R_O	Output Impedance (Single Ended)	40	50	60	Ω	

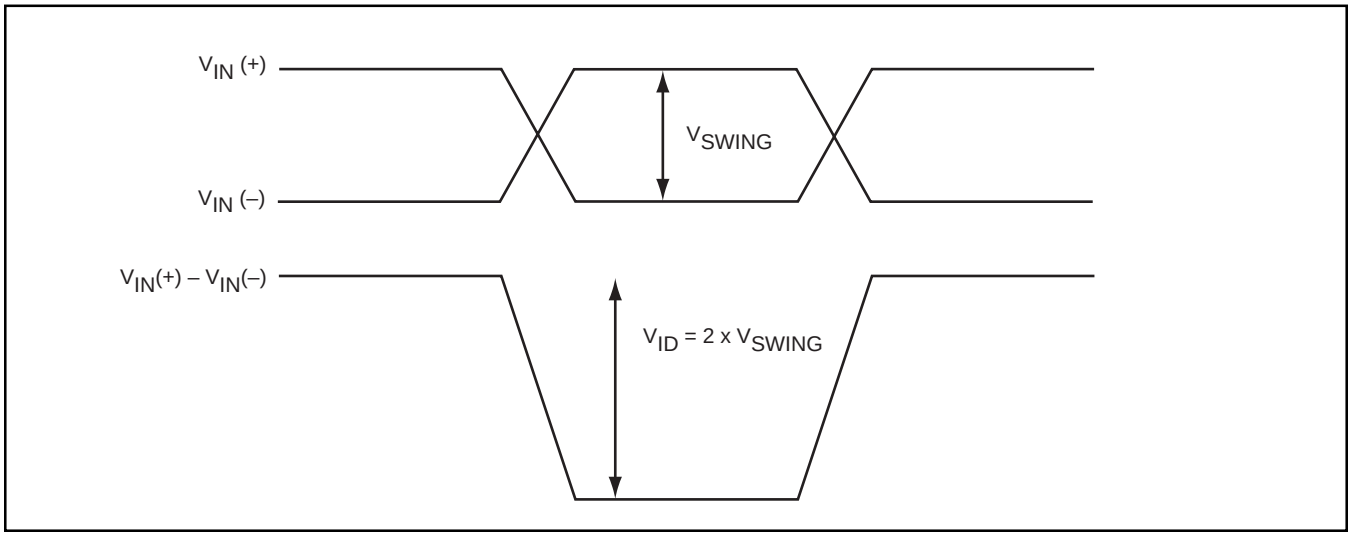
Table 16. Input/Output Characteristics (+2.7 V supply)

Parameter	Description	Min	Typ	Max	Units	Conditions
LVTTL Inputs						
V_{IH}	Input High Voltage	2		V_{CC}	V	Vcc = Max
V_{IL}	Input Low Voltage	0		0.8	V	Vcc = Max
I_{IH}	Input High Current			50	µA	VIN = 2.4 V
I_{IL}	Input Low Current	-500			µA	VIN = 0.5 V
ΔV_{HYST}	Magnitude of hysteresis		120		mV	
LVPECL Inputs						
V_{ID}	Differential Input Voltage Swing	200		1600	mV	See Figure 8.
V_{ID}	Differential Input Voltage Swing	1601		2200	mV	See Figure 8. Must be AC coupled input. Junction temperature must not exceed 100˚ C.
V_I	Input Voltage Range	1.9		V_{CC} -0.3	V	See Figure 15. Only used when DC coupling to the inputs.
$V_{INOFFSET}$	Inherent DC offset voltage between the P and N of each input		7		mV	
I_{IH}	Input High Current			10	mA	V_{ID} = Max
I_{IL}	Input Low Current	-10			mA	V_{ID} = Max
R_{DIFF}	Differential Input Resistance	80	100	120	Ω	
CML Outputs						
V_{OH}	CML Output High Voltage (with output setting #1)	V_{CC} -0.22		V_{CC} -0.013	V	100 Ω line-to-line. (Without AC coupling caps.)
V_{OL}	CML Output Low Voltage (with output setting #1)	V_{CC} -0.60		V_{CC} -0.037	V	100 Ω line-to-line. (Without AC coupling caps.)
V_{OH}	CML Output High Voltage (with output setting #2)	V_{CC} -0.30		V_{CC} -0.051	V	100 Ω line-to-line. (Without AC coupling caps.)
V_{OL}	CML Output Low Voltage (with output setting #2)	V_{CC} -0.82		V_{CC} -0.13	V	100 Ω line-to-line. (Without AC coupling caps.)
V_{OH}	CML Output High Voltage (with output setting #3)	V_{CC} -0.37		V_{CC} -0.083	V	100 Ω line-to-line. (Without AC coupling caps.)
V_{OL}	CML Output Low Voltage (with output setting #3)	V_{CC} -0.98		V_{CC} -0.24	V	100 Ω line-to-line. (Without AC coupling caps.)
V_{OH}	CML Output High Voltage (with output setting #4)	V_{CC} -0.44		V_{CC} -0.11	V	100 Ω line-to-line. (Without AC coupling caps.)

Table 16. Input/Output Characteristics (+2.7 V supply) (Continued)

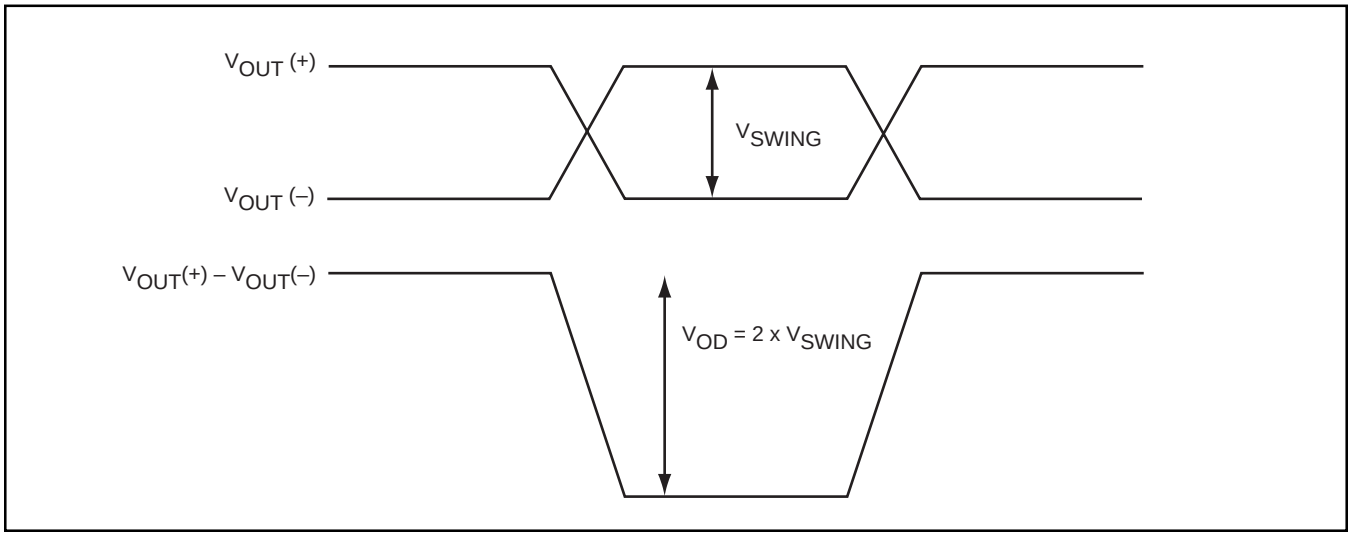
Parameter	Description	Min	Typ	Max	Units	Conditions
V_{OL}	CML Output Low Voltage (with output setting #4)	V_{CC} -1.175		V_{CC} -0.32	V	100 Ω line-to-line. (Without AC coupling caps.)
V_{OH}	CML Output Low Voltage (with output setting #5)	V_{CC} -0.52		V_{CC} -0.13	V	100 Ω line-to-line. See Table 3 for output swing settings. See Figure 9. Peak-to-peak.
V_{OL}	CML Output Low Voltage (with output setting #5)	V_{CC} -1.43		V_{CC} -0.34	V	100 Ω line-to-line. See Table 3 for output swing settings. See Figure 9. Peak-to-peak.
V_{OH}	CML Output Low Voltage (with output setting #6)	V_{CC} -0.58		V_{CC} -0.17	V	100 Ω line-to-line. See Table 3 for output swing settings. See Figure 9. Peak-to-peak.
V_{OL}	CML Output Low Voltage (with output setting #6)	V_{CC} -1.62		V_{CC} -0.42	V	100 Ω line-to-line. See Table 3 for output swing settings. See Figure 9. Peak-to-peak.
V_{OD}	CML Serial Output Differential Voltage Swing (output setting #1)	225	348	467	mV	100 Ω line-to-line. See Table 3 for output swing settings. See Figure 9. Peak-to-peak.
V_{OD}	CML Serial Output Differential Voltage Swing (output setting #2)	336	509	666	mV	100 Ω line-to-line. See Table 3 for output swing settings. See Figure 9. Peak-to-peak.
V_{OD}	CML Serial Output Differential Voltage Swing (output setting #3)	461	669	856	mV	100 Ω line-to-line. See Table 3 for output swing settings. See Figure 9. Peak-to-peak.
V_{OD}	CML Serial Output Differential Voltage Swing (output setting #4)	563	818	1045	mV	100 Ω line-to-line. See Table 3 for output swing settings. See Figure 9. Peak-to-peak.
V_{OD}	CML Serial Output Differential Voltage Swing (output setting #5)	661	962	1228	mV	100 Ω line-to-line. See Table 3 for output swing settings. See Figure 9. Peak-to-peak.
V_{OD}	CML Serial Output Differential Voltage Swing (output setting #6)	752	1095	1396	mV	100 Ω line-to-line. See Table 3 for output swing settings. See Figure 9. Peak-to-peak.
R_O	Output Impedance (Single Ended)	40	50	60	Ω	

Figure 8. Differential Input Voltage



Note: $V_{IN}(+) – V_{IN}(-)$ is the algebraic difference of the input signals.

Figure 9. Differential Output Voltage



Note: $V_{OUT}(+) – V_{OUT}(-)$ is the algebraic difference of the input signals.

Figure 10. LVTTL Input Rise and Fall Time

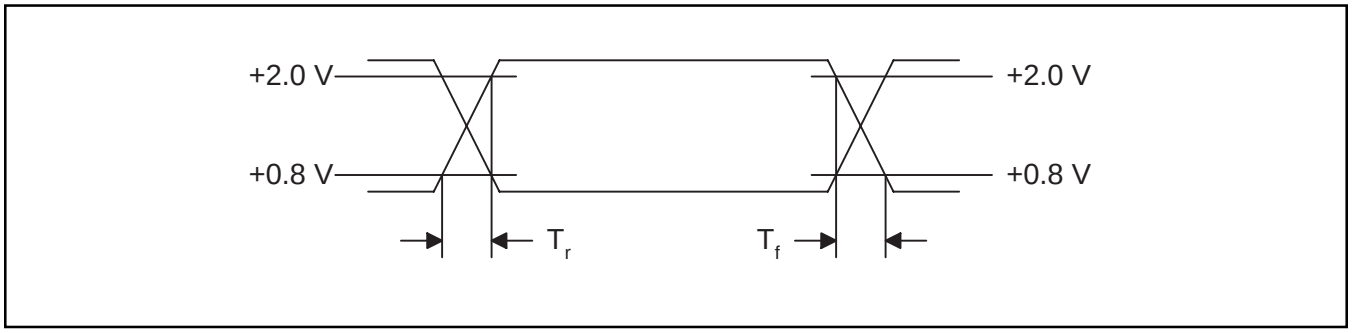


Figure 11. Differential CML Output to +3.3 V or +2.7 V PECL Input AC Coupled Termination

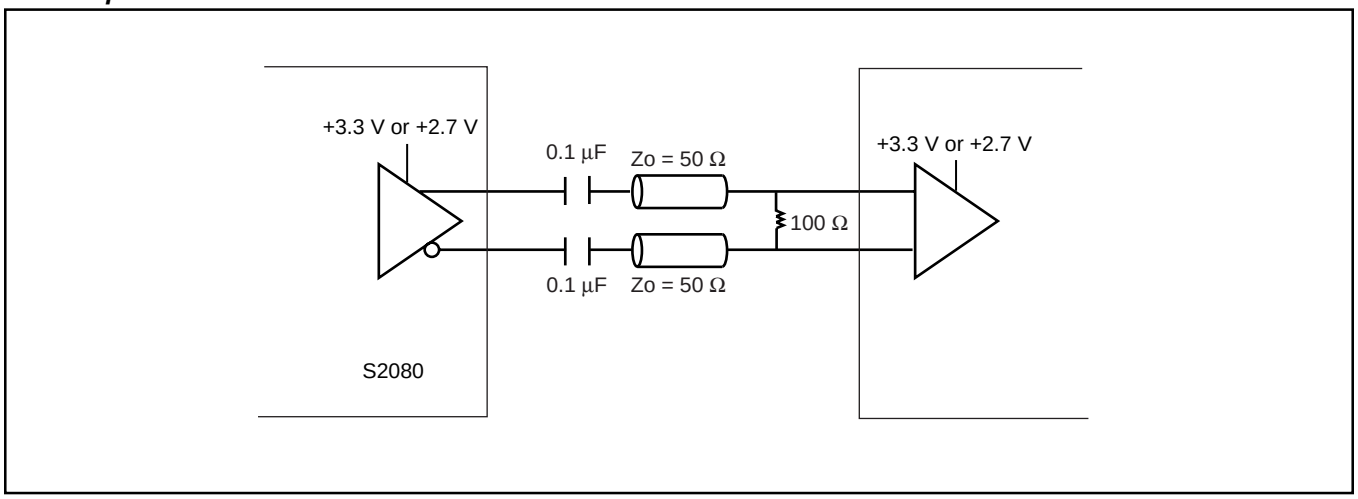


Figure 12. S2080 Output DC Coupled to S2080 Input

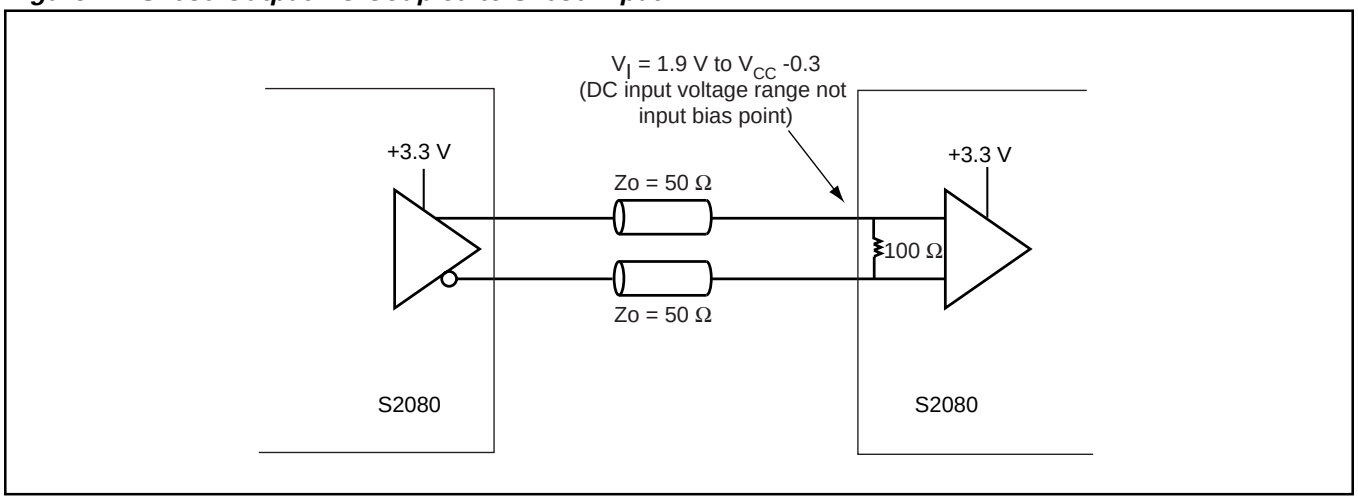


Figure 13. S2090 Output DC Coupled to S2080 Input

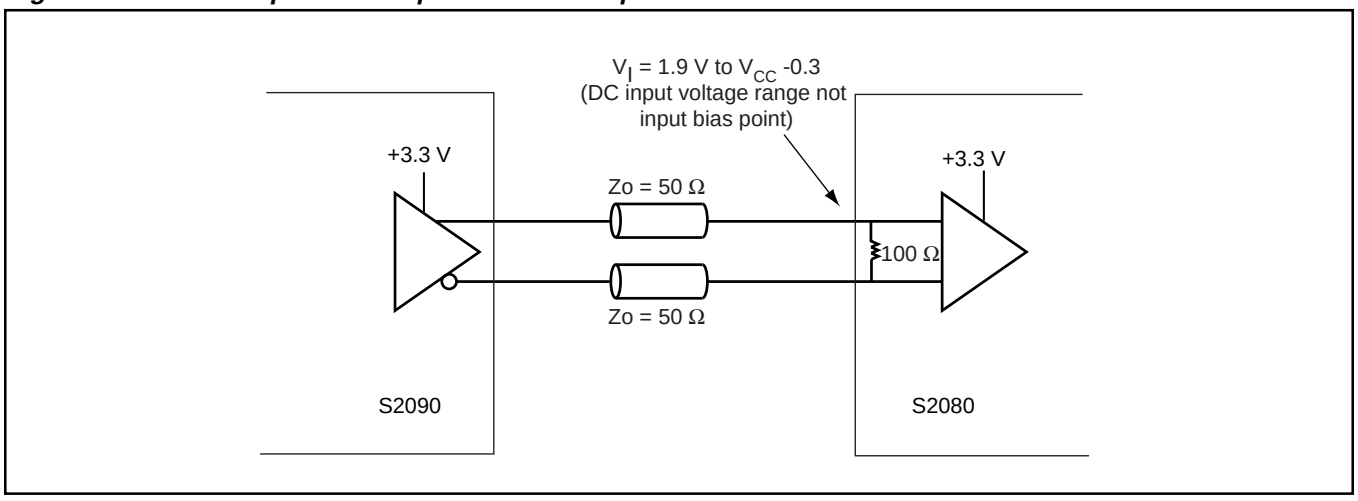


Figure 14. S2080 Output DC Coupled to S2090 Input

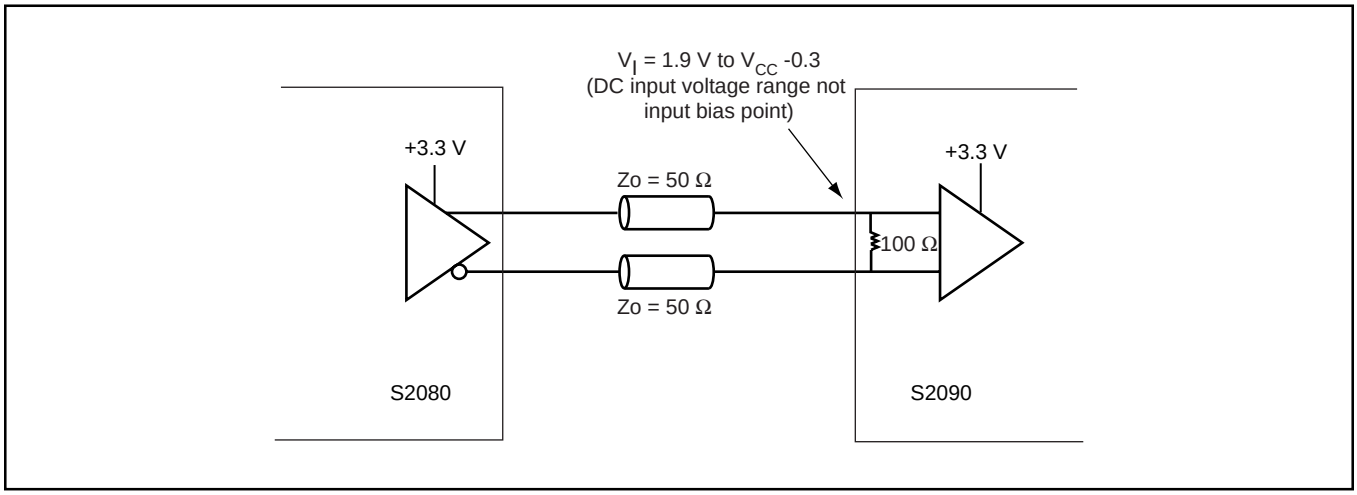
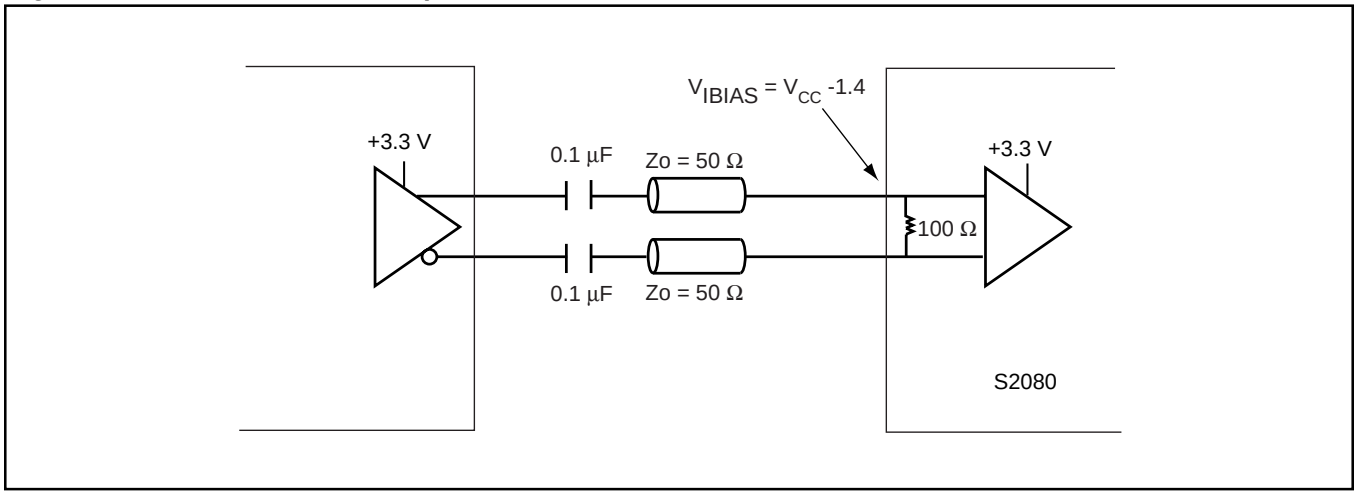


Figure 15. Differential LVPECL Inputs



Ordering Information

PREFIX	DEVICE	PACKAGE
S – Integrated Circuit	2080	CB – 474 CBGA

XX Prefix XXXX Device XX Package

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