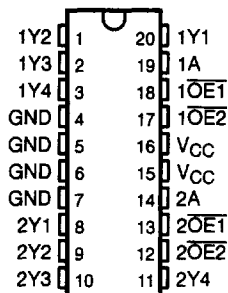


# CDC208, CDC208-7 DUAL 1-LINE TO 4-LINE CLOCK DRIVERS WITH 3-STATE OUTPUTS

SCAS109C – APRIL 1990 – REVISED MARCH 1994

- CDC208 Replaces 74ACT11208
- CDC208-7 Replaces 74ACT11208-7
- Low-Skew Propagation Delay Specifications for Clock-Driver Applications
- TTL-Compatible Inputs and CMOS-Compatible Outputs
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin  $V_{CC}$  and GND Pin Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- $\mu$ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages and Standard Plastic 300-mil DIPs (N)

DB, DW, OR N PACKAGE  
(TOP VIEW)



## description

The CDC208/208-7 contains dual clock-driver circuits that fanout one input signal to four outputs with minimum skew for clock distribution (see Figure 2). The device also offers two output-enable ( $\overline{OE1}$  and  $\overline{OE2}$ ) inputs for each circuit that can force the outputs to be disabled to a high-impedance state or to a high- or low-logic level independent of the signal on the respective A input.

Skew parameters are specified for a reduced temperature and voltage range common to many applications.

The CDC208/208-7 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

EPIC is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA Information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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**WITH 3-STATE OUTPUTS**

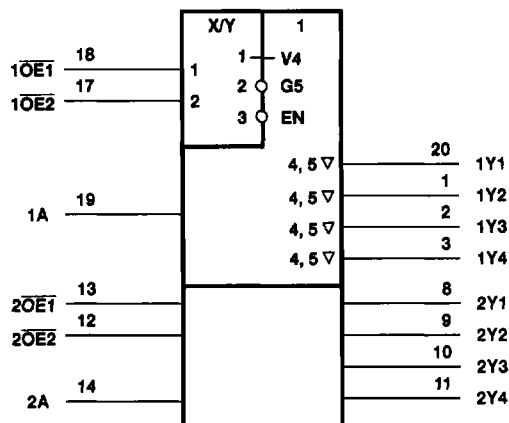
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FUNCTION TABLES

INPUTS			OUTPUTS			
$\overline{1OE1}$	$\overline{1OE2}$	1A	1Y1	1Y2	1Y3	1Y4
L	L	L	L	L	L	L
L	L	H	H	H	H	H
L	H	X	L	L	L	L
H	L	X	H	H	H	H
H	H	X	Z	Z	Z	Z

INPUTS			OUTPUTS			
$\overline{2OE1}$	$\overline{2OE2}$	2A	2Y1	2Y2	2Y3	2Y4
L	L	L	L	L	L	L
L	L	H	H	H	H	H
L	H	X	L	L	L	L
H	L	X	H	H	H	H
H	H	X	Z	Z	Z	Z

logic symbol†

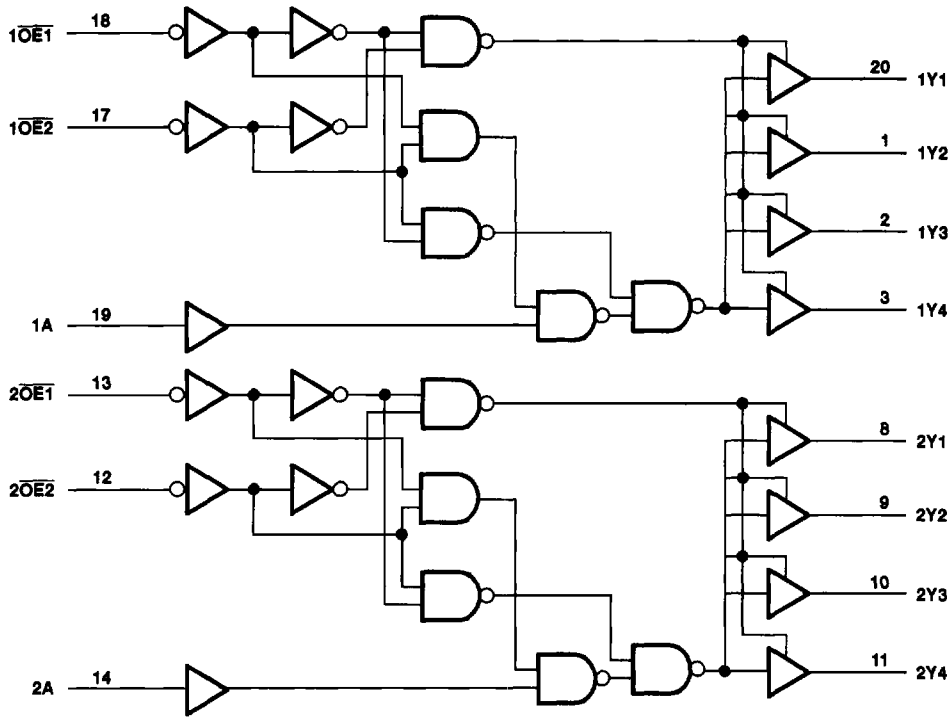


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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**logic diagram (positive logic)**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) .....	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	$\pm 50$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 200$ mA
Storage temperature range .....	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

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## recommended operating conditions

	MIN	NOM	MAX	UNIT
V <sub>CC</sub> Supply voltage	4.5	5	5.5	V
V <sub>IH</sub> High-level input voltage	2			V
V <sub>IL</sub> Low-level input voltage			0.8	V
V <sub>I</sub> Input voltage	0	V <sub>CC</sub>		V
I <sub>OH</sub> High-level output current			-24	mA
I <sub>OL</sub> Low-level output current			24	mA
Δt/Δv Input transition rise or fall rate	0		10	ns/V
f <sub>clock</sub> Input clock frequency			60	MHz
T <sub>A</sub> Operating free-air temperature	-40		85	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			CDC208		CDC208-7		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	4.5 V	4.4		4.4	4.4			V	
		5.5 V	5.4		5.4	5.4				
	I <sub>OH</sub> = -24 mA	4.5 V	3.94		3.8	3.8				
		5.5 V	4.94		4.8	4.8				
	I <sub>OH</sub> = -50 mA†	5.5 V								
I <sub>OH</sub> = -75 mA†	5.5 V			3.85	3.85					
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	4.5 V		0.1	0.1	0.1			V	
		5.5 V		0.1	0.1	0.1				
	I <sub>OL</sub> = 24 mA	4.5 V		0.36	0.44	0.44				
		5.5 V		0.36	0.44	0.44				
	I <sub>OL</sub> = 50 mA†	5.5 V								
I <sub>OL</sub> = 75 mA†	5.5 V			1.65	1.65					
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V		±0.1	±1	±1		μA		
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V		±0.5	±5	±5		μA		
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V		8	80	80		μA		
ΔI <sub>CC</sub> ‡	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V		0.9	1	1		mA		
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		4				pF		
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5 V		10				pF		

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.

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**switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			CDC208		CDC208-7		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	1A and 2A	Any Y	5.3	8.5	10.9	5.3	11.7	5.3	11.7	ns
$t_{PHL}$			3.6	7.7	11	3.6	11.5	3.6	11.5	
$t_{PLH}$	$\overline{1OE1}$ , $\overline{1OE2}$ , and $\overline{2OE1}$ , $\overline{2OE2}$	Any Y	4.7	8.5	11.7	4.7	12.8	4.7	12.8	ns
$t_{PHL}$			4.4	8.4	11.3	4.4	12.4	4.4	12.4	
$t_{PZH}$	$\overline{1OE2}$ or $\overline{2OE2}$	Any Y	4.4	8.1	11.3	4.4	12.4	4.4	12.4	ns
$t_{PZL}$	$\overline{1OE1}$ or $\overline{2OE1}$		5	9.6	13.3	5	14.9	5	14.9	
$t_{PHZ}$	$\overline{1OE2}$ or $\overline{2OE2}$	Any Y	4.2	7.4	9.3	4.2	10.2	4.2	10.2	ns
$t_{PLZ}$	$\overline{1OE1}$ or $\overline{2OE1}$		5.4	7.5	9.2	5.4	9.9	5.4	9.9	

**switching characteristics,  $V_{CC} = 5\text{ V} \pm 0.25\text{ V}$ ,  $T_A = 25^\circ\text{C}$  to  $70^\circ\text{C}$  (see Note 2 and Figures 1 and 2)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CDC208		CDC208-7		UNIT
			MIN	MAX	MIN	MAX	
$t_{PLH}$	1A and 2A	Any Y	7.6	10.2	7.6	10.2	ns
$t_{PHL}$			6.6	9.8	6.6	9.8	
$t_{sk(o)}$	1A and 2A	Any Y	1		0.7		ns

NOTE 2: All specifications are valid only for all outputs switching simultaneously and in phase.

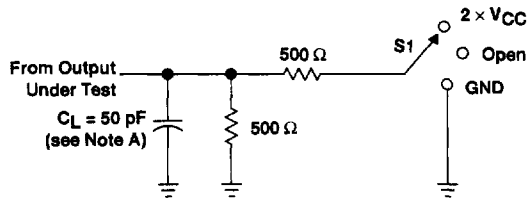
**operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$**

PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance per bank	Outputs enabled	96	pF
		Outputs disabled	12	

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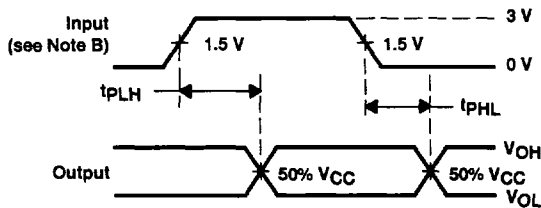
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## PARAMETER MEASUREMENT INFORMATION

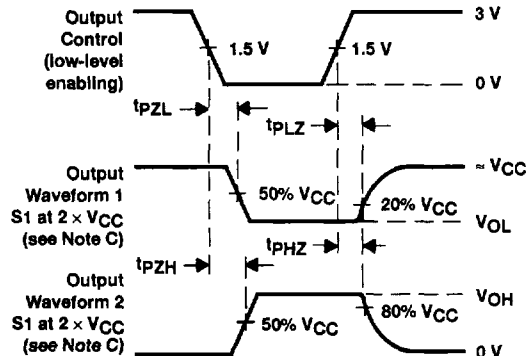


(see Note A) LOAD CIRCUIT FOR OUTPUTS

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

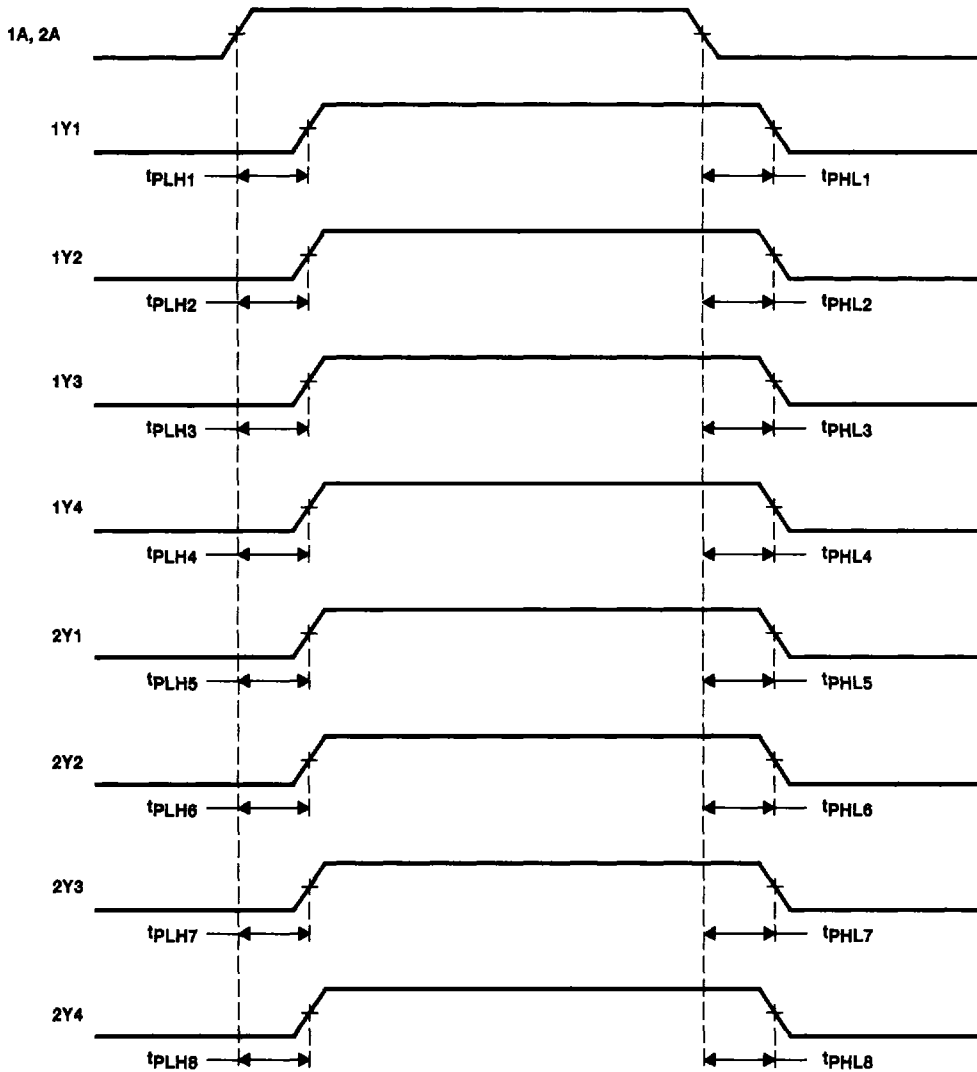
- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 3$  ns,  $t_f \leq 3$  ns. For testing pulse duration:  $t_r = t_f = 1$  to 3 ns. Pulse polarity can be either high-to-low-to-high or low-to-high-to-low.  
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Figure 1. Load Circuit and Voltage Waveforms

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**PARAMETER MEASUREMENT INFORMATION**



NOTE D: Output skew,  $t_{sk(o)}$ , is calculated as the greater of:

- The difference between the fastest and slowest of  $t_{PLHn}$  ( $n = 1, 2, \dots, 8$ )
- The difference between the fastest and slowest of  $t_{PHLn}$  ( $n = 1, 2, \dots, 8$ )

**Figure 2. Waveforms for Calculation of  $t_{sk(o)}$**