

To our customers,

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## Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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J-FET INPUT LOW-OFFSET DUAL OPERATIONAL AMPLIFIER

The  $\mu$ PC4092 dual operational amplifier offers high input impedance, low offset voltage, high slew rate, and stable AC operating characteristics. NEC's unique high-speed PNP transistor ( $f_T = 300$  MHz) in the output stage solves the oscillation problem of current sinking with a large capacitive load. Zener-zap resistor trimming in the input stage produces excellent offset voltage and temperature drift characteristics.

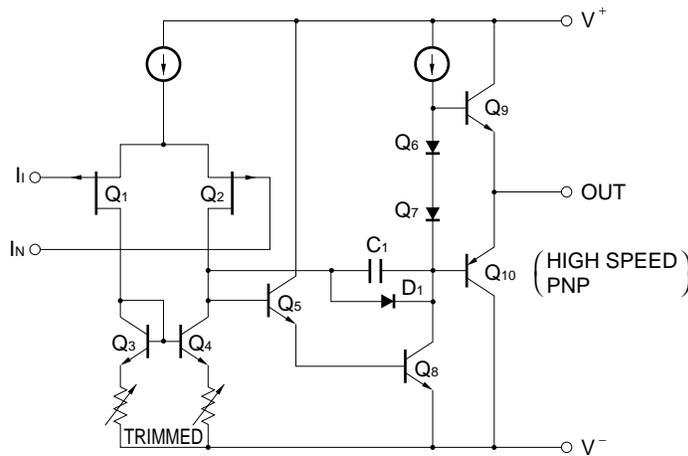
FEATURES

- Stable operation with 10000 pF capacitive load
- Low input offset voltage  
 $\pm 3$  mV (MAX.)  
 $\pm 7$   $\mu$ V/ $^{\circ}$ C (TYP.) temperature drift
- Very low input bias and offset currents
- Low noise :  $e_n = 19$  nV/ $\sqrt{\text{Hz}}$  (TYP.)
- Output short circuit protection
- High input impedance ... J-FET Input Stage
- Internal frequency compensation
- High slew rate: 15 V/ $\mu$ s (TYP.)

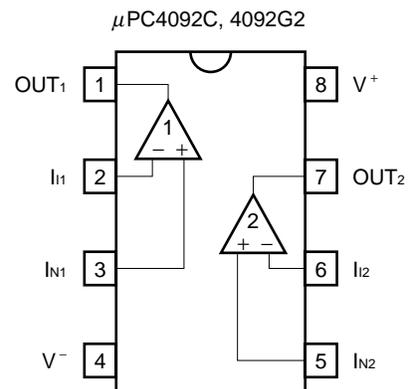
★ ORDERING INFORMATION

Part Number	Package
$\mu$ PC4092C	8-pin plastic DIP (7.62 mm (300))
$\mu$ PC4092G2	8-pin plastic SOP (5.72 mm (225))

EQUIVALENT CIRCUIT (1/2 Circuit)



PIN CONFIGURATION (Top View)



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**ABSOLUTE MAXIMUM RATINGS ( $T_A = 25\text{ }^\circ\text{C}$ )**

Parameter		Symbol	Ratings	Unit
Voltage between $V^+$ and $V^-$ <sup>Note 1</sup>		$V^+ - V^-$	-0.3 to +36	V
Differential Input Voltage		$V_{ID}$	$\pm 30$	V
Input Voltage <sup>Note 2</sup>		$V_I$	$V^- - 0.3$ to $V^+ + 0.3$	V
Output Voltage <sup>Note 3</sup>		$V_O$	$V^- - 0.3$ to $V^+ + 0.3$	V
Power Dissipation	C Package <sup>Note 4</sup>	$P_T$	350	mW
	G2 Package <sup>Note 5</sup>		440	mW
Output Short Circuit Duration <sup>Note 6</sup>			Indefinite	sec
Operating Ambient Temperature		$T_A$	-20 to +80	$^\circ\text{C}$
Storage Temperature		$T_{stg}$	-55 to +125	$^\circ\text{C}$

**Notes 1.** Reverse connection of supply voltage can cause destruction.

2. The input voltage should be allowed to input without damage or destruction. Even during the transition period of supply voltage, power on/off etc., this specification should be kept. The normal operation will establish when the both inputs are within the Common Mode Input Voltage Range of electrical characteristics.
3. This specification is the voltage which should be allowed to supply to the output terminal from external without damage or destructive. Even during the transition period of supply voltage, power on/off etc., this specification should be kept. The output voltage of normal operation will be the Output Voltage Swing of electrical characteristics.
4. Thermal derating factor is  $-5.0\text{ mV}/^\circ\text{C}$  when operating ambient temperature is higher than  $55\text{ }^\circ\text{C}$ .
5. Thermal derating factor is  $-4.4\text{ mV}/^\circ\text{C}$  when operating ambient temperature is higher than  $25\text{ }^\circ\text{C}$ .
6. Pay careful attention to the total power dissipation not to exceed the absolute maximum ratings, Note 4 and Note 5.

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply Voltage	$V^\pm$	$\pm 5$		$\pm 16$	V
Output Current	$I_o$			$\pm 10$	mA
Capacitive Load ( $A_v = +1$ , $R_i = 0\ \Omega$ )	$C_L$			10000	pF

**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, V<sup>±</sup> = ±15 V)**

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Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input Offset Voltage	V <sub>IO</sub>	R <sub>s</sub> ≤ 50 Ω		±1	±3	mV
Input Offset Current <sup>Note 7</sup>	I <sub>IO</sub>			±25	±100	pA
Input Bias Current <sup>Note 7</sup>	I <sub>B</sub>			50	200	pA
Large Signal Voltage Gain	A <sub>v</sub>	R <sub>L</sub> ≥ 2 kΩ, V <sub>o</sub> = ±10 V	25000	200000		
Supply Current <sup>Note 8</sup>	I <sub>CC</sub>	I <sub>o</sub> = 0 A		5	6.8	mA
Common Mode Rejection Ratio	CMR		70	100		dB
Supply Voltage Rejection Ratio	SVR		70	100		dB
Output Voltage Swing	V <sub>om</sub>	R <sub>L</sub> ≥ 10 kΩ	±12	+14.0 -13.3		V
		R <sub>L</sub> ≥ 2 kΩ	±10	+13.5 -12.8		V
Common Model Input Voltage Range	V <sub>ICM</sub>		±11	+14 -12		V
Slew Rate	SR	A <sub>v</sub> = 1		15		V/μs
Unity Gain Frequency	f <sub>unity</sub>			4		MHz
Input Equivalent Noise Voltage Density	e <sub>n</sub>	R <sub>s</sub> = 100 Ω, f = 1 kHz		19		nV/√Hz
Channel Separation				120		dB
Input Offset Voltage	V <sub>IO</sub>	R <sub>s</sub> ≤ 50 Ω, T <sub>A</sub> = -20 to +70 °C			±5	mV
Average V <sub>IO</sub> Temperature Drift	ΔV <sub>IO</sub> /ΔT	T <sub>A</sub> = -20 to +70 °C		±7		μV/°C
Input Offset Current <sup>Note 7</sup>	I <sub>IO</sub>	T <sub>A</sub> = -20 to +70 °C			±2	nA
Input Bias Current <sup>Note 7</sup>	I <sub>B</sub>	T <sub>A</sub> = -20 to +70 °C			7	nA

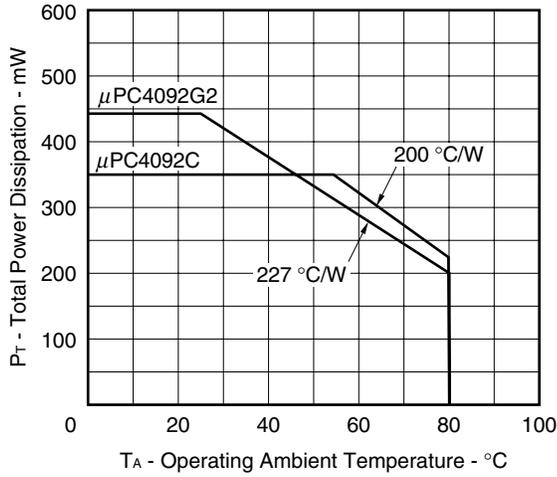
**Notes 7.** Input bias currents flow into IC. Because each currents are gate leak current of P-channel J-FET on input stage. And that are temperature sensitive. Short time measuring method is recommendable to maintain the junction temperature close to the operating ambient temperature.

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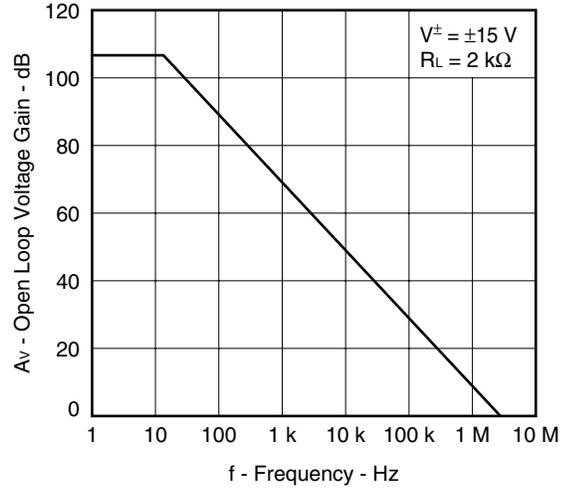
**8.** This current flows irrespective of the existence of use.

TYPICAL PERFORMANCE CHARACTERISTICS ( $T_A = 25\text{ }^\circ\text{C}$ , TYP.)

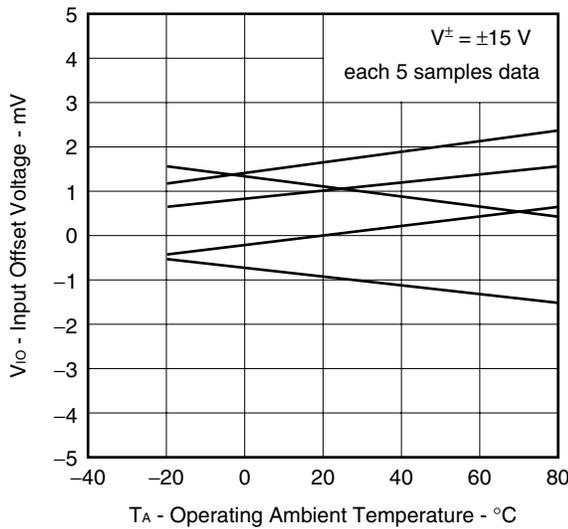
POWER DISSIPATION



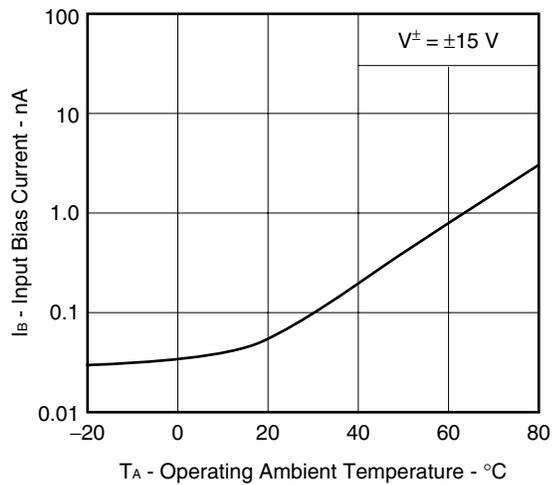
OPEN LOOP FREQUENCY RESPONSE



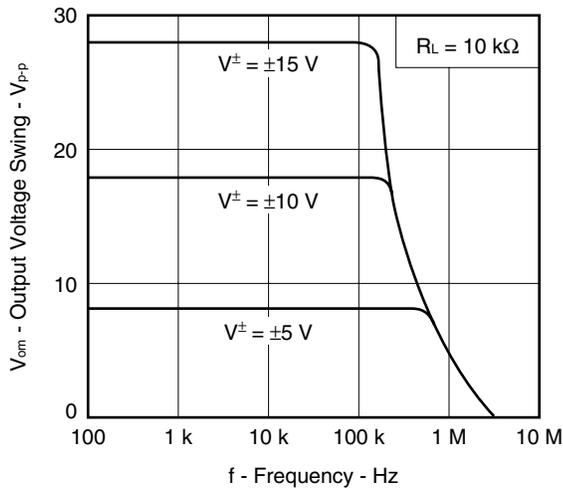
★ INPUT OFFSET VOLTAGE



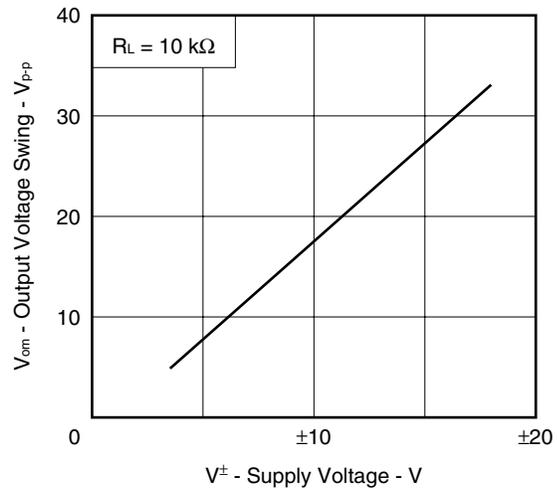
INPUT BIAS CURRENT

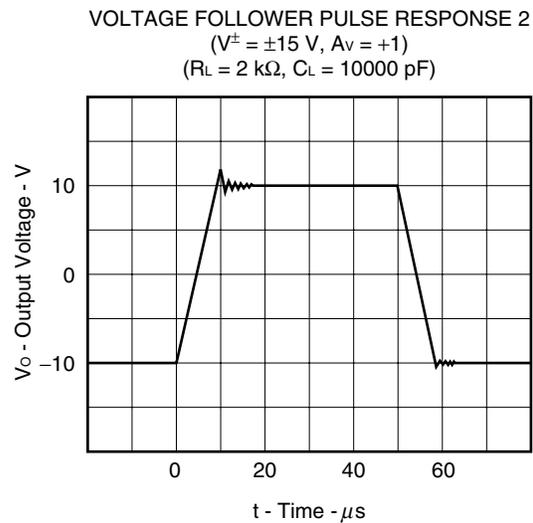
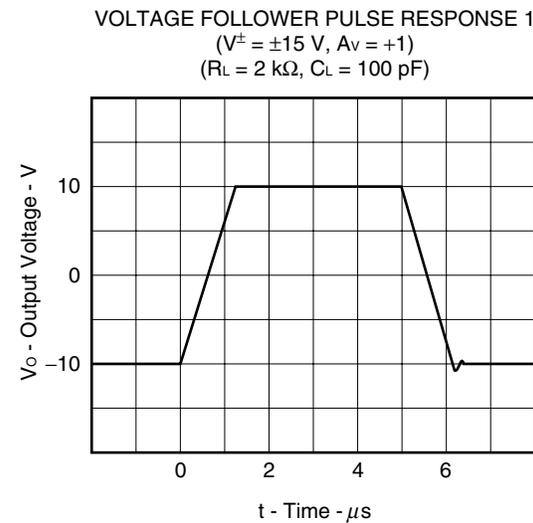
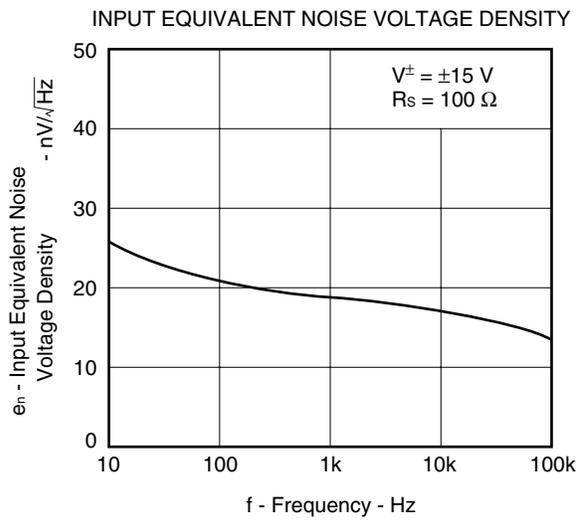
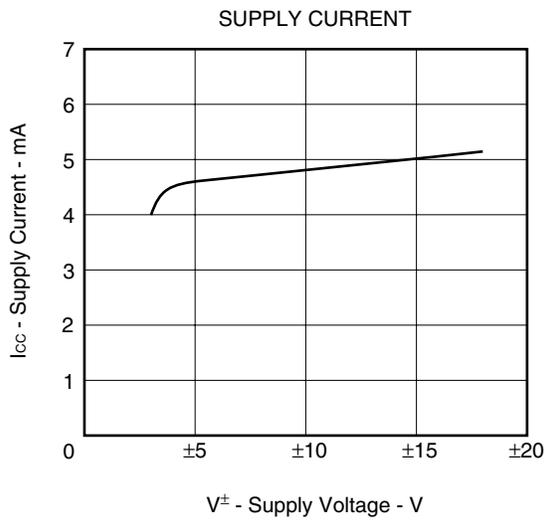
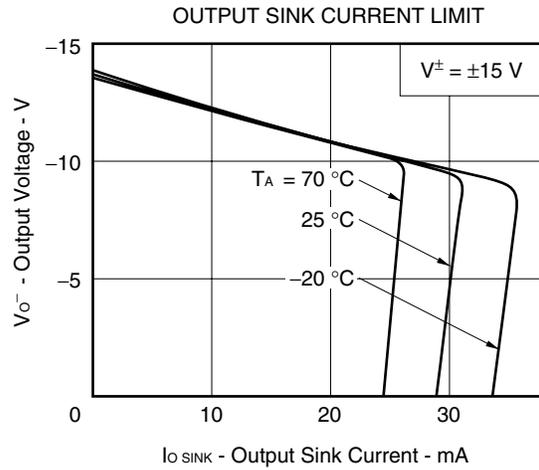
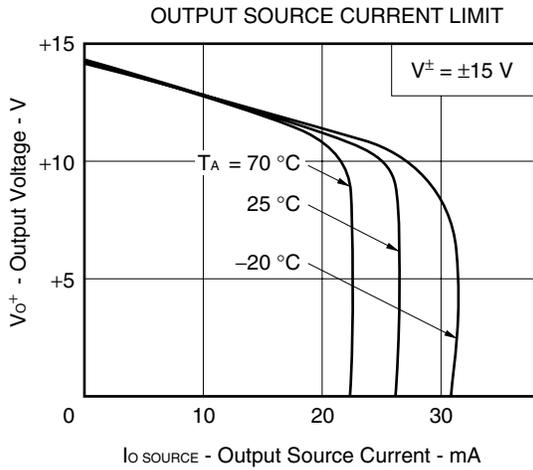


LARGE SIGNAL FREQUENCY RESPONSE



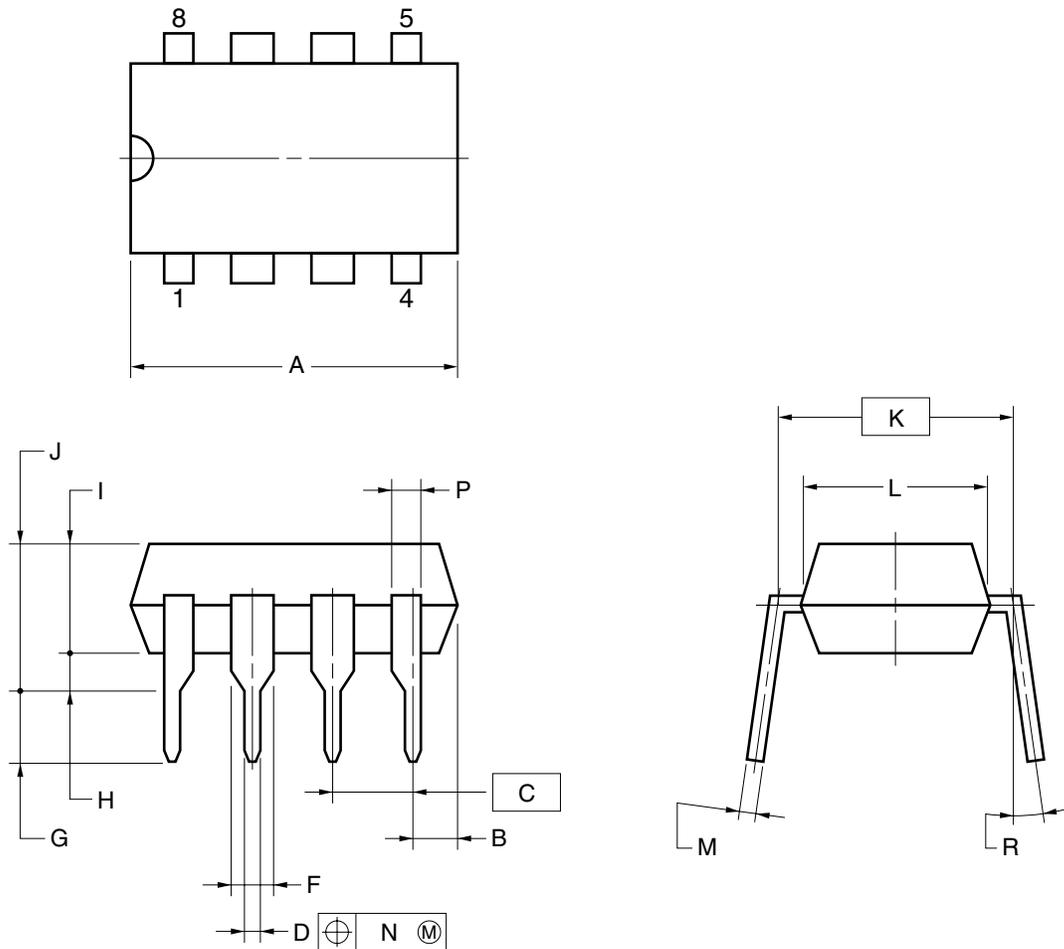
OUTPUT VOLTAGE SWING





★ PACKAGE DRAWINGS

8-PIN PLASTIC DIP (7.62mm(300))



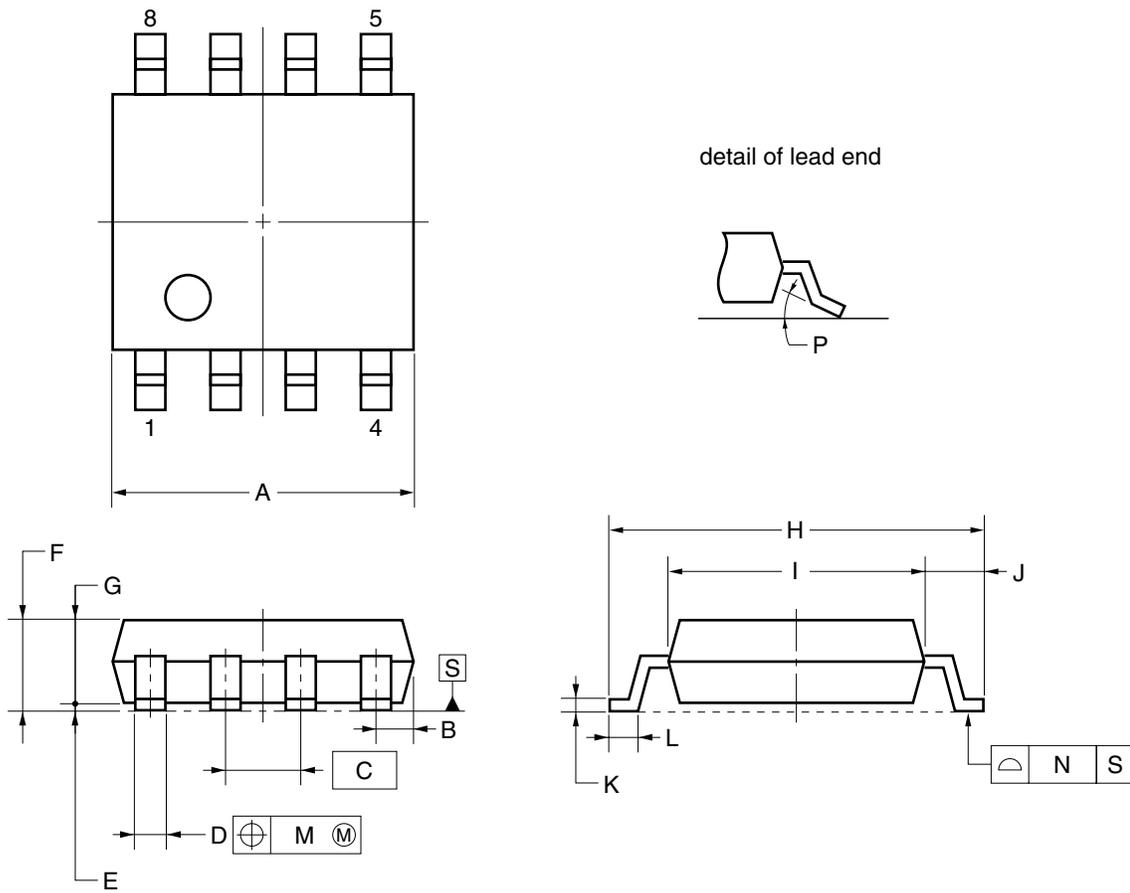
NOTES

1. Each lead centerline is located within 0.25 mm of its true position (T.P.) at maximum material condition.
2. Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS
A	10.16 MAX.
B	1.27 MAX.
C	2.54 (T.P.)
D	0.50±0.10
F	1.4 MIN.
G	3.2±0.3
H	0.51 MIN.
I	4.31 MAX.
J	5.08 MAX.
K	7.62 (T.P.)
L	6.4
M	0.25 <sup>+0.10</sup> <sub>-0.05</sub>
N	0.25
P	0.9 MIN.
R	0-15°

P8C-100-300B,C-2

8-PIN PLASTIC SOP (5.72 mm (225))



**NOTE**

Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	5.2 <sup>+0.17</sup> / <sub>-0.20</sub>
B	0.78 MAX.
C	1.27 (T.P.)
D	0.42 <sup>+0.08</sup> / <sub>-0.07</sub>
E	0.1±0.1
F	1.59±0.21
G	1.49
H	6.5±0.3
I	4.4±0.15
J	1.1±0.2
K	0.17 <sup>+0.08</sup> / <sub>-0.07</sub>
L	0.6±0.2
M	0.12
N	0.10
P	3° <sup>+7°</sup> / <sub>-3°</sub>

S8GM-50-225B-6

★ RECOMMENDED SOLDERING CONDITIONS

The μPC4092 should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (<http://www.necel.com/pkg/en/mount/index.html>)

Type of Surface Mount Device

μPC4092G2: 8-pin plastic SOP (5.72 mm (225))

Process	Conditions	Symbol
Infrared Ray Reflow	Peak temperature: 230 °C or below (Package surface temperature), Reflow time: 30 seconds or less (at 210 °C or higher), Maximum number of reflow processes: 1 time.	IR30-00-1
Vapor Phase Soldering	Peak temperature: 215 °C or below (Package surface temperature), Reflow time: 40 seconds or less (at 200 °C or higher), Maximum number of reflow processes: 1 time.	VP15-00-1
Wave Soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or less, Maximum number of flow processes: 1 time, Pre-heating temperature: 120 °C or below (Package surface temperature).	WS60-00-1
Partial Heating Method	Pin temperature: 300 °C or below, Heat time: 3 seconds or less (Per each side of the device).	—

**Caution** Apply only one kind of soldering condition to a device, except for "partial heating method", or the device will be damaged by heat stress.

Type of Through-hole Device

μPC4092C: 8-pin plastic DIP (7.62 mm (300))

Process	Conditions
Wave Soldering (only to leads)	Solder temperature: 260 °C or below, Flow time: 10 seconds or less.
Partial Heating Method	Pin temperature: 300 °C or below, Heat time: 3 seconds or less (per each lead).

**Caution** For through-hole device, the wave soldering process must be applied only to leads, and make sure that the package body does not get jet soldered.

## REFERENCE DOCUMENTS

- ★ QUALITY GRADES ON NEC SEMICONDUCTOR DEVICES C11531E
- SEMICONDUCTOR DEVICE MOUNT MANUAL <http://www.necel.com/pkg/en/mount/index.html>
- NEC SEMICONDUCTOR DEVICE RELIABILITY/QUALITY CONTROL SYSTEM IEI-1212
- (STANDARD LINEAR IC)

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