SILICON STACKED GATE MOS INTEGRATED CIRCUIT

TENTATIVE

TC534000AFT

4M BIT (512K WORD × 8 BIT) CMOS MASK ROM

DESCRIPTION

The TC534000AFT is a 4,194,304 bits read only memory organized as 524,288 words by 8 bits.

The TC534000AFT is fabricated using Toshiba's advanced CMOS technology which provides the high speed and low power features with access time of 150ns, an operation current of 40mA at 6.7MHz and a standby current of 20μA.

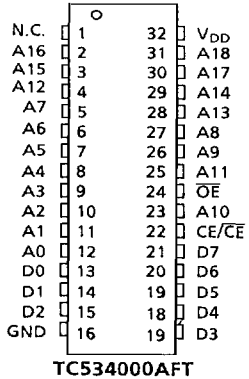
The TC534000AFT has one programmable chip enable input $\overline{CE}$/CE for device selection.

The TC534000AFT is packaged in a 400mil 32 pin TSOP Type II.

FEATURES

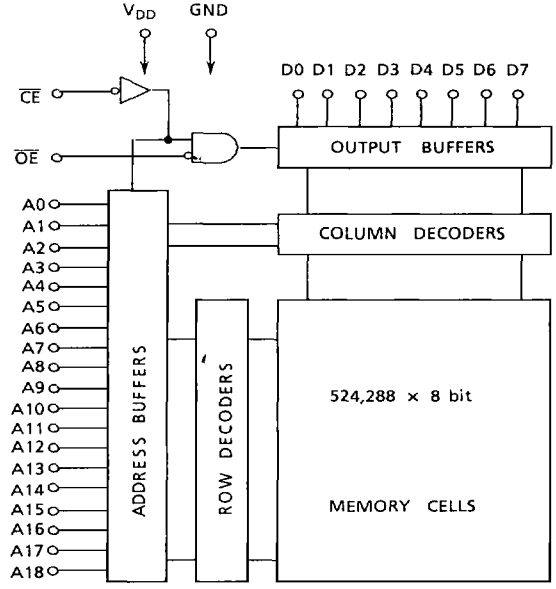
- Single 5V Power Supply
- Access Time : 150ns (Max.) V_{DD}=5V±10%
- Power Dissipation
  - Operating Current : 40mA (Max.)
  - Standby Current : 20μA (Max.)
- All Inputs and Outputs : TTL Compatible
- Three State Outputs
- Fully Static Operation
- Programmable Chip Enable
- TC534000AFT : TSOP32−P−400

PIN CONNECTION



TC534000AFT

BLOCK DIAGRAM



PIN NAMES

A0~A18	Address inputs
D0~D7	Data Outputs
$\overline{OE}$	Output Enable Input
CE/$\overline{CE}$	Chip Enable Input
V_{DD}	Power Supply
GND	Ground
N.C.	No Connection

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.5~7.0	V
V_{IN}	Input Voltage	−0.5~V_{DD}	V
V_{OUT}	Output Voltage	0~V_{DD}	V
P_D	Power Dissipation	0.6	W
T_{STG}	Storage Temperature	−55~150	°C
T_{OPR}	Operating Temerature	0~70	°C
T_{SOLDER}	Soldering Temerature · Time	260 · 10	°C · sec

D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.5	V
V_{IH}	Input High Voltage	2.2	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	−0.3	0.8	V

D.C. and OPERATING CHARACTERISTICS (V_{DD} = 5V ± 10% , Ta = 0~70°C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0~V_{DD}	−	± 1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} , V_{OUT} = 0~V_{DD}	−	± 5.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V	−1.0	−	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V	2.0	−	mA
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}	−	2	mA
I_{DDS2}		$\overline{CE}$ = V_{DD} and V_{IN} = 0V (V_{DD})	−	20	μA
I_{DDO1}	Operating Current	V_{IN} = V_{IH} / V_{IL} , t_{cycle} = 150ns	−	50	mA
I_{DDO2}		V_{IN} = V_{DD} / 0V , t_{cycle} = 150ns	−	40	mA

CAPACITANCE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	f = 1MHz , Ta = 25°C	−	10	pF
C_{OUT}	Output Capacitance	f = 1MHz , Ta = 25°C	−	10	pF

Note : This Parameter is periodically sampled and is not 100% tested.

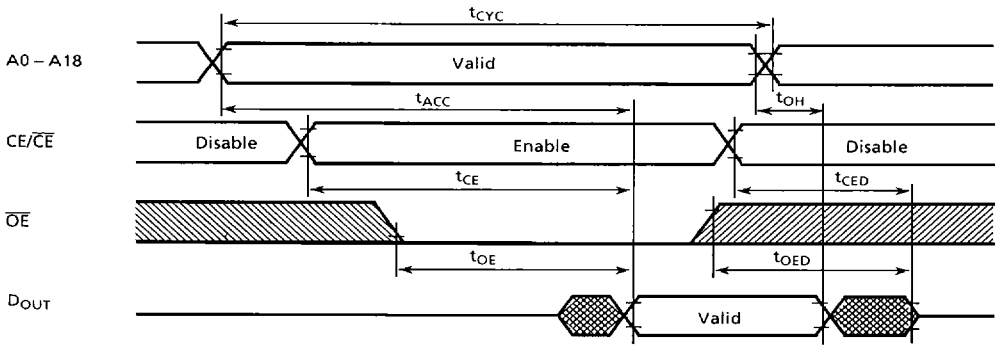
A.C. CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{ACC}	Access Time	–	150	ns
t_{CE}	Chip Enable Access Time	–	150	ns
t_{OE}	Output Enable Access Time	–	70	ns
t_{CED}	Output Disable Time from $\overline{CE}$	0	60	ns
t_{OED}	Output Disable Time from $\overline{OE}$	0	60	ns
t_{OH}	Output Hold Time	5	–	ns
t_{CYC}	Cycle Time	150	–	ns

A.C. TEST CONDITIONS

Output Load		: 100pF + 1TTL
Input Levels		: 0.6V , 2.4V
Timing Measurement Reference Levels	Input	: 0.8V , 2.2V
	Output	: 0.8V , 2.0V
Input Rise and Fall Time		: 5ns

TIMING WAVEFORMS



OPERATION MODE

MODE	$\overline{CE}$ (CE)	$\overline{OE}$	A0~A18	Outputs	Power
Read	L (H)	L	Valid	Data Out	Operating
Standby	H (L)	*	*	High-Z	Standby
Output Deselect	L (H)	H	*	High-Z	Operating

H : VIH L : VIL * : VIH or VIL