42 AMP, 200 VOLT 3 PHASE BRIDGE SMART POWER HYBRID

4320

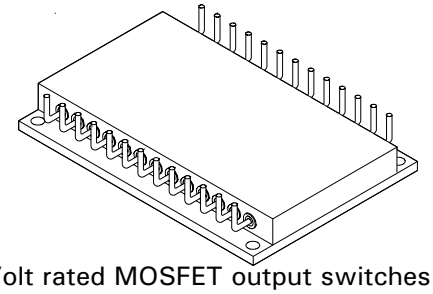
M.S.KENNEDY CORP.

4707 Dey Road Liverpool, N.Y. 13088 (315) 701-6751

MIL-PRF-38534 CERTIFIED

FEATURES:

- 200V, 42 Amp Capability
- Ultra Low Thermal Resistance - Junction to Case - 0.3°C/W
- Self-Contained, Smart Low Side/High Side Drive Circuitry
- Internal dv/dt and di/dt Control
- Internal Under-Voltage, Short-Circuit Protection
- Programmable 5V TTL/CMOS or 15V CMOS Inputs
- Capable of Switching Frequencies from DC to 50KHz



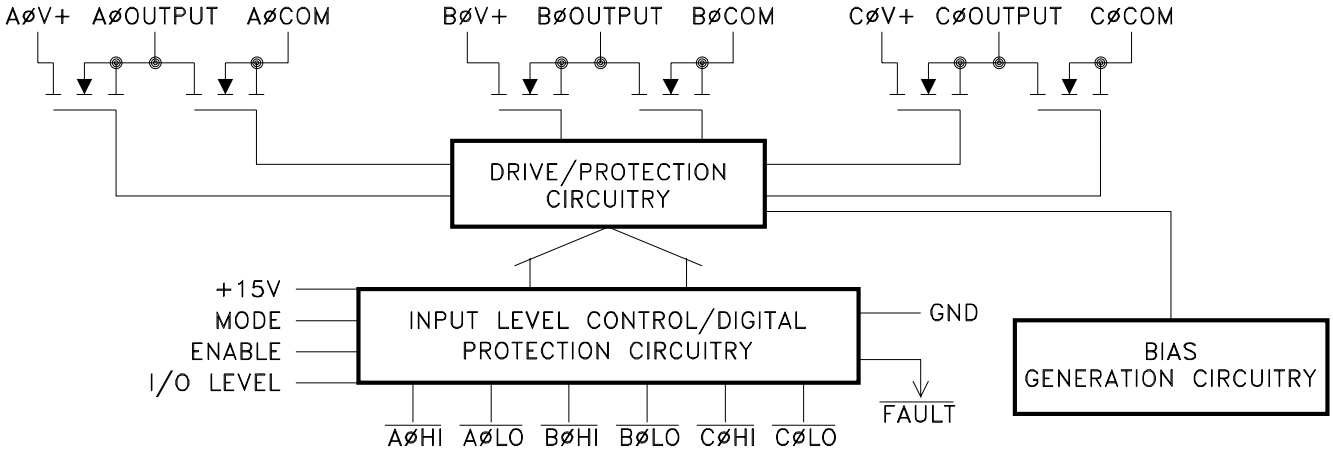
DESCRIPTION:

The MSK 4320 is a 42 Amp, 3 Phase Bridge Smart Power Hybrid with 200 Volt rated MOSFET output switches. The output switches are a new family of power MOSFETs with intrinsic fast recovery diodes worthy of being used instead of blocked out and replaced with other diodes. These diodes are capable of operating currents that match the MOSFETs along with excellent reverse recovery times specified at typical high current operating conditions, not small signal diode recovery conditions. These diodes are fully capable of being used as flyback diodes for the inductive environments of motor drives.

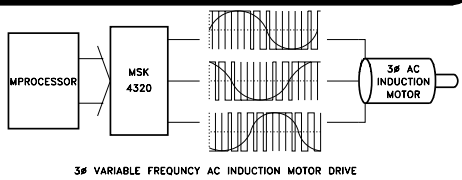
This new smart power motor drive hybrid has 5V TTL/CMOS or 15V CMOS compatible inputs with Schmitt triggered buffers for high noise immunity. Internal smart circuitry prevents simultaneous turn-on of in-line transistors, eliminating shoot-through. The circuitry contains an ENABLE pin for shutdown of the complete drive. Fault protection, in the form of short-circuit output and under-voltage lockout from the bias supply, prevents large scale catastrophic conditions. Dv/dt and di/dt limiting circuitry is also included to protect the switches and the hybrid.

The internal high-side power supply, derived from the +15 volt bias, completely eliminates the need for floating high side power supplies to be provided by the user. A unique feature of the convenient on-board supply is its ability to supply the high-side drive for the upper switch at DC output conditions without total dependency on output switching.

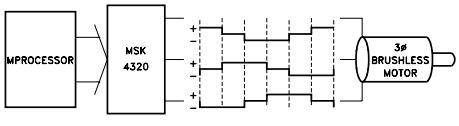
EQUIVALENT SCHEMATIC



TYPICAL APPLICATIONS



3ø VARIABLE FREQUNCY AC INDUCTION MOTOR DRIVE



3ø BRUSHLESS DC MOTOR DRIVE

PIN-OUT INFORMATION

1	Enable	10	$\overline{\text{AØLO}}$	19	N/C
2	Mode	11	I/O Level	20	BØOutput
3	$\overline{\text{Fault}}$	12	$\overline{\text{BØLO}}$	21	BØV+
4	N/C	13	$\overline{\text{CØLO}}$	22	N/C
5	+15V	14	CØCOM	23	AØCOM
6	$\overline{\text{Gnd}}$	15	CØOutput	24	AØOutput
7	$\overline{\text{AØHI}}$	16	CØV+	25	AØV+
8	$\overline{\text{BØHI}}$	17	N/C	26	N/C
9	$\overline{\text{CØHI}}$	18	BØCOM		

ELECTRICAL SPECIFICATIONS

Parameter	Test Conditions	Group A Subgroup ④ ⑤	MSK 4320B ③ Min.	Typ. ①	Max.	MSK 4320 ② Min.	Typ. ①	Max.	Units
OUTPUT SWITCH CHARACTERISTICS									
Output On-Resistance (Each FET)	I_D = 42Amps	1	-	-	0.1	-	-	0.12	Ω
		2	-	-	0.225	-	-	-	Ω
		3	-	-	0.075	-	-	-	Ω
Instant Forward Voltage (Intrinsic Diode)	I_S = 42Amps	1	-	-	1.6	-	-	1.9	V
		2	-	-	1.4	-	-	-	V
		3	-	-	1.8	-	-	-	V
Leakage Current (Each FET)	V_{DS} = 200V	1	-	-	250	-	-	300	uA
	V_{DS} = 160V	2	-	-	1	-	-	-	mA
	V_{DS} = 200V	3	-	-	250	-	-	-	uA
BIAS SUPPLY CHARACTERISTICS + 15V SUPPLY									
Quiescent Bias Current	V_{DD} = 15VDC	1	-	-	10	-	-	10	mA
		2	-	-	15	-	-	-	mA
		3	-	-	10	-	-	-	mA
Bias Current (@ 50KHz Switching)	V_{DD} = 15VDC	1	-	-	150	-	-	150	mA
		2	-	-	200	-	-	-	mA
		3	-	-	150	-	-	-	mA
INPUT SIGNAL CHARACTERISTICS									
LOGIC INPUTS-ENABLE, A,B,C (HI And LO)									
Input Voltage-Low	Mode = 5VDC	1	-	1.3	0.8	-	1.3	0.8	V
	I/O Level = 5Vdc	2,3	-	-	0.8	-	-	-	V
	Mode = 0VDC	1	-	-	1.5	-	-	1.5	V
	I/O Level = 5VDC	2,3	-	-	1.5	-	-	-	V
	Mode = 0VDC	1	-	-	3.75	-	5.0	3.75	V
	I/O Level = 15VDC	2,3	-	-	3.75	-	-	-	V
Input Voltage-High	Mode = 5VDC	1	2.0	1.5	-	2.0	1.5	-	V
	I/O Level = 5VDC	2,3	2.0	-	-	-	-	-	V
	Mode = 0VDC	1	3.5	2.75	-	3.5	2.75	-	V
	I/O Level = 5VDC	2,3	3.6	-	-	-	-	-	V
	Mode = 0VDC	1	11.25	-	-	11.25	-	-	V
	I/O Level = 15VDC	2,3	11.25	-	-	-	-	-	V
OUTPUT SIGNAL CHARACTERISTICS									
FAULT OUTPUT:									
Output Voltage-Low	NO LOAD-Fault Output	1	-	-	0.05	-	-	0.05	V
		2,3	-	-	0.05	-	-	-	V
Output Voltage-High	NO LOAD-Fault Output	1	14.95	-	-	14.95	-	-	V
		2,3	14.95	-	-	-	-	-	V
Output Current-Source/Sink		1	±3.4	±8.8	-	±3.4	±8.8	-	mA
		2	±2.4	-	-	-	-	-	mA
		3	±4.2	-	-	-	-	-	mA
SWITCHING CHARACTERISTICS									
UPPER DRIVE:									
Turn-On Propagation Delay	V + AØ,BØ,CØ = 100V I_O = 42Amps	4	-	208	675	-	208	810	nS
Turn-On Rise Time		4	-	65	170	-	65	204	nS
Turn-Off Propagation Delay		4	-	312	915	-	312	1098	nS
Turn-Off Fall Time		4	-	51	125	-	51	150	nS
LOWER DRIVE:									
Turn-On Propagation Delay	V + AØ,BØ,CØ = 100V I_O = 42Amps	4	-	88	225	-	88	270	nS
Turn-On Rise Time		4	-	65	170	-	65	204	nS
Turn-Off Porpagation Delay		4	-	172	390	-	172	468	nS
Turn-Off Fall Time		4	-	51	125	-	51	150	nS
Reverse Recovery Time ①	I_F = 25A di/dt = 100A/μS V_R = 100V, T_J = 125°C	-	-	-	300	-	-	300	nS
Reverse Recovery Charge ①		-	-	1.6	-	-	1.6	-	μCoul
Peak Recovery Current ①		-	-	23	-	-	23	-	A

NOTES:

① Guaranteed by design but not tested. Typical parameters are representative of actual device performance but are for reference only.
② Industrial grade devices shall be tested to subgroups 1 and 4 unless otherwise specified.
③ Military grade devices ('B' suffix) shall be 100% tested to subgroups 1,2,3 and 4.
④ Subgroup 5 and 6 testing available upon request.
⑤ Subgroup 1,4 $T_A = T_C = +25°C$
Subgroup 2,5 $T_A = T_C = +125°C$
Subgroup 3,6 $T_A = T_C = -55°C$

ABSOLUTE MAXIMUM RATINGS

$V+$	Output Supply Voltage	200V
I_O	Output Current (Continuous)	42A
I_P	Output Current (Peak)	168A
E_{AR}	Maximum Repetitive Avalanche Energy	30mJ
V_{BIAS}	Bias Supply Voltage	+18V
V_{IN}	I/O Level, Mode	+18V
V_L	Logic Input Voltages	(I/O Level + 0.3V)
P_D	Power Dissipation @ 125 °C (Each Transistor)	83W
$R_{\theta JC}$	Thermal Resistance (Output Transistor)	0.3°C/W
T_L	Lead Temperature For Soldering (10 Seconds)	300°C
T_C	Case Operating Temperature MSK4320	-40°C to +85°C
	MSK4320B	-55°C to +125°C
T_{STG}	Storage Temperature Range	-65°C to +150°C
T_J	Junction Temperature Operating Maximum	+150°C

APPLICATION NOTES

PIN DESCRIPTION

+15V - Is the low voltage supply for all the internal logic and drivers. A 0.1µF ceramic capacitor in parallel with a 1uF tantalum capacitor is recommeded bypassing for the **+15V-GND** pins.

GND - Is the low voltage supply return pin and the input logic return reference. All logic input and logic output is referenced to this pin. This pin can vary ±5 volts from the **COM** power return pins without affecting any of the logic functions.

MODE - Is an input which controls the type of levels for all logic signal inputs. A 5 volt level at this input causes all input logic to be **TTL** compatible. A 0 volt level at this input causes all input logic to be **CMOS** compatible.

ENABLE - Is a control input which will turn off the complete bridge, causing all output switches to be turned off. This input logic level will follow the **MODE** and **I/O LEVEL** settings.

I/O LEVEL - Is a control input for controlling input logic level voltages. 5 volts on this pin causes 5 volt **I/O** compatibility (**TTL** or **CMOS**), and 15 volts on this pin causes 15 volt **CMOS I/O** compatibility.

$\overline{\text{AØHI}}$, $\overline{\text{BØHI}}$, $\overline{\text{CØHI}}$ - Are low active logic inputs for signaling the corresponding phase high-side switch to turn on. The input levels follow the **MODE** and **I/O LEVEL** settings. Typical propagation delays are around 1µS.

$\overline{\text{AØLO}}$, $\overline{\text{BØLO}}$, $\overline{\text{CØLO}}$ - Are low active logic inputs for signaling the corresponding phase low-side switch to turn on. The input levels follow the **MODE** and **I/O LEVEL** settings. Typical propagation delays are around 1µS.

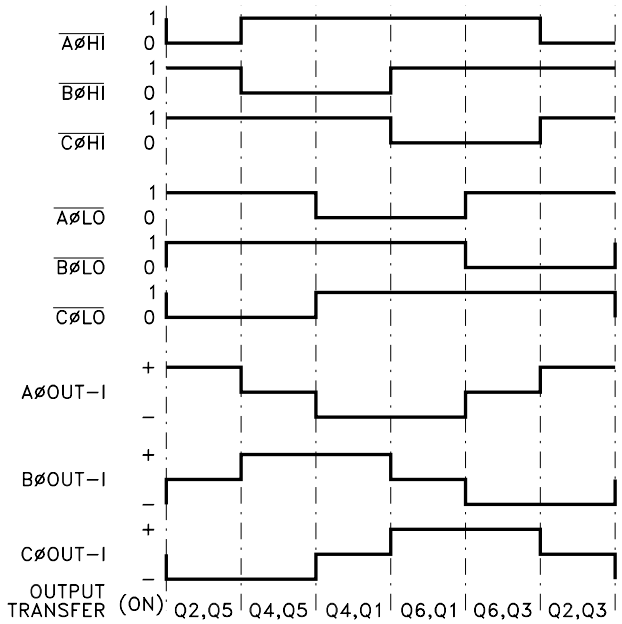
$\overline{\text{FAULT}}$ - Is a logic output pin that gets enabled any time the **VCC** level goes below the cutoff point, or an overcurrent condition occurs. Bringing **VCC** back to normal levels will reset **$\overline{\text{FAULT}}$**. Removing the overcurrent conditioin and allowing the low-side logic inputs to remain low (off) for 10µS will restore operation. The logic output level follows the **MODE** and **I/O LEVEL** settings.

AØ+, BØ+, CØ+ - Is the high voltage positive rail for each phase of the bridge. Proper bypassing to each phase **COM** with sufficient capacitance to suppress any voltage transients, and to ensure removing any drooping during switching should be done as close to the pins on the hybrid as possible.

AØCOM, BØCOM, CØCOM - Is the return side for each phase of the bridge. A sense resistor can be connected between this point and **GND**, which is the high voltage negative rail. **COM**'s can float above and below the **GND** pin up to 5 volts and proper operation will be maintained. Precautions should be taken not to allow this voltage to exceed ±5 volts under any conditions.

AØ, BØ, CØ - Are the pins connecting the 3 phase bridge switch outputs.

THREE PHASE, SIX STEP, FULL WAVE COMMUTATION WAVEFORMS



APPLICATION NOTES CON'T

PROTECTION:

- All logic inputs use a 300nS filter. A pulse width below this will get ignored.
- **VCC** voltage below the cutoff level of 8.65 volts will reset all switch outputs off and ignore subsequent logic inputs until **VCC** is restored.
- Undervoltage lockout of the internal drivers for the high-side switches also occurs at 8.65 volts, but will not flag with the **FAULT** output. This may occur if the high-side output gets switched at greater than 25kHZ without switching the low-side. The internal power supply for the high-side switch will sag too low for adequate switching. Either slow down the PWM rate or PWM the low-side switches instead.
- Switching a low-side logic input while the corresponding phase high-side logic input is activated will be ignored until the high-side is turned off. The opposite condition is also true. This is cross-conduction lockout and will occur any time low and high-side inputs for a phase are activated at the same time.
- A 2µS deadtime is automatically inserted between high and low-side output switching to allow complete turn-off of each switch, and no overlap will occur.

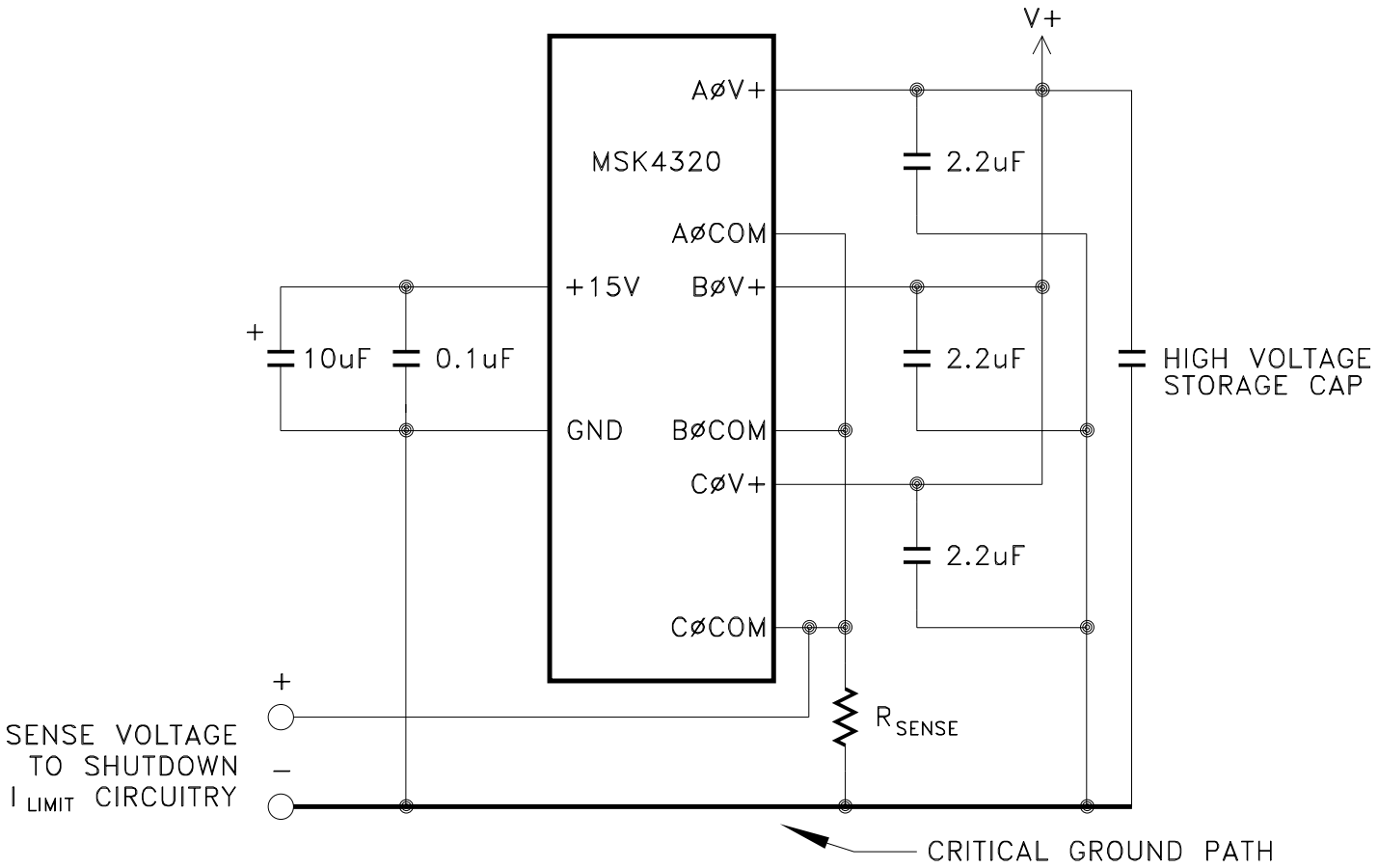
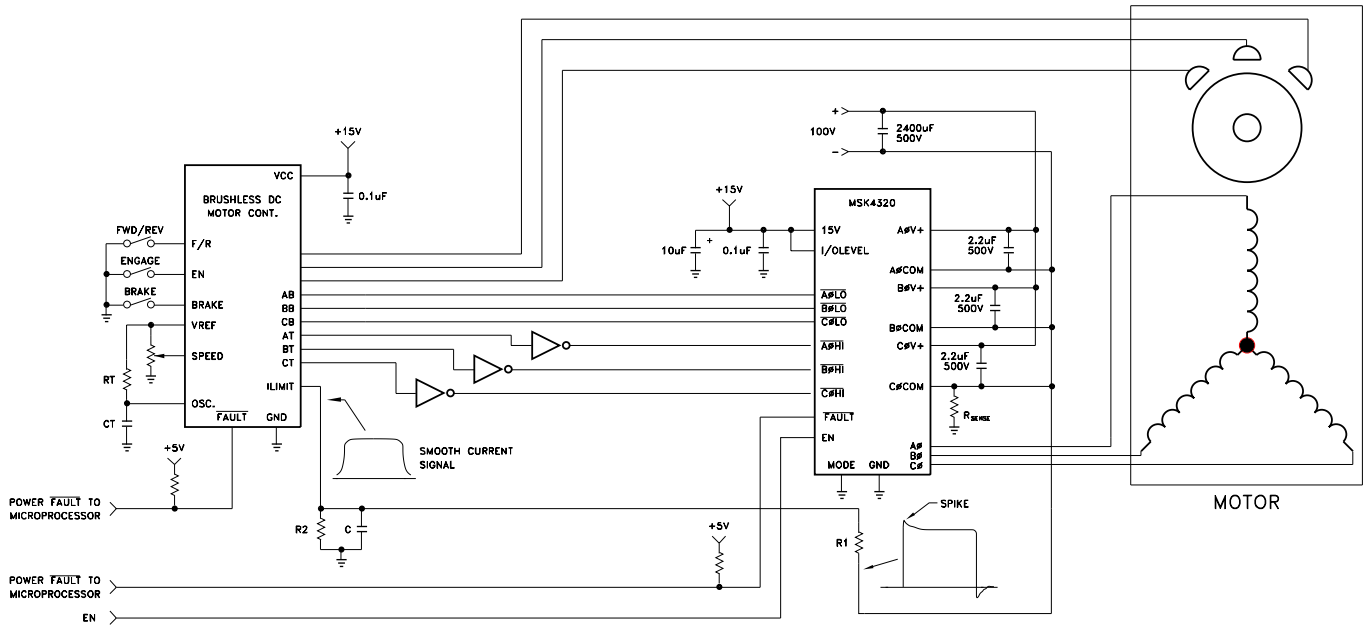


FIGURE 1

BYPASSING, GROUNDING, CURRENT SENSE

TYPICAL SYSTEM OPERATION



TRUTH TABLE FOR EACH PHASE		
$\overline{LIN}$	$\overline{HIN}$	OUTPUT
L	L	FLOAT(INVALID STATE)
H	L	HIGHSIDE ON
L	H	LOWSIDE ON
H	H	FLOAT

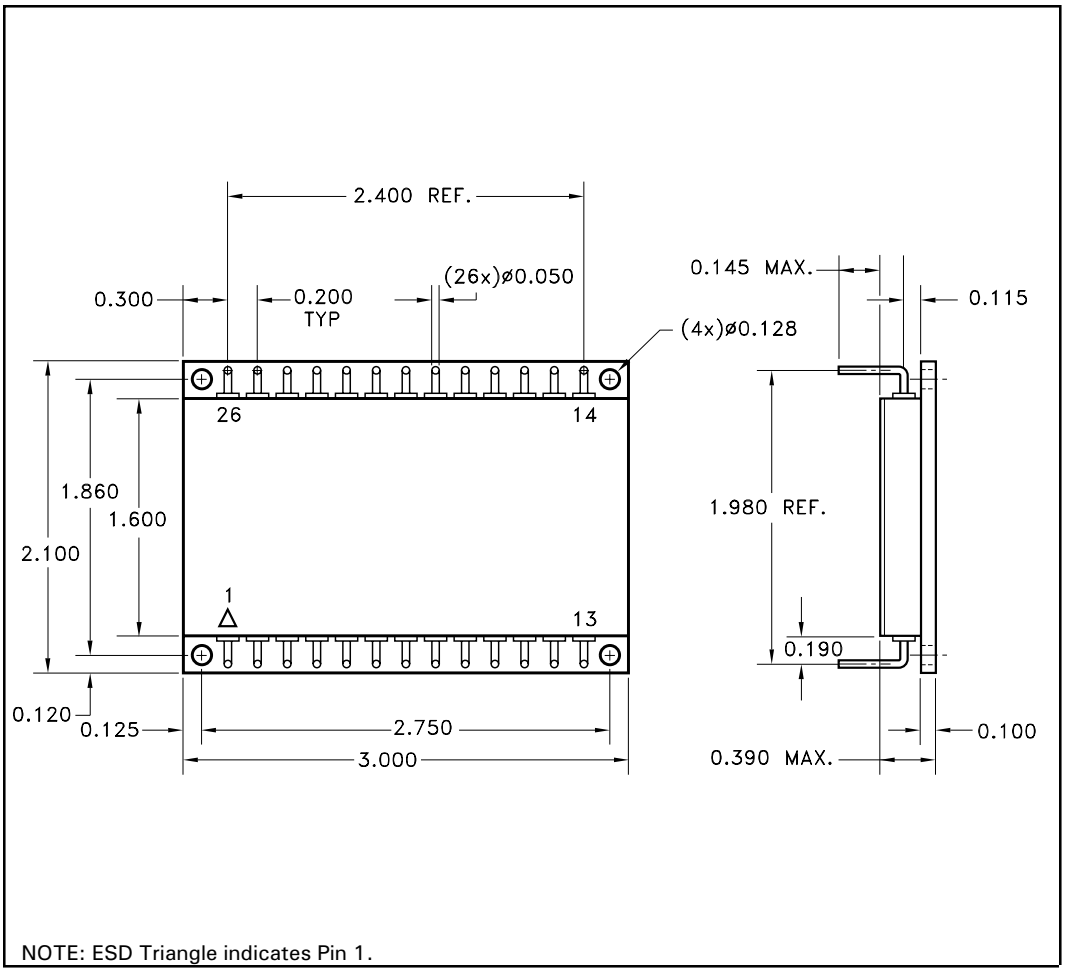
The MSK4320 is designed to be used with a +100 volt high voltage bus, +15 volt low power bus, and +15 volt logic signals. Proper deratings should be applied when designing the MSK4320 into a system. High frequency layout techniques with ground planes on a printed circuit board are the only method that should be used for circuit construction. This will prevent pulse jitter caused by excessive noise pickup on the current sense signal or the error amp signal.

Ground planes for the power circuitry and high power circuitry should be kept separate. The connection between the bottom of the current sense resistor, ground pin, and the high power coms are connected at this point. This is a critical path and high currents should not be flowing between the current sense and coms. Inductance in this path should be kept to a minimum. An RC filter will filter out the current spike and keep the detected noise for those circuits down to a minimum. In the system shown above, the limit is a PWM pulse by pulse limit controlled by the motor controller.

When controlling the motor speed by the PWM method, it is recommended that the low side switches be PWM pulsed due to the limited power supplies used to power the high side switch drives. The high side power supplies are completely isolated from the low side and are designed to keep the high side alive for continuous high side conduction in the case of a rotor stall or startup. The higher the PWM speed the higher the current load on the drive supply. PWMing the low side will prevent loading the high side supplies.

The logic signals coming from the typical motor control IC are set up for driving N channel low side and P channnel high side switches directly, and are usually 15 volt levels. Typically, the low side signals out of the controller are high active and the high side are low active. Inverters are shown in the system schematic for the high side controller output.

MECHANICAL SPECIFICATIONS



NOTE: ESD Triangle indicates Pin 1.

ALL DIMENSIONS ARE ±0.010 INCHES UNLESS OTHERWISE LABELED

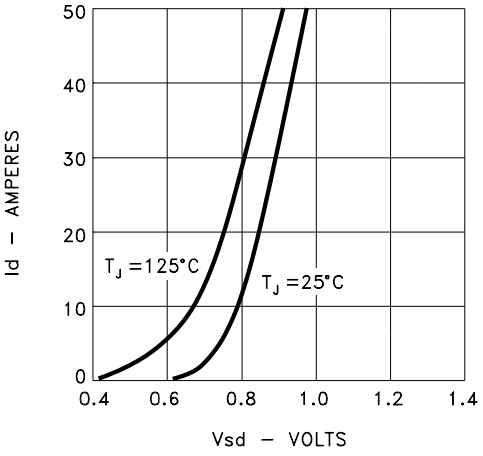
ORDERING INFORMATION

Part Number	Screening Level
MSK4320	Industrial
MSK4320B	Military-Mil-PRF-38534

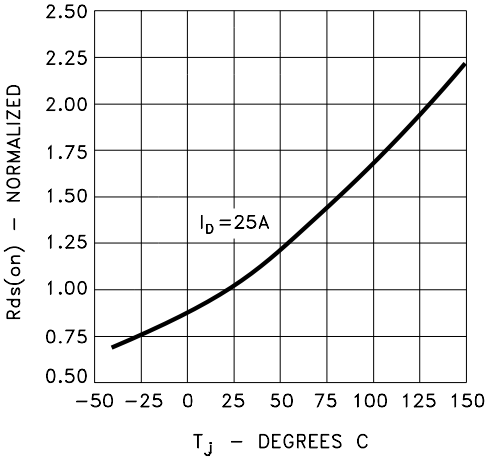
M.S. Kennedy Corp.
4707 Dey Road, Liverpool, New York 13088
Phone (315) 701-6751
FAX (315) 701-6752
www.mskennedy.com

TYPICAL PERFORMANCE CURVES

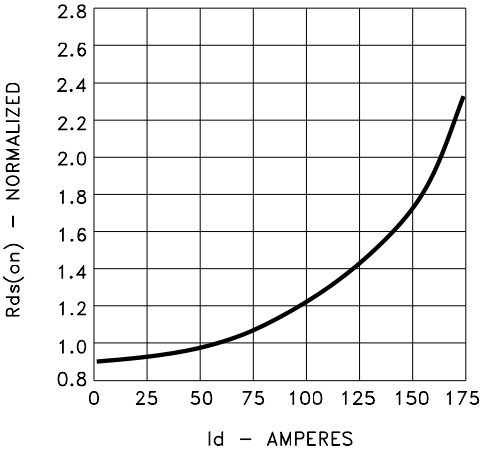
SOURCE CURRENT vs SOURCE TO DRAIN VOLTAGE



TEMPERATURE DEPENDENCE OF DRAIN TO SOURCE RESISTANCE



Rds(on) vs DRAIN CURRENT



TEMPERATURE DEPENDENCE OF BREAKDOWN VOLTAGE