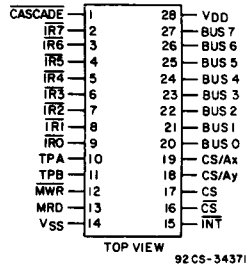
CDP1877, CDP1877C



TERMINAL ASSIGNMENT

Programmable Interrupt Controller (PIC)

Features:

- *Compatible with CDP1800 series*
- *Programmable long branch vector address and vector interval*
- *8 levels of interrupt per chip*
- *Easily expandable*
- *Latched interrupt requests*
- *Hard wired interrupt priorities*
- *Memory mapped*
- *Multiple chip select inputs to minimize address space requirements*

The RCA-CDP1877 and CDP1877C• are programmable 8-level interrupt controllers designed for use in CDP1800-series microprocessor systems. They provide added versatilty by extending the number of permissible interrupts from 1 to N in increments of 8.

When a high to low transition occurs on any of the PIC interrupt lines ($\overline{IR0}$ to $\overline{IR7}$), it will be latched and, unless the request is masked, it will cause the $\overline{INTERRUPT}$ line on the PIC and consequently the $\overline{INTERRUPT}$ input on the CPU to go low.

The CPU accesses the PIC by having interrupt vector register R(1) loaded with the memory address of the PIC. After the interrupt S3 cycle, this register value will appear at the CPU address bus, causing the CPU to fetch an instruction from the PIC. This fetch cycle clears the interrupt request latch bit to accept a new high-to-low transition, and also causes the PIC to issue a long branch instruction (CO) followed by the preprogrammed vector address written into the PIC's address registers, causing the CPU to branch to the address corresponding to the highest priority active interrupt request.

• Formerly RCA-Dev. Type No. TA10911 and TA10911C, respectively.

If no other unmasked interrupts are pending, the $\overline{INTERRUPT}$ output of the PIC will return high. When an interupt is requested on a masked interrupt line, it will be latched but it will not cause the PIC $\overline{INTERRUPT}$ output to go low. All pending interrupts, masked and unmasked, will be indicated by a "1" in the corresponding bit of the status register. Reading of the status register will clear all pending interrupt request latches.

Several PICs can be cascaded together by connecting the $\overline{INTERRUPT}$ output of one chip to the $\overline{CASCADE}$ input of another. Each cascaded PIC provides 8 additional interrupt levels to the system. The number of units cascadable depends on the amount of memory space and the extent of the address decoding in the system.

Interrupts are prioritized in descending order; $\overline{IR7}$ has the highest and $\overline{IR0}$ has the lowest priority.

The CDP1877 and CDP1877C are functionally identical. They differ in that the CDP1877 has a recommended operating voltage range of 4 to 10.5 volts, and the CDP1877C has a recommended operating voltage range of 4 to 6.5 volts. They types are supplied in 28-lead dual-in-line ceramic packages (D suffix), and 28-lead dual-in-line plastic packages (E suffix).

Programmable Interrupt Controller (PIC) Programming Model

BUS 7						BUS 0	
A15	A14	A13	PAGE REGISTER A12	A11	A10	A9	A8	WRITE ONLY
BUS 7						BUS 0	
B7	B6	B5	CONTROL REGISTER B4	B3	B2	B1	B0	WRITE ONLY
BUS 7						BUS 0	
M7	M6	M5	MASK REGISTER M4	M3	M2	M1	M0	WRITE ONLY
BUS 7						BUS 0	
S7	S6	S5	STATUS REGISTER S4	S3	S2	S1	S0	READ ONLY
BUS 7						BUS 0	
P7	P6	P5	POLLING REGISTER P4	P3	P2	P1	P0	READ ONLY

File Number **1319**

CDP1877, CDP1877C

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltage referenced to V_{SS} terminal)
CDP1877 ..... −0.5 to +11 V
CDP1877C ..... −0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A=−40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A=+60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW
For T_A=−55 to +100°C (PACKAGE TYPE D) ..... 500 mW
For T_A=+100 to 125°C (PACKAGE TYPE D) ..... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A=FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE D ..... −55 to +125°C
PACKAGE TYPE E ..... −40 to +85°C
STORAGE-TEMPERATURE RANGE (T_{stg}) ..... −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

4

STATIC ELECTRICAL CHARACTERISTICS at T_A=−40 to +85°C, V_{DD} ±5%, Except as noted

CHARACTERISTIC		CONDITIONS			LIMITS						UNITS
		V_O (V)	V_{IN} (V)	V_{DD} (V)	CDP1877 Min.	CDP1877 Typ.*	CDP1877 Max.	CDP1877C Min.	CDP1877C Typ.*	CDP1877C Max.	
Quiescent Device Current	I_{DD}	—	0, 5	5	—	0.01	50	—	0.02	200	μA
		—	0, 10	10	—	1	200	—	—	—	
Output Low Drive (Sink) Current	I_{OL}	0.4	0, 5	5	1.6	3.2	—	1.6	3.2	—	mA
		0.5	0, 10	10	2.6	5.2	—	—	—	—	
Output High Drive (Source) Current	I_{OH}	4.6	0, 5	5	−1.15	−2.3	—	−1.15	−2.3	—	
		9.5	0, 10	10	−2.6	−5.2	—	—	—	—	
Output Voltage Low-Level	V_{OL}‡	—	0, 5	5	—	0	0.1	—	0	0.1	V
		—	0, 10	10	—	0	0.1	—	—	—	
Output Voltage High Level	V_{OH}‡	—	0, 5	5	4.9	5	—	4.9	5	—	
		—	0, 10	10	9.9	10	—	—	—	—	
Input Low Voltage	V_{IL}	0.5,4.5	—	5	—	—	1.5	—	—	1.5	
		0.5,9.5	—	10	—	—	3	—	—	—	
Input High Voltage	V_{IH}	0.5,4.5	—	5	3.5	—	—	3.5	—	—	
		0.5,9.5	—	10	7	—	—	—	—	—	
Input Leakage Current	I_{IN}	Any Input	0, 5	5	—	—	±1	—	—	±1	μA
			0, 10	10	—	—	±2	—	—	—	
3-State Output Leakage Current	I_{OUT}	0, 5	0, 5	5	—	$\pm 10^{-4}$	±1	—	$\pm 10^{-4}$	±1	
		0, 10	0, 10	10	—	$\pm 10^{-4}$	±10	—	—	—	
Input Capacitance	C_{IN}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance	C_{OUT}	—	—	—	—	10	15	—	10	15	
Operating Device Current	I_{OPER}#			5	—	0.5	1.0	—	0.5	1.0	mA
				10	—	1.9	3.0	—	—	—	

*Typical values are for T_A=25°C and nominal V_{DD}. ‡I_{OL}=I_{OH}=1 μA.

Operating current measured under worst-case conditions in a 3.2-MHz CDP1802A system: one PIC access per instruction cycle.

CDP1877, CDP1877C

OPERATING CONDITIONS at T_A=Full Package-Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1877		CDP1877C		
	Min.	Max.	Min.	Max.	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	

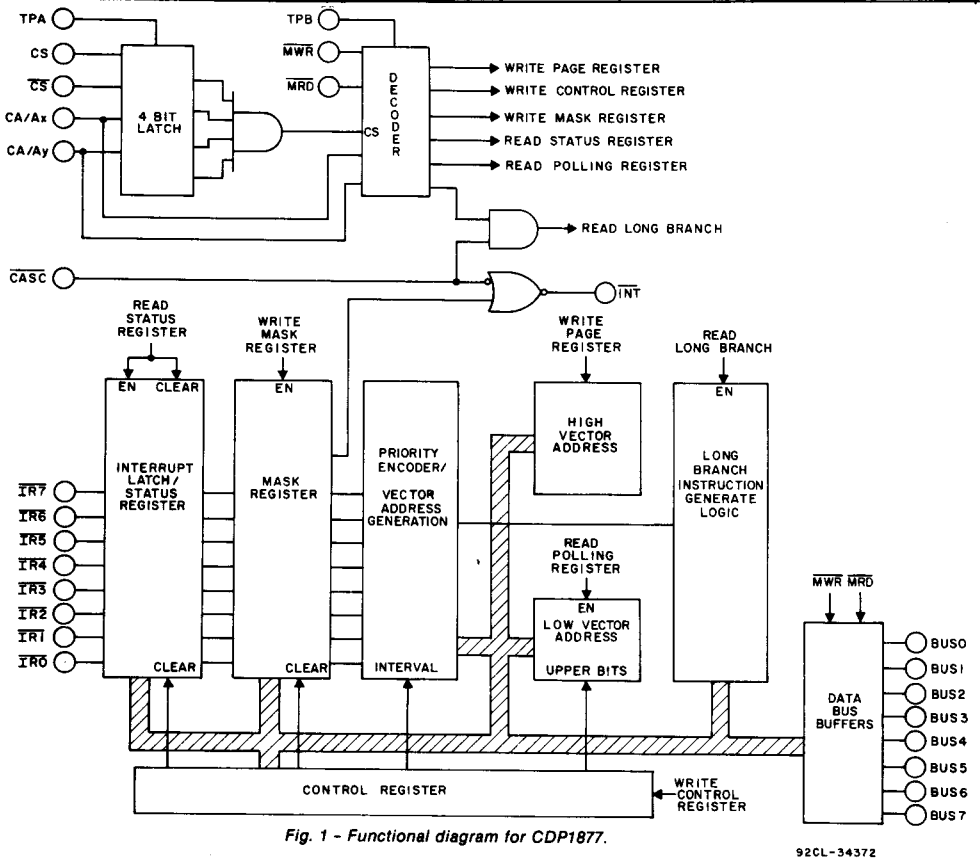


Fig. 1 - Functional diagram for CDP1877.

Functional Definitions for CDP1877 and CDP1877C Terminals

TERMINAL	USAGE	TYPE
V_{DD}—V_{SS}	Power	
BUS0—BUS7	Data bus—Communicates information to and from CPU	Bidirectional
$\overline{IR0}$—$\overline{IR7}$	Interrupt Request Lines	Input
$\overline{INTERRUPT}$	Interrupt to CPU	Output
$\overline{MRD}$, $\overline{MWR}$	Read/Write controls from CPU	Input
TPA, TPB	Timing pulses from CPU	Input
CS, $\overline{CS}$	Chip selects, Enable Chip if valid during TPA	Input
CS/Ax, CS/Ay	Used as a Chip Select during TPA and as a Register address during Read/Write Operations	Input
$\overline{CASCADE}$	Used for cascading several PIC units. The $\overline{INTERRUPT}$ output from a higher priority PIC can be tied to this input, or the input can be tied to Vdd if cascading is not used.	Input

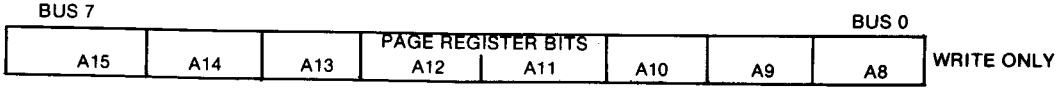
PIC Programming Model

INTERNAL REGISTERS

The PIC has three write-only programmable registers and two read-only registers.

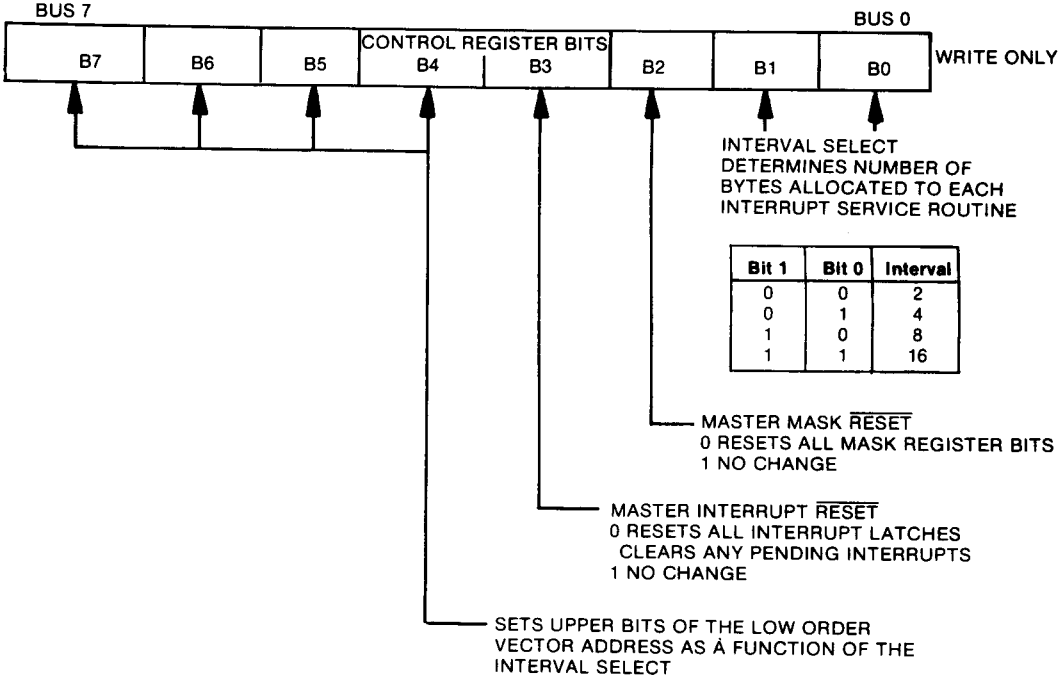
Page Register

This write only register contains the high order vector address the device will issue in response to an interupt request. This high-order address will be the same for any of the 8 possible interrupt requests; thus, interrupt vectoring differs only in location within a specified page.



Control Register

The upper nibble of this write-only register contains the low order vector address the device will issue in response to an interrupt request. The lower nibble is used for a master interrupt reset, master mask reset and for interval select.



Bit 1	Bit 0	Interval
0	0	2
0	1	4
1	0	8
1	1	16

THE LOW ORDER VECTOR ADDRESS WILL BE SET ACCORDING TO THE TABLE BELOW:

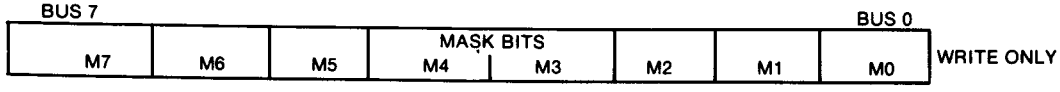
INTERVAL SELECTED- NO. OF BYTES	LOW ADDRESS BITS BIT B7	BIT B6	BIT B5	BIT B4
2	SETS A7	SETS A6	SETS A5	SET A4
4	SETS A7	SETS A6	SETS A5	X
8	SETS A7	SETS A6	X	X
16	SETS A7	X	X	X

X=DON'T CARE

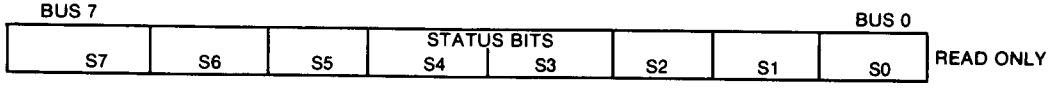
NOTE: All DON'T CARE Addresses and Addresses A0-A3 are determined by interrupt request.

CDP1877, CDP1877C

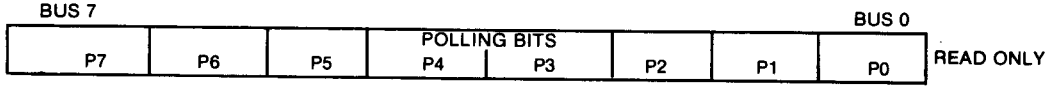
Mask Register
A "1" written into any location in this write only register will mask the corresponding interrupt request line. All interrupt inputs (except CASCADE) are maskable.



Status Register
In this read only register a "1" will be present in the corresponding bit location for every masked or unmasked pending interrupt.

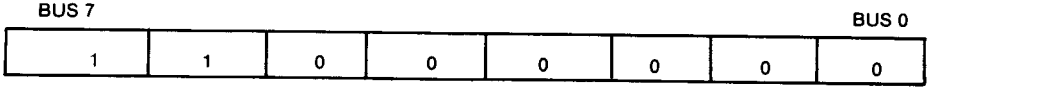


Polling Register
This read only register provides the low order vector address and is used to identify the source of interrupt if a polling technique, rather than interrupt servicing, is used.



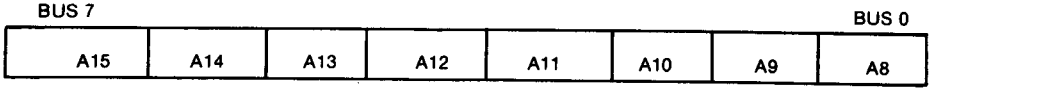
RESPONSE TO INTERRUPT (AFTER S3 CYCLE)
The PIC's response to interrogation by the CPU is always 3 bytes long, placed on the data bus in consecutive bytes in the following format:

First (Instruction) Byte:
LONG BRANCH INSTRUCTION - CO (Hex)

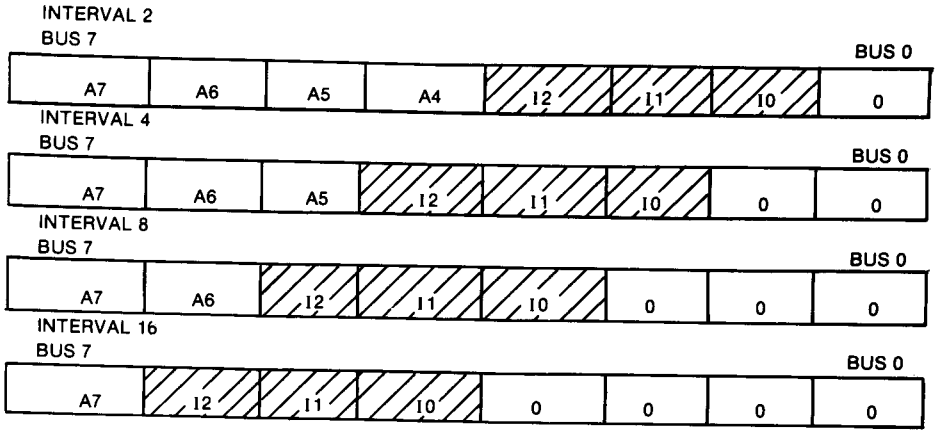


Second (High-Order Address) Byte
This byte is the High-Order vector Address that was written into the PIC's Page Register by the user. The PIC does not alter this value in any way.

High-Order Vector Address



Third (Low-Order Address) Bytes



Indicates active interrupt input number (binary 0 to 7).

Bits indicated by Ax (x=4 to 7) are the same as programmed into the Control Register. All other bits are generated by the PIC.

REGISTER ADDRESSES

In order to read/write or obtain an interrupt vector from any PIC in the system, all chip selects (CS/Ax, CS/Ay, CS, $\overline{CS}$) must be valid during TPA.

CS/Ax and CS/Ay are multiplexed addresses; both must be high during TPA, and set according to this table during TPB to access the proper register.

CS/Ax	CS/Ay	$\overline{RD}$	$\overline{WR}$	ACTION TAKEN
1	0	0	1	READ Long Branch instruction and vector for highest priority unmasked interrupt pending.
1	0	1	0	WRITE to Page Register
0	1	1	0	WRITE to Control Register
0	0	0	1	READ Status Register
0	0	1	0	WRITE to Mask Register
0	1	0	1	READ Polling Register (Used to identify INTERRUPT source if Polling technique rather than INTERRUPT service is used.)
1	1	X	X	Unused condition

CDP1877, CDP1877C

PIC Application Examples

Example I—Single PIC Application

Fig. 2 shows all the connections required between CPU and PIC to handle eight levels of interrupt control.

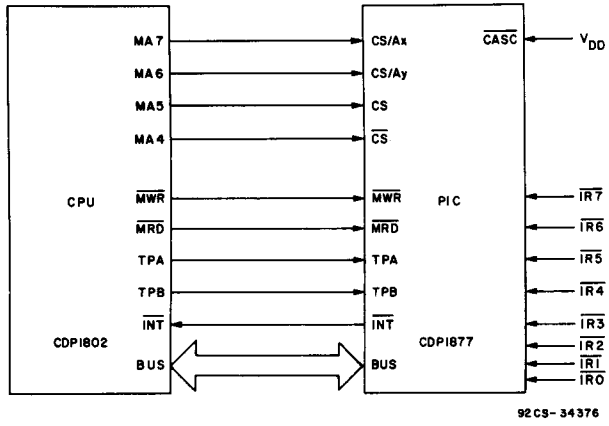


Fig. 2 - PIC and CPU connection diagram.

Programming

Programming the PIC consists of the following steps:

1. Disable interrupt at CPU.
2. Reset Master Interrupt Bit, B3, of Control Register.
3. Write a "1" into the Interrupt Input bit location of the Mask Register, if masking is desired.
4. Write the High-Order Address byte into the Page Register.
5. Write the Low-Order Address and the vector interval into the Control Register.
6. Program R(1) of the CPU to point to the PIC so that the Long Branch instruction can be read from the PIC during the Interrupt Service routine.

Values for Example I with LOCATION 84E0 arbitrarily chosen as the Vector Address with interval of eight bytes, $\overline{IR4}$ pending, is shown in Table I.

In deriving the above addresses, all DON'T CARE bits are assumed to be 0.

When an INTERRUPT ($\overline{IR4}$) is received by the CPU, it will address the PIC and will branch to the interrupt service routine.

The three bytes generated by the PIC will be:

1st Byte=$C0_H$
2nd Byte=84_H
3rd Byte=$E0_H$

Table I — Register Address Values

REGISTER	REGISTER ADDRESS	OPERATION	DATA BYTE
MASK	E000H	WRITE	00_H
CONTROL	E040H	WRITE	CE_H
PAGE	E080H	WRITE	84_H
STATUS	E000H	READ	10_H
POLLING	E040H	READ	E0H
R(1) (IN CPU)	E080H	—	—

Example II—Multi-PIC Application

Fig. 3 shows all the connections required between CPU and PICs to handle sixteen levels of interrupt control.

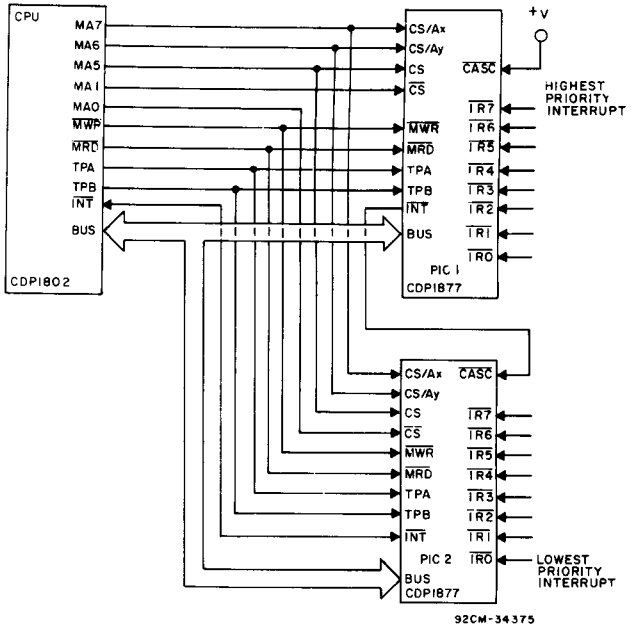


Fig. 3 - PICs and CPU connection diagram.

Register Address Assignments

The low-byte register address for any WRITE or READ operation is the same as shown in Table I.

The high-byte register differs for each PIC because of the linear addressing technique shown in the example:

PIC 1=111XXX01 ($E1_H$ FOR X=0)
PIC 2=111XXX10 ($E2_H$ FOR X=0)

The R(1) vector address is unchanged. This address will select both PICs simultaneously (R(1).1=111XXX00=$E0_H$). Internal CDP1877 logic controls which PIC will respond when an interrupt request is serviced.

Additional PIC Application Comments

The interval select options provide significant flexibility for interrupt routine memory allocations:

- The 2-byte interval allows one to dedicate a full page to interrupt servicing, with variable space between routines, by specifying indirect vectoring with 2 byte short branch instructions on the current page.
- The 4-byte interval allows for a 3 byte long branch to any location in memory where the interrupt service routine is located. The branch can be preceded by a Save Instruction to save previous contents of X and P on the stack.
- The 8-byte and 16-byte intervals allow enough space to perform a service routine without indirect vectoring. The amount of interval memory can be increased even further if all 8 INTERRUPTS are not required. Thus a 4-level interrupt system could use alternate $\overline{IR}$ Inputs, and expand the interval to 16 and 32 bytes, respectively.

The 4 Chip Selects allow one to conserve total allotted memory space to the PIC. For one chip, a total of 4 address lines could be used to select the device, mapping it into as little as 4-K of memory space. Note that this selection technique is the only one that allows the PIC to work properly in the system: I/O mapping cannot be used because the PIC must work within the CDP1800 interrupt structure to define the vector address. Decoded signals also will not work because the chip selects must be valid on the trailing edge of TPA.

CDP1877, CDP1877C

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=-40 to +85°C, V_{DD} ±5%, t_r,t_f=20 ns, V_{IH}=0.7 V_{DD}, V_{IL}=0.3 V_{DD}, C_L=50 pF

CHARACTERISTIC		V_{DD} (V)	LIMITS						UNITS
			CDP1877			CDP1877C			
			Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Address to TPA Setup Time	t_{AS}	5	60	—	—	60	—	—	ns
		10	40	—	—	—	—	—	
Address to TPA Hold Time	t_{AH}	5	60	—	—	60	—	—	
		10	40	—	—	—	—	—	
Data Valid after TPB	t_{DTPB}	5	370	—	—	370	—	—	
		10	210	310	—	—	—	—	
Data Hold Time from Write	t_{HW}	5	30	—	—	30	—	—	
		10	40	—	—	—	—	—	
Address to Valid Data Access Time	t_{DR}	5	—	340	490	—	340	490	
		10	—	125	230	—	—	—	
Data Setup Time to Write	t_{DSU}	5	0	—	—	0	—	—	
		10	0	—	—	—	—	—	
Address Hold from TPB	t_{HTPB}	5	80	—	—	80	—	—	
		10	40	—	—	—	—	—	
Minimum $\overline{MWR}$ Pulse Width	$t_{\overline{MWR}}$	5	130	—	—	130	—	—	
		10	60	—	—	—	—	—	
Minimum $\overline{IR}$ Pulse Width	$t_{\overline{IRX}}$	5	130	—	—	130	—	—	
		10	60	—	—	—	—	—	

* Typical values are for T_A=25°C and V_{DD} ±5%.

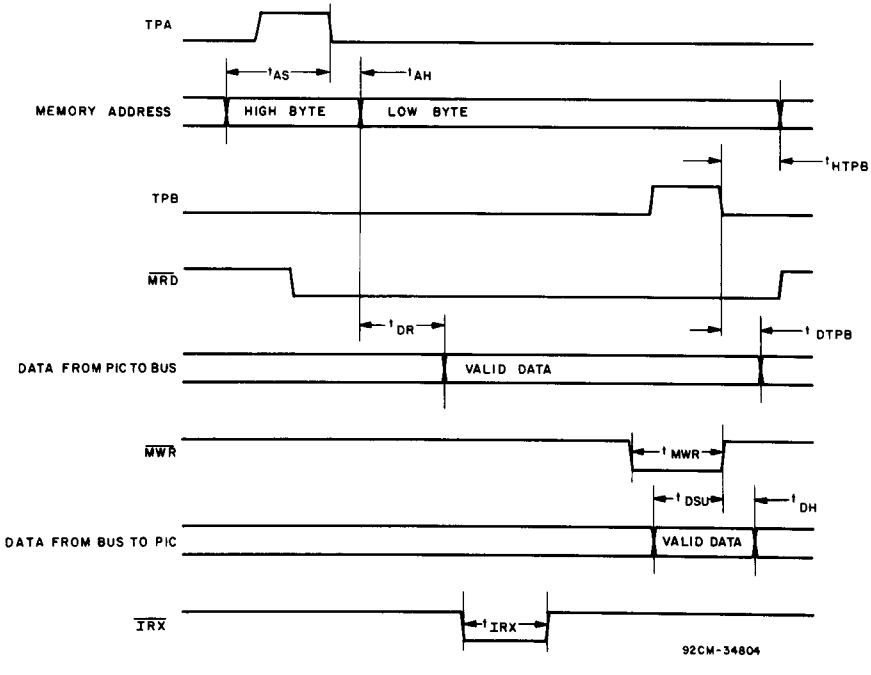


Fig. 4 - Timing waveforms for CDP1877.