4. TMS9914A ELECTRICAL SPECIFICATIONS

4.1 ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)*

Supply voltage, V_{CC} (see Note 1)	−0.3 V to 20 V
All input and output voltages	−0.3 V to 20 V
Continuous power dissipation	0.8 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−55°C to 150°C

* Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1. Under absolute maximum ratings voltage values are with respect to V_{SS}.

4.2 RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Supply voltage, V_{SS}		0		V
High-level input voltage, V_{IH}	2		$V_{CC}+1$	V
Low-level input voltage, V_{IL}	$V_{SS}-0.3$		0.8	V
Operating free-air temperature, T_A	0		70	°C

4.3 ELECTRICAL CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS

PARAMETER			TEST CONDITIONS‡	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	Except REN,IFC,INT	I_{OH} = −400 μA	2.4		V_{CC}	V
		REN,IFC only	I_{OH} = −100 μA	2.2		V_{CC}	
V_{OL}	Low-level output voltage		I_{OL} = 2 mA	V_{SS}		0.4	V
I_I	Input current (any input)		V_I = 2 V to V_{CC}			±10	μA
I_{CC}	V_{CC} supply current					150	mA
C_i	Input capacitance (any input)		f = 1 MHz, unmeasured pins at 0 V			15	pF

† All typical values are at T_A = 25°C and nominal voltage.

‡ θJ_A = 78°C, θJ_C = 34°C.

4.4 TIMING CHARACTERISTICS AND REQUIREMENTS

Timing characteristics and requirements are given in Section 4.4.1 through Section 4.4.6; relevant timing diagrams are shown in Figure 4-1 through Figure 4-9.

4.4.1 *Clock and Host Interface Timing Requirements Over Full Range of Operating Conditions*

	PARAMETER	MIN	TYP	MAX	UNIT
$t_{c(\phi)}$	Clock cycle time	200		2000	ns
$t_{w(\phi H)}$	Clock high pulse width	100		1955	ns
$t_{w(\phi L)}$	Clock low pulse width	45			ns
$t_{su(AD)}$	Address setup time	0			ns
$t_{su(DBIN)}$	DBIN setup time	0			ns
$t_{su(CE)}$	$\overline{CE}$ setup time	100			ns
$t_{su(WE)}$	$\overline{WE}$ setup time	0			ns
$t_{w(WE)}$	$\overline{WE}$ low pulse width	80			ns
$t_{su(DA)}$	Data setup time	60			ns
$t_{h(DA)}$	Data hold time	0			ns
$t_{h(AD)}$	Address hold time	0			ns
$t_{h(DBIN)}$	DBIN hold time	0			ns
$t_{h(CE)}$	$\overline{CE}$ hold time	80			ns
$t_{su(GR)}$	$\overline{ACCGR}$ setup time	100			ns
$t_{h(GR)}$	$\overline{ACCGR}$ hold time	80			ns

4.4.2 Host Interface Timing Characteristics Over Full Range of Operating Conditions

	PARAMETER	MIN	TYP	MAX	UNIT
$t_{a(CE)}$	Access time from $\overline{CE}$			150	ns
$t_{a(DBIN)}$	Access time from DBIN			150	ns
$t_{su(AD)}$	Address setup time to $\overline{CE}$	0			ns
$t_{z(DBIN)}$	Hi-Z time from DBIN		50	100	ns
$t_{z(CE)}$	Hi-Z time from $\overline{CE}$		50	100	ns
$t_{a(GR)}$	Access time from $\overline{ACCGR}$			150	ns
$t_{z(GR)}$	Hi-Z time from $\overline{ACCGR}$		50	100	ns
$t_{d(GR-RQ)}$	Delay of $\overline{ACCRQ}$ high from $\overline{ACCGR}$			100	ns

4.4.3 Source Handshake Timing Characteristics Over Full Range of Operating Conditions (see Note 1)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{d1}	Delay of DAV true from end of write operation to data out register	Normal T_1 (see Note 2)	12(ø)†	12(ø)† + 310	ns
		Short T_1 (see Note 2)	8(ø)†	8(ø)† + 310	ns
		Very short T_1 (see Note 2)	4(ø)†	4(ø)† + 310	ns
t_{d2}	Delay of valid GPIB data lines from end of write cycle			140	ns
t_{d3}	Delay of BO interrupt from DAC true	BO interrupt unmasked		300	ns
t_{d4}	Delay of $\overline{ACCRQ}$ DAC true			300	ns
t_{d5}	Delay of DAV false from DAC true			160	ns

NOTES. 1. The timing of the source handshake is the same whether ATN is true or false (i.e., whether the device is in TACS, CACS, or SPAS).

2. A very short bus settling time (T_1) occurs on the second and subsequent data byte sent when ATN is false if the 'vstd1' feature is set. A slightly longer bus settling time takes place if 'std1' is set unless there is a very short bus settling time. In all other instances, a normal bus settling time occurs.

4.4.4 Acceptor Handshake Timing Characteristics Over Full Range of Operating Conditions

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{d6}	Delay of BI interrupt from DAV true	BI interrupt unmarked ATN = false device is in LACS	2(ϕ)1	2(ϕ)1 + 415	ns
t_{d7}	Delay of $\overline{\text{ACCRQ}}$ from DAV true	ATN = false device is in LACS	2(ϕ)1	2(ϕ)1 + 290	ns
t_{d8}	Delay of NDAC false from DAV true	ATN = false device is in LACS	3(ϕ)1	3(ϕ)1 + 445	ns
t_{d9}	Delay of NRFD false from end of read operation of Data In register	ATN = false device is in LACS		220	ns
t_{d10}	Delay of interface message interrupt from DAV true (see Note 3)	ATN = true device not in CACS all interface message interrupts (except UNO)	2(ϕ)1	2(ϕ)1 + 415	ns
		UNO interrupt only	5(ϕ)1	5(ϕ)1 + 415	ns
t_{d11}	Delay of NDAC false from DAV true	ATN = true device not in CACS no DAC holdoff	7(ϕ)1	7(ϕ)1 + 415	ns
t_{d12}	Delay of NDAC false from end of write operation			230	ns
t_{d13}	Delay of NRFD false from DAV false	ATN = true device not in CACS		180	ns

NOTE 3 The interrupts generated by interface messages are shown in Table 4-1.

4.4.5 ATN, EOI, and IFC Timing Characteristics Over Full Range of Operating Conditions

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{d14}	Delay of NDAC true from ATN true	Device is not in CACS		195	ns
t_{d15}	Delay of TE high from EOI true	Device is not in CACS		125	ns
t_{d16}	Delay of valid data from EOI true	Device is not in CACS		140	ns
t_{d17}	Delay of TE low from EOI false	Device is not in CACS		125	ns
t_{d18}	Delay of NRFD true from ATN false	Device is in LADS/LACS		140	ns
t_{d19}	Response time to IFC		$16t_{C(\phi)}$	$30t_{C(\phi)}$	ns

4.4.6 Controller Timing Characteristics Over Full Range of Operating Conditions

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{d20}	Delay of ATN true from end of t_{ca} *aux command*		$8t_{c(\phi)}$	$10(\phi)1+220$	ns
t_{d21}	Delay of BO interrupt from end of t_{ca} *aux command*		$18t_{c(\phi)}$	$22(\phi)1+415$	ns
t_{d22}	Delay of ATN true from end of t_{cs} *aux command*	BO *unmasked* device is in ANRS	$8t_{c(\phi)}$	$10(\phi)1+220$	ns
t_{d23}	Delay of BO interrupt from end of t_{cs} *aux command*	BO *unmasked* device is in ANRS	$18t_{c(\phi)}$	$22(\phi)1+415$	ns
t_{d24}	Delay of EOI true from r_{pp} aux command set			230	ns
t_{d25}	Delay of EOI false from r_{pp} aux command cleared			230	ns
t_{d26}	Delay of EOI from r_{pp} aux command cleared	BO unmasked	$8t_{c(\phi)}$	$10(\phi)1+415$	ns
t_{d27}	Delay of ATN false from sts aux command	Device is not in SDYS or STRS		210	ns

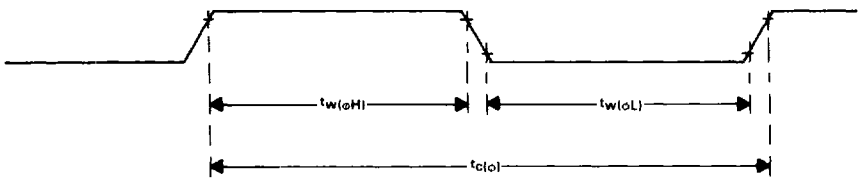


FIGURE 4-1 – TMS9914A CLOCK CYCLE TIMING

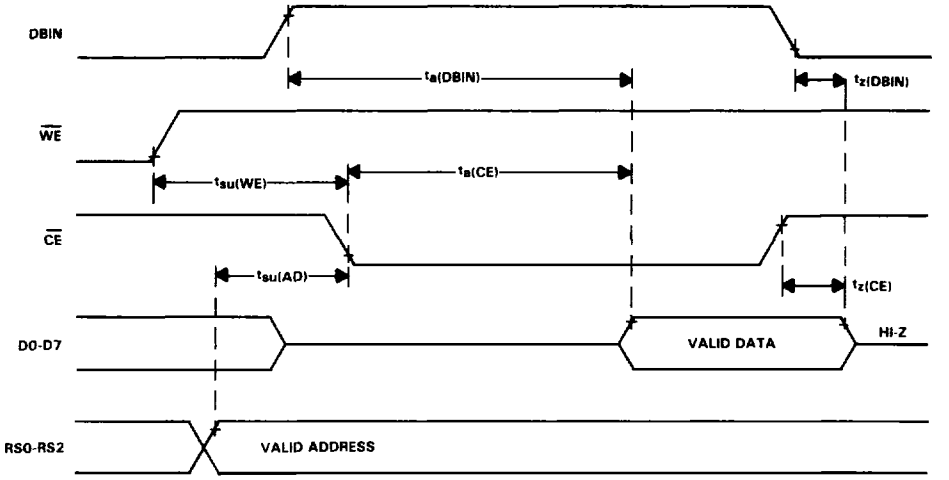
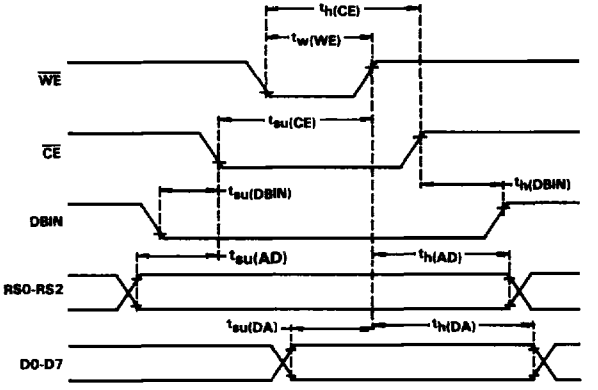
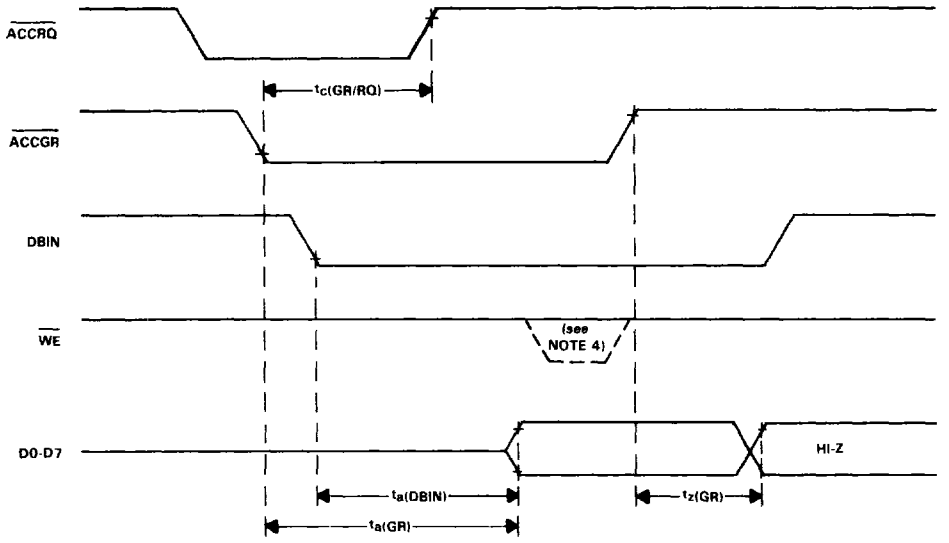


FIGURE 4-2 – TMS9914A READ CYCLE TIMING



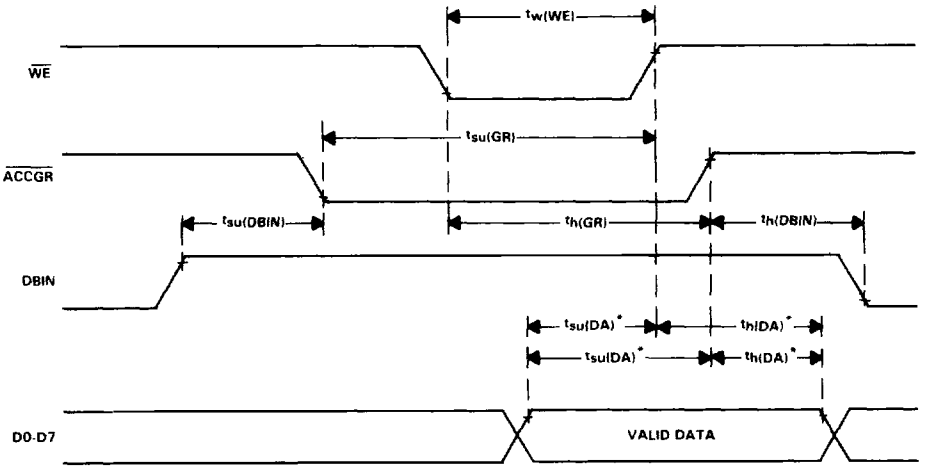
NOTE: $t_{h(AD)}$ and $t_{h(DA)}$ are shown measured from the rising edge of $\overline{WE}$. This is the correct reference point in this figure, since the measurement should be from the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever comes first.

FIGURE 4-3 – TMS9914A WRITE CYCLE TIMING



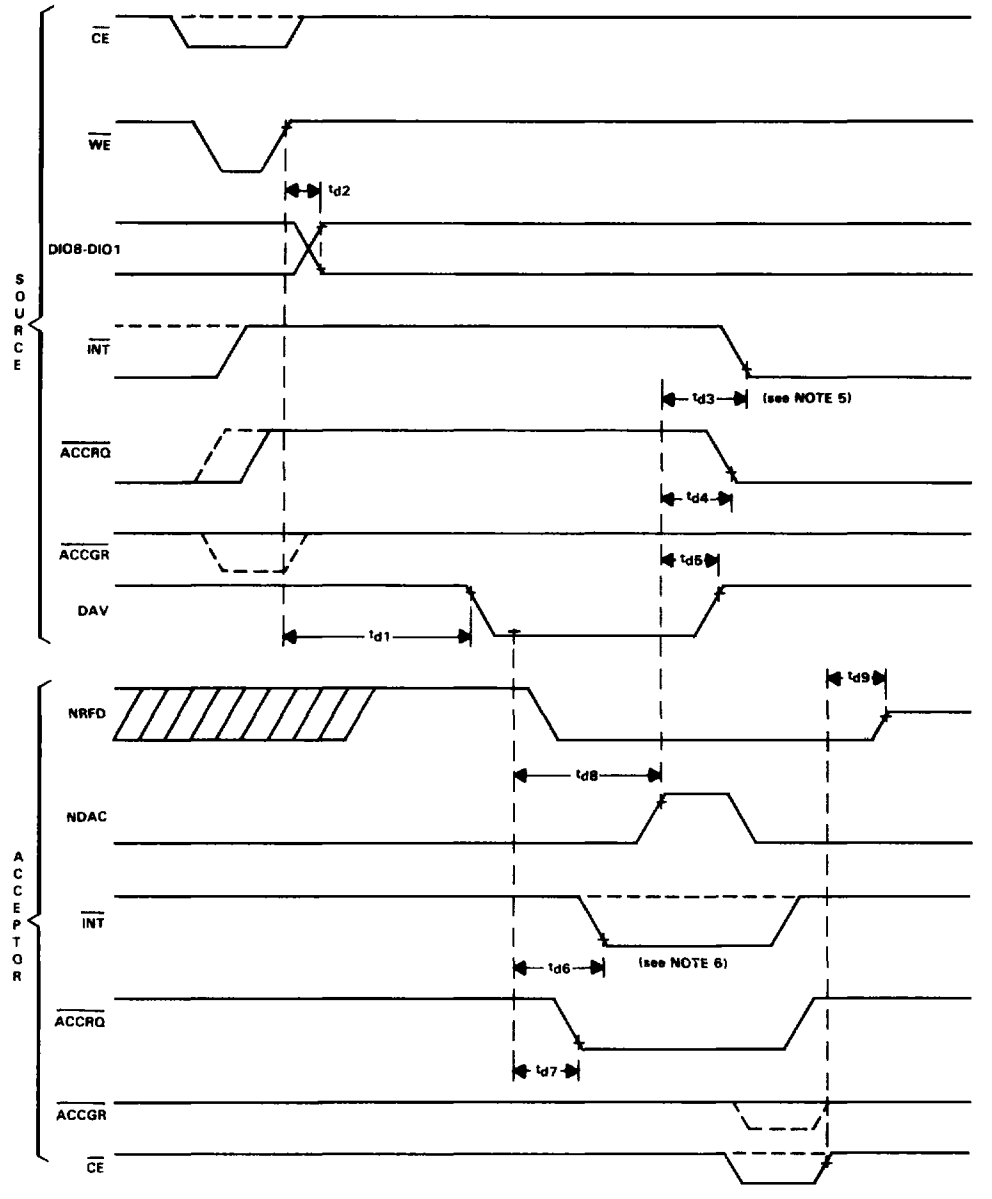
NOTE 4: A write enable pulse may occur in a DMA read operation. A write enable pulse may therefore be provided for system memory and need not be suppressed at the TMS9914A.

FIGURE 4-4 – TMS9914A DMA READ OPERATION



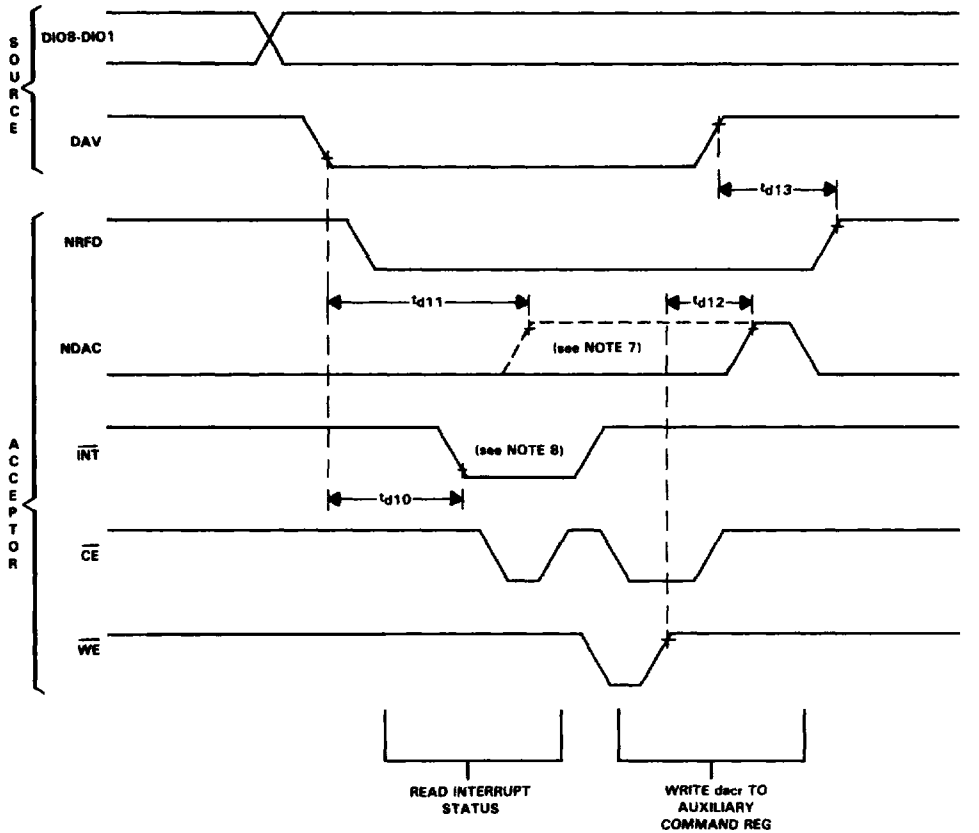
* $t_{su(DA)}$ and $t_{h(DA)}$ are only applicable to the first signal to become inactive whether it is $\overline{WE}$ or $\overline{ACCGR}$.

FIGURE 4-5 – TMS9914A DMA WRITE OPERATION



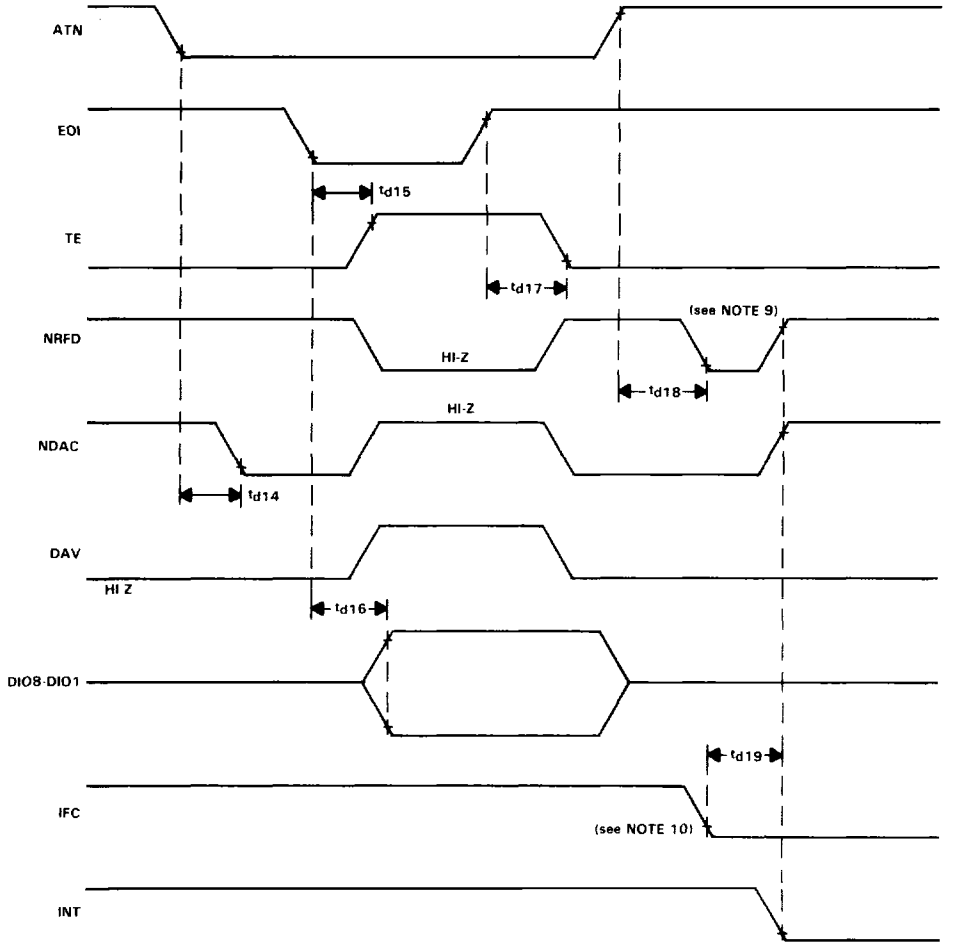
NOTES: 5. The interrupt line is taken low by a BO interrupt.
6. The interrupt line is taken low by a BI interrupt.

FIGURE 4-6 – TMS9914A SOURCE AND ACCEPTOR HANDSHAKE TIMING(S)



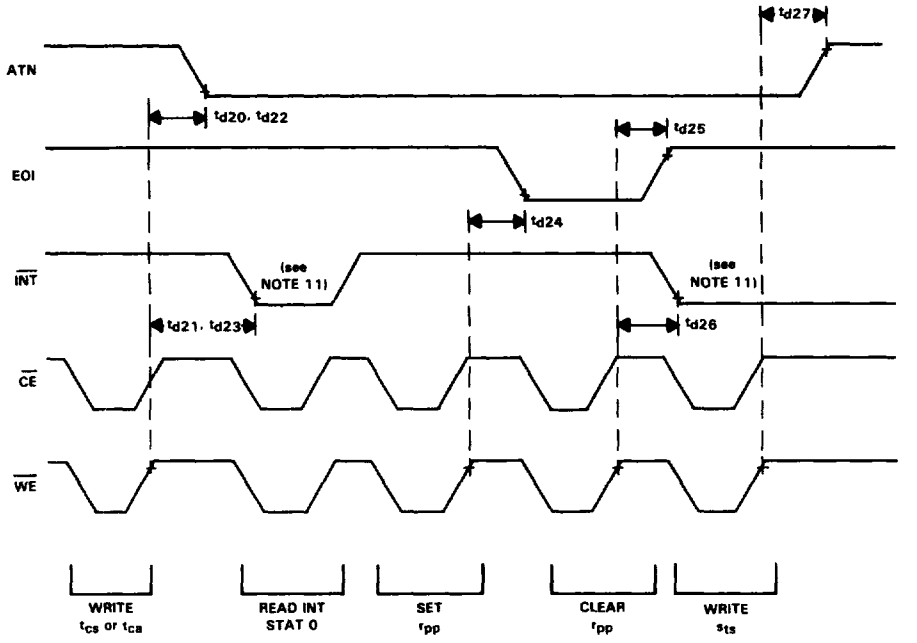
NOTES: 7. The broken line shows the waveform if there is no DAC holdoff. The solid lines assume there is a DAC holdoff.
8. The interrupts generated by interface messages are shown in Table 3-15.

FIGURE 4-7 – TMS9914A ACCEPTOR HANDSHAKE TIMING "ATN" TRUE



NOTES: 9. This assumes that an RFD holdoff occurs
10. IFC causes the TMS9918A to be unaddressed and an IFC interrupt occurs.

FIGURE 4-8 – TMS9914A RESPONSE TO 'ATN' AND 'EOI'



NOTE 11: A BO interrupt occurs as the TMS9914A enters CACS.

FIGURE 4-9 – TMS9914A CONTROLLER TIMING