MC-421000C8
1,048,576 x 8-BIT
CMOS DYNAMIC RAM MODULE

PRELIMINARY INFORMATION

Description

The MC-421000C8 is a static-column, 1,048,576-word by 8-bit dynamic RAM module designed to operate from a single +5-volt power supply. Advanced CMOS circuitry, including a single-transistor storage cell, 2048 sense amplifiers per data output, multiplexed address buffers and flexible refresh controls, provides good system operating margins.

The MC-421000C8 is functionally equivalent to eight μPD421002 standard 1M DRAMs. Refreshing is accomplished by means of $\overline{RAS}$-only refresh cycles, hidden refresh cycles, $\overline{CS}$ before $\overline{RAS}$ refresh cycles, or by normal read or write cycles on the 512 address combinations of A_0-A_8 during an 8-ms period.

Packaged in a Single Inline Memory Module (SIMM™) to enhance reliability and reduce the size, weight and cost of a system, the MC-421000C8 includes eight μPD421002s in SOJ packages and eight power supply decoupling capacitors.

SIMM is a trademark of Wang Laboratories.

Features

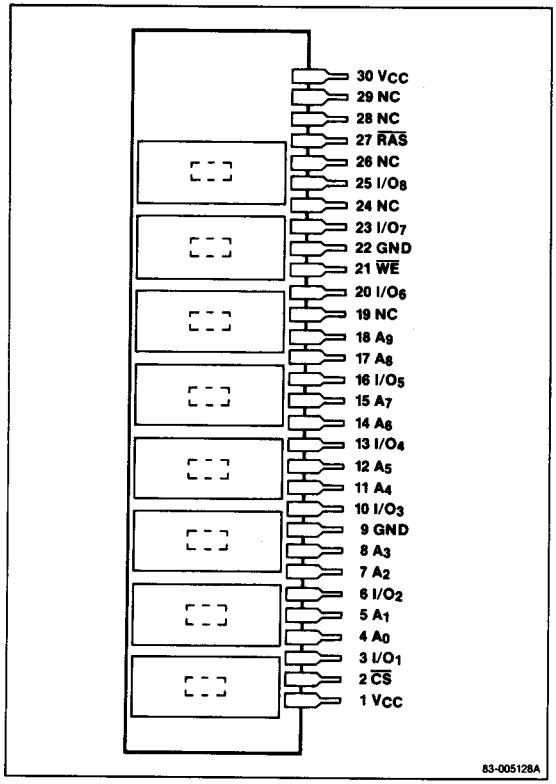
- ☐ 1,048,576-word by 8-bit organization
- ☐ Single +5-volt ± 10% power supply
- ☐ Standard 30-pin Single Inline Memory Module (SIMM)
- ☐ Eight 1M dynamic RAMs incorporated in high-density SOJ packaging (μPD421002LA)
- ☐ Eight power supply decoupling capacitors
- ☐ Low power dissipation: 44 mW standby (max)
- ☐ TTL-compatible inputs and outputs
- ☐ 512 refresh cycles (A_0-A_8 are refresh address pins)
- ☐ Static-column capability

Ordering Information

Part Number	Row Access Time (max)	Column Access Time (max)	Address Access Time (max)	Package
MC-421000C8A-80	80 ns	20 ns	45 ns	30-pin leaded SIMM
A-10	100 ns	25 ns	55 ns	
A-12	120 ns	30 ns	65 ns	
MC-421000C8B-80	80 ns	20 ns	45 ns	30-pin socket-able SIMM
B-10	100 ns	25 ns	55 ns	
B-12	120 ns	30 ns	65 ns	

Pin Configurations

30-Pin SIMM, MC-421000C8A



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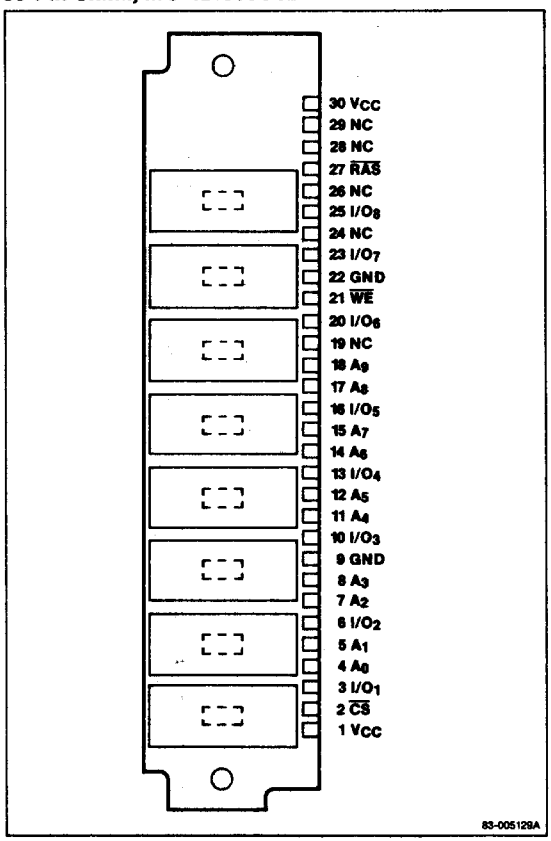
Pin Configurations (cont)

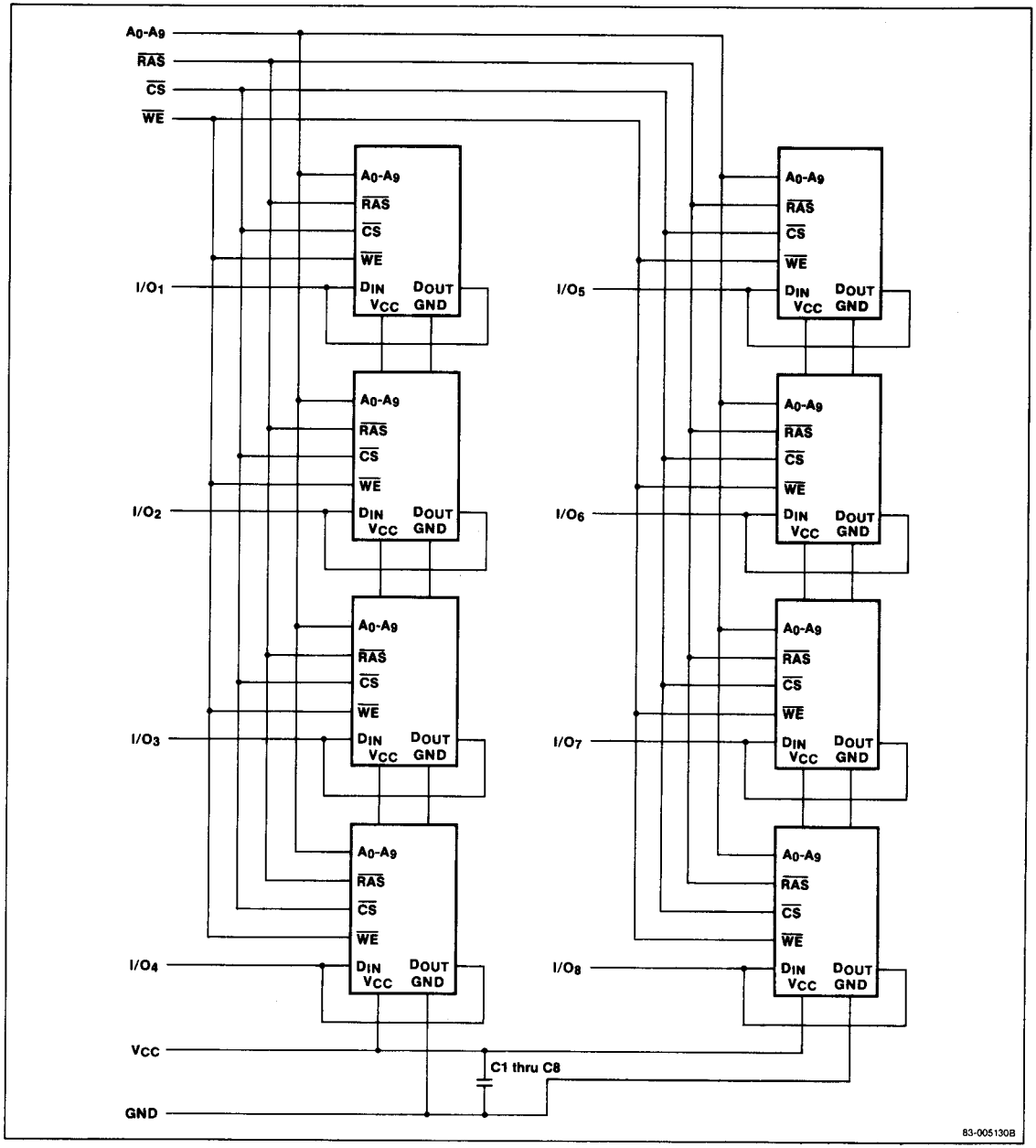
30-Pin SIMM, MC-421000C8B



Pin Identification

Symbol	Function
A_0-A_9	Address inputs
I/O_1-I/O_8	Common data inputs/outputs
$\overline{RAS}$	Row address strobe
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Block Diagram



Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	8.0 W

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

$T_A = 25°C$; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	60	pF	A_0-A_9, $\overline{RAS}$, $\overline{CS}$, $\overline{WE}$
Input/output capacitance	C_D	15	pF	I/O_1-I/O_8

DC Characteristics

$T_A = 0$ to +70°C; $V_{CC} = 5.0$ V ±10%; GND = 0 V

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V	
Input voltage, low	V_{IL}	−1.0		0.8	V	
Standby current	I_{CC2}			16	mA	$\overline{RAS} = \overline{CS} \geq V_{IH}$ (min)
				8	mA	$\overline{RAS} = \overline{CS} \geq V_{CC} - 0.2$ V
Input leakage current	I_{IL}	−80		80	μA	For A_0-A_9, $\overline{RAS}$, $\overline{CS}$, $\overline{WE}$: $V_{IN} = 0$ to V_{CC}; other pins = 0 V
Output leakage current	I_{OL}	−10		10	μA	For I/O_1-I/O_8: D_{OUT} disabled; $V_{OUT} = 0$ to V_{CC}
Output voltage, low	V_{OL}	0		0.4	V	$I_{OUT} = 4.2$ mA
Output voltage, high	V_{OH}	2.4		V_{CC}	V	$I_{OUT} = -5$ mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

		Limits							
		MC-421000C8-80		MC-421000C8-10		MC-421000C8-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		560		480		400	mA	$\overline{RAS}$, $\overline{CS}$ cycling; $t_{RC} = t_{RC}$ min (Note 5)
Operating current, refresh cycle, average	I_{CC3}		560		480		400	mA	$\overline{RAS}$ cycling; $\overline{CS} \geq V_{IH}$; $t_{RC} = t_{RC}$ min; I_O = 0 mA (Note 5)
Operating current, $\overline{CS}$ before $\overline{RAS}$ refreshing, average	I_{CC5}		560		480		400	mA	$t_{RC} = t_{RC}$ min; I_O = 0 mA (Note 5)
Random read or write cycle time	t_{RC}	160		190		220		ns	(Note 6)
Refresh period	t_{REF}		8		8		8	ms	Addresses A_0-A_8
Access time from $\overline{RAS}$	t_{RAC}		80		100		120	ns	(Notes 7, 8)
Access time from $\overline{CS}$	t_{CAC}		20		25		30	ns	(Notes 7, 9, 10)
Access time from column address	t_{AA}		45		50		60	ns	(Notes 7, 10)
Output buffer turnoff delay	t_{OFF}	0	20	0	25	0	30	ns	(Note 11)
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	(Note 4)
$\overline{RAS}$ precharge time	t_{RP}	70		80		90		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		30		ns	
$\overline{CS}$ pulse width	t_{CS}	20	100000	25	100000	30	100000	ns	
$\overline{CS}$ hold time	t_{CSH}	80		100		120		ns	
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	25	60	25	75	25	90	ns	(Note 12)
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 13)
$\overline{CS}$ precharge time	t_{CP}	10		10		15		ns	
$\overline{RAS}$ precharge $\overline{CS}$ hold time	t_{RPC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	12		12		15		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	17	35	17	50	20	60	ns	(Note 10)
Column address setup time	t_{ASC}	0	20	0	20	0	25	ns	
Column address hold time	t_{CAH}	20		20		25		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	80		100		120		ns	

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AC Characteristics (cont)

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

Parameter	Symbol	Limits						Unit	Test Conditions
		MC-421000C8-80		MC-421000C8-10		MC-421000C8-12			
		Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ to column address hold time	t_{AH}	15		15		15		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	45		50		60		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		ns	(Note 14)
Read command hold time referenced to $\overline{CS}$	t_{RCH}	0		0		0		ns	(Note 14)
Column address hold time referenced to $\overline{RAS}$ (write cycle)	t_{AWR}	60		70		85		ns	
Write command hold time	t_{WCH}	15		20		25		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	55		70		85		ns	
Write command pulse width	t_{WP}	15		20		25		ns	(Note 15)
Write command to $\overline{RAS}$ lead time	t_{RWL}	25		30		35		ns	
Write command to $\overline{CS}$ lead time	t_{CWL}	15		20		25		ns	
Data-in setup time	t_{DS}	0		0		0		ns	(Note 16)
Data-in hold time	t_{DH}	20		20		25		ns	(Note 16)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	60		70		85		ns	
Write command setup time	t_{WCS}	0		0		0		ns	
$\overline{CS}$ setup time for $\overline{CS}$ before $\overline{RAS}$ refreshing	t_{CSR}	10		10		10		ns	(Note 17)
$\overline{CS}$ hold time for $\overline{CS}$ before $\overline{RAS}$ refreshing	t_{CHR}	15		20		25		ns	(Note 17)
Static-Column Operation									
Static-column operating current, average	I_{CC4}		480		400		320	mA	$\overline{RAS}$ = $\overline{CS}$ = V_{IL}; addresses cycling; t_{RSC} = t_{RSC} min or t_{WSC} = t_{WSC} min (Note 5)
Static-column read cycle time	t_{RSC}	50		60		70		ns	(Note 6)
Static-column write cycle time	t_{WSC}	50		60		70		ns	(Note 6)
Static-column $\overline{RAS}$ pulse width	t_{RASC}	80	100000	100	100000	120	100000	ns	

AC Characteristics (cont)

$T_A = 0$ to $+70°C$; $V_{CC} = 5.0\ V \pm 10\%$

Parameter	Symbol	Limits MC-421000C8-60 Min	Max	MC-421000C8-10 Min	Max	MC-421000C8-12 Min	Max	Unit	Test Conditions
Static-Column Operation (cont)									
$\overline{RAS}$ to second $\overline{WE}$ delay	t_{RSW}	95		115		135		ns	
Write invalid time	t_{WI}	10		10		10		ns	
Output hold time from address	t_{OH}	5		5		5		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles before proper device operation is achieved.

(3) Ac measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured by assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range ($T_A = 0$ to $+70°C$) is assured.

(7) Load = 2 TTL (−1 mA, +4 mA) loads and 100 pF ($V_{OH} = 2.0$ V, $V_{OL} = 0.8$ V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).

(10) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(11) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(12) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

(13) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CS}$ cycles that are preceded by any cycle.

(14) Specifications for either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

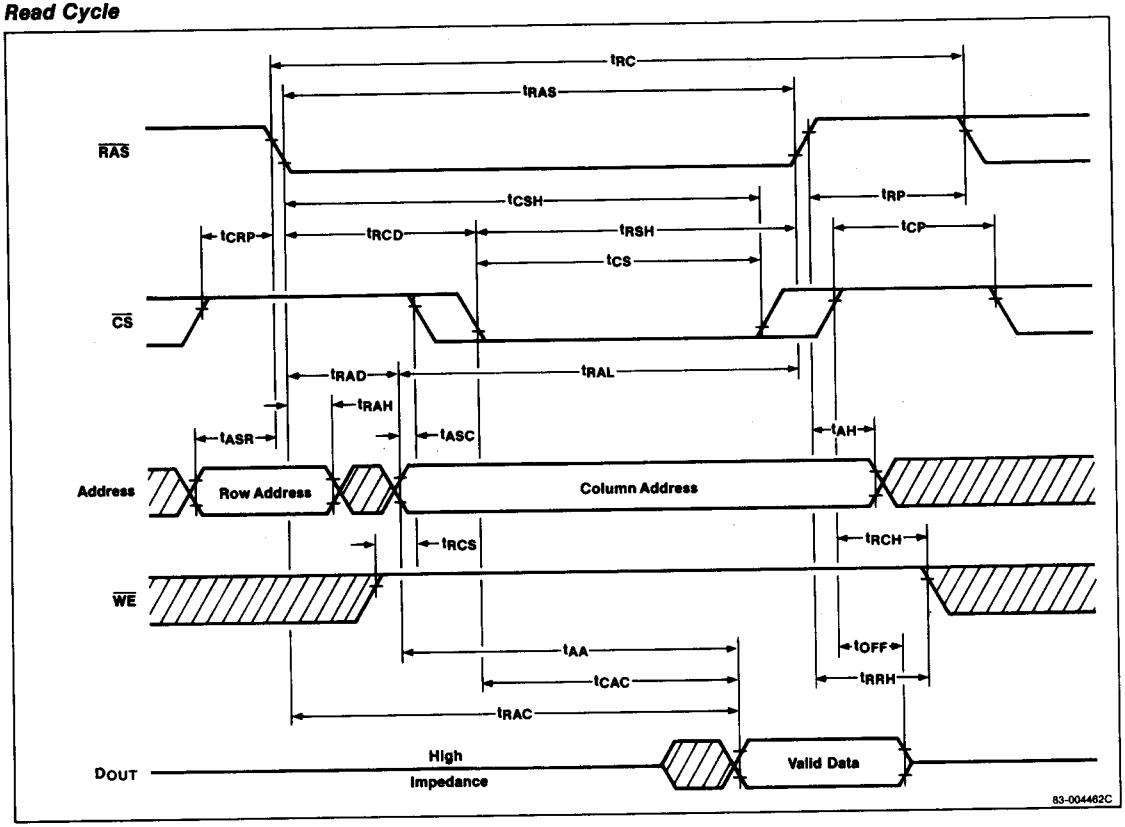
(15) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, specifications for both t_{WCS} and t_{WCH} must be met.

(16) These parameters are referenced to the falling edge of $\overline{CS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(17) $\overline{CS}$ before $\overline{RAS}$ operation is specified.

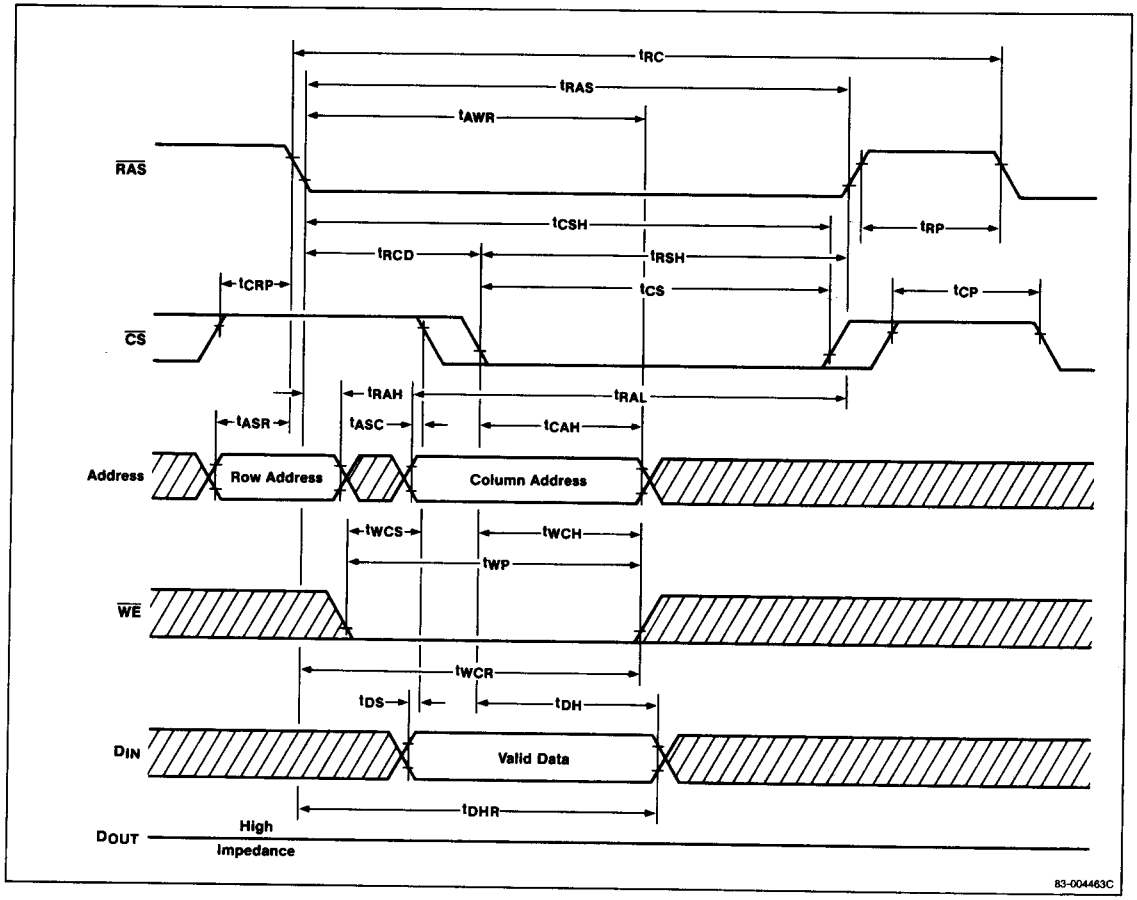
Timing Waveforms

Read Cycle



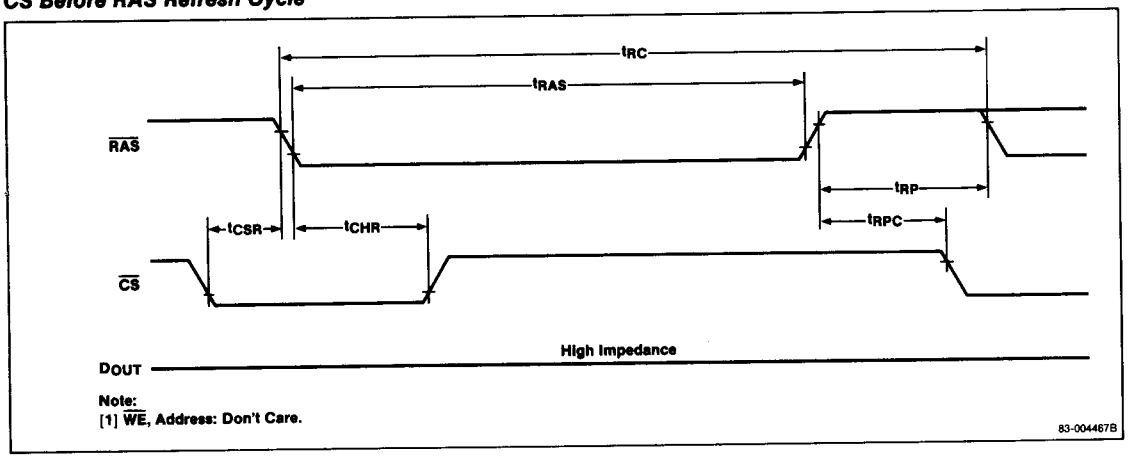
Timing Waveforms (cont)

Write Cycle (Early Write)



Timing Waveforms (cont)

$\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle



Note:
[1] $\overline{WE}$, Address: Don't Care.

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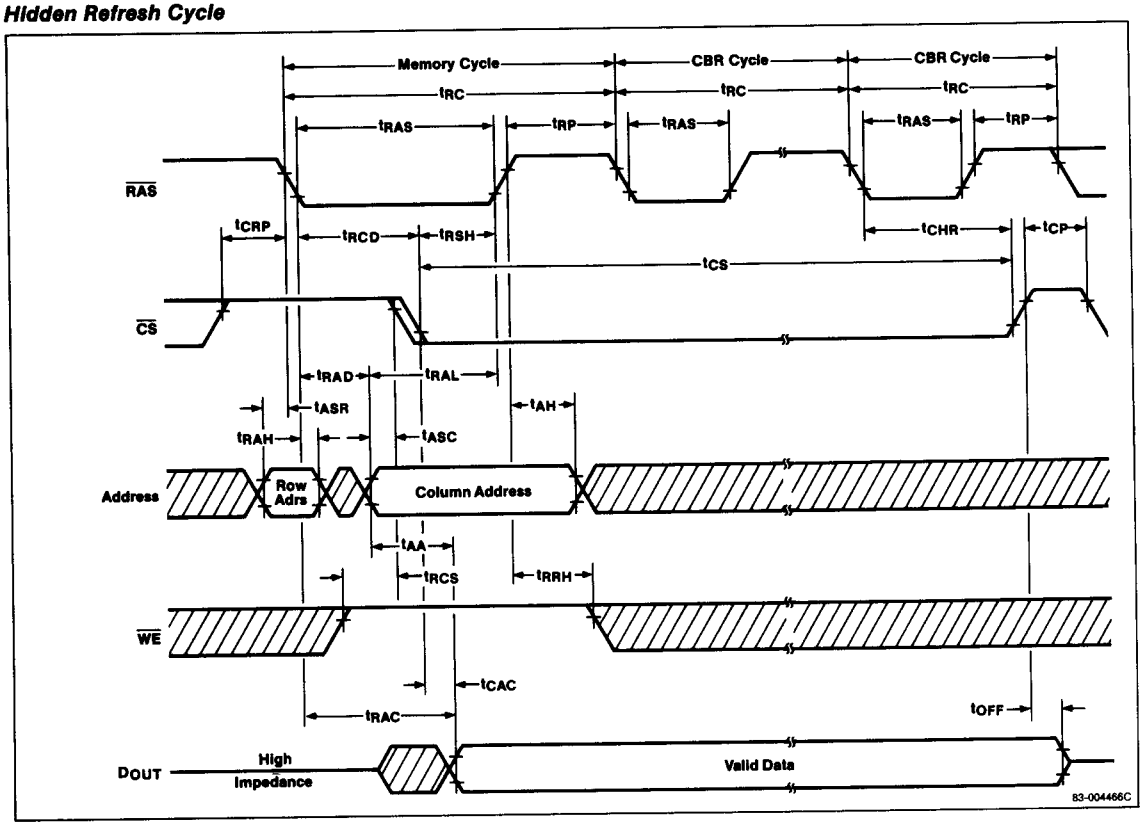
Hidden Refresh Cycle



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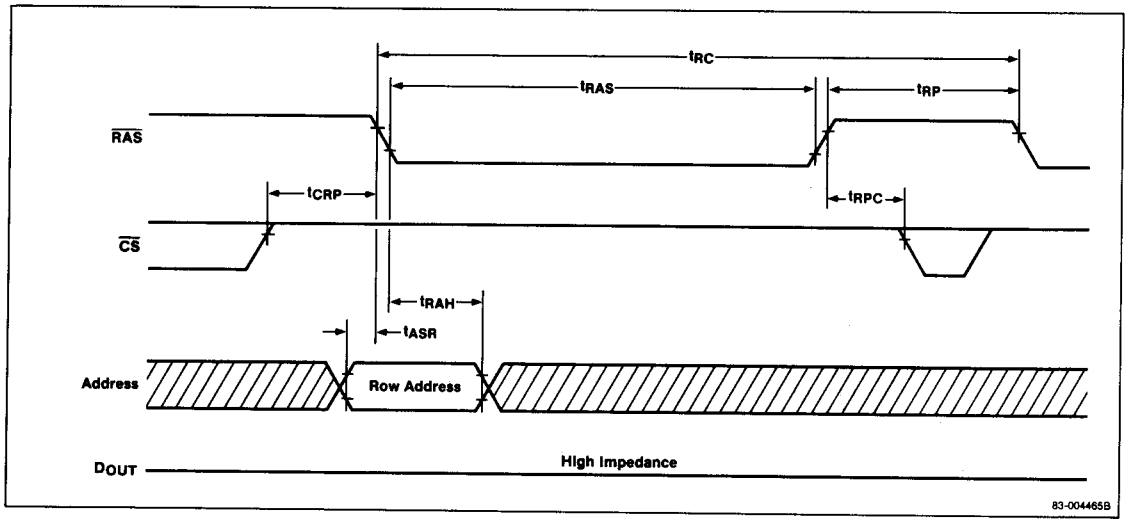
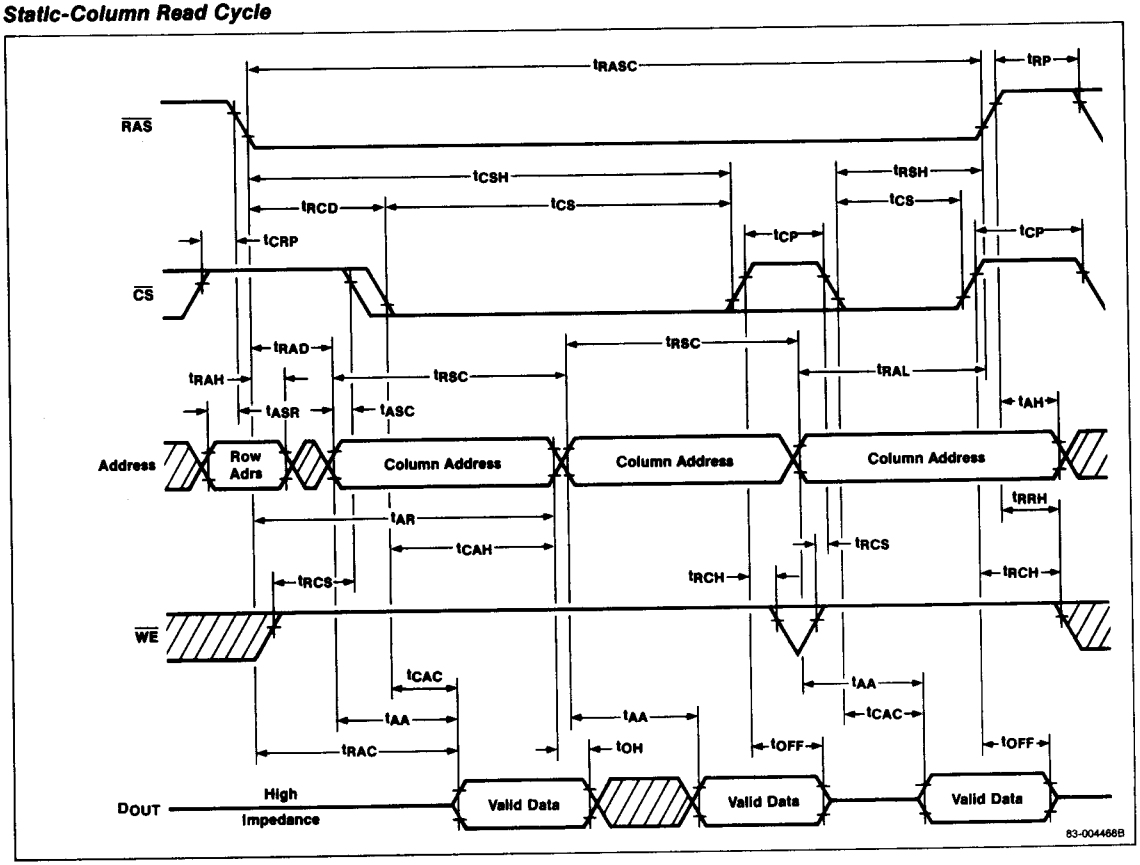
Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



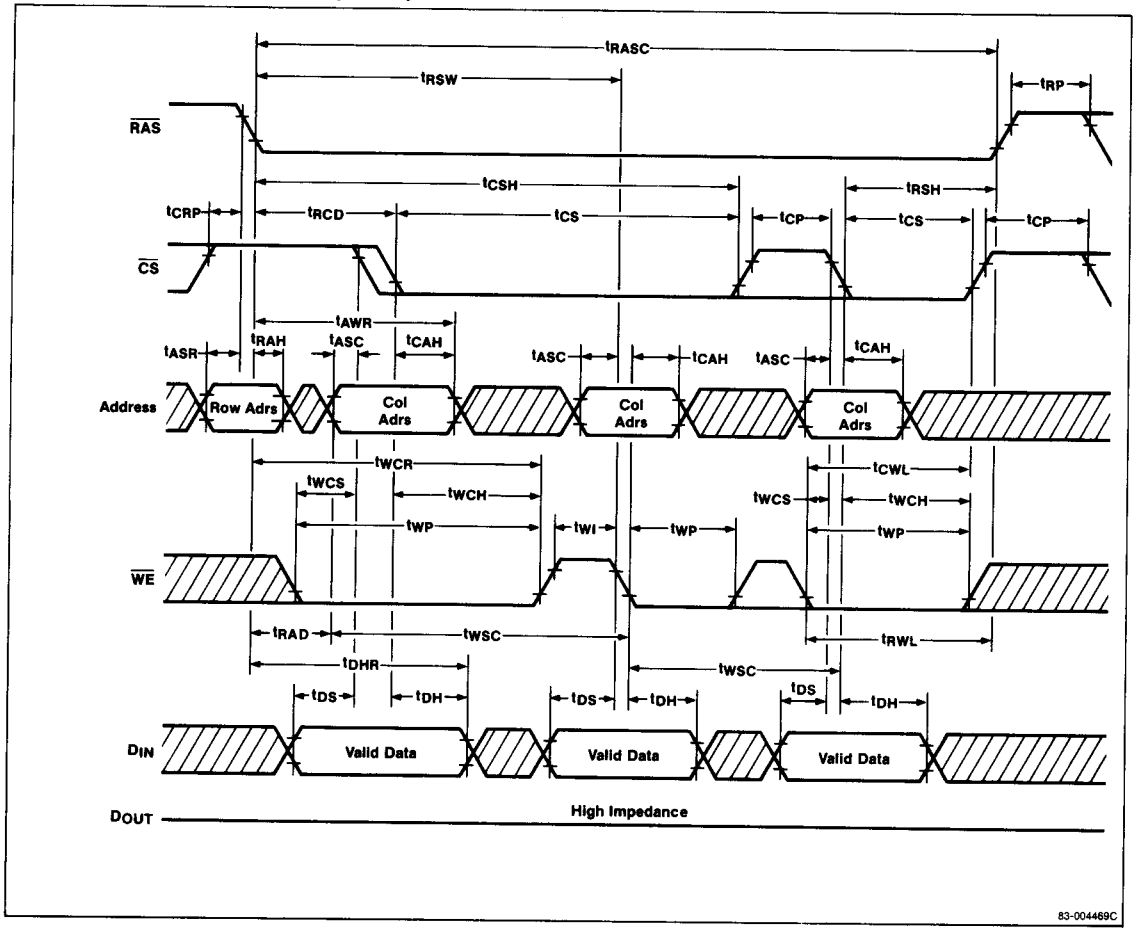
Timing Waveforms (cont)

Static-Column Read Cycle



Timing Waveforms (cont)

Static-Column Write Cycle (Early Write)



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