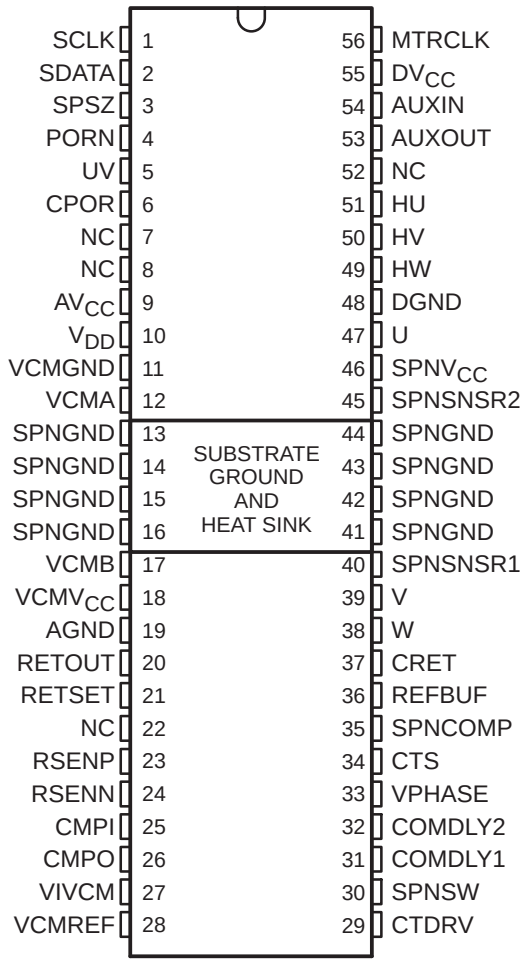
- **Single-Chip Voice-Coil Motor Driver and Spindle-Motor Driver**
- **Precision Dual-Voltage Monitor**
- **Operates From Single 5-V Supply**
- **LinBiCMOS™ Technology**
- **Low Power Dissipation**
- **Internal Overtemperature Shutdown Circuitry**
- **Low-Profile 56-Terminal DL Package and 64-Terminal PM Package Available**
- **4-V Reference Buffer**
- **System Power-On Reset**
- **Monotonic 8-Bit DAC**

DL PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TLS2205 is a combination voice-coil and spindle-motor driver with voltage monitor integrated circuit. This circuit is designed for small-form-factor, high-performance hard disk drives. The TLS2205 integrates a three-phase brushless dc motor driver with a linear full-bridge voice-coil driver. Additional circuitry is added for power-up and power-down sequencing of the driver amplifiers used for motor speed control. A brake function can be invoked on the spindle motor after the head is in a safe landing zone. External sense resistors are used for precision spindle motor and VCM current monitoring. Automatic head retract is provided for voltage or thermal fault conditions. The TLS2205 operates with only 5 V of supply voltage and has a sleep-mode option for low-power applications. All device functions are controlled from a three-wire serial port. Device packaging is a 56-terminal DL or 64-terminal PM package. Center pins are tied to the die mount tab for improved heat dissipation on both packages.

Voice-Coil Motor Driver

- **±0.4-A MOS H-Bridge Power Amplifier**
- **No Crossover Distortion**
- **Precision VCM Control Loop With External Sense Resistor**
- **Internal 8-Bit Control DAC With Four Gain Ranges**
- **Controlled-Velocity Head Retract**
- **Compensation Adjust Terminals for Bandwidth Control**
- **Capability for External Velocity Feedback**
- **Low $r_{DS(on)}$, 2 Ω Total**
- **No External Retract Power Supply Isolation Components Required**

Spindle-Motor Driver

- **Hall- or Back-EMF Commutation Circuitry**
- **3-Phase Driver With 1.3-A MOS Output**
- **Bipolar or Unipolar Drive Modes**
- **Programmable Frequency-Locked Speed Control Loop**
- **Programmable Start-Up Current**
- **Linear Spindle Current Control**
- **Low $r_{DS(on)}$, 1.3 Ω Total**
- **Sector Data Tachometer Signal Input (Optional)**
- **Speed Sense Tachometer Output**
- **Internal Schottky Diodes for Retract Power Source**
- **Controlled Brake Function**

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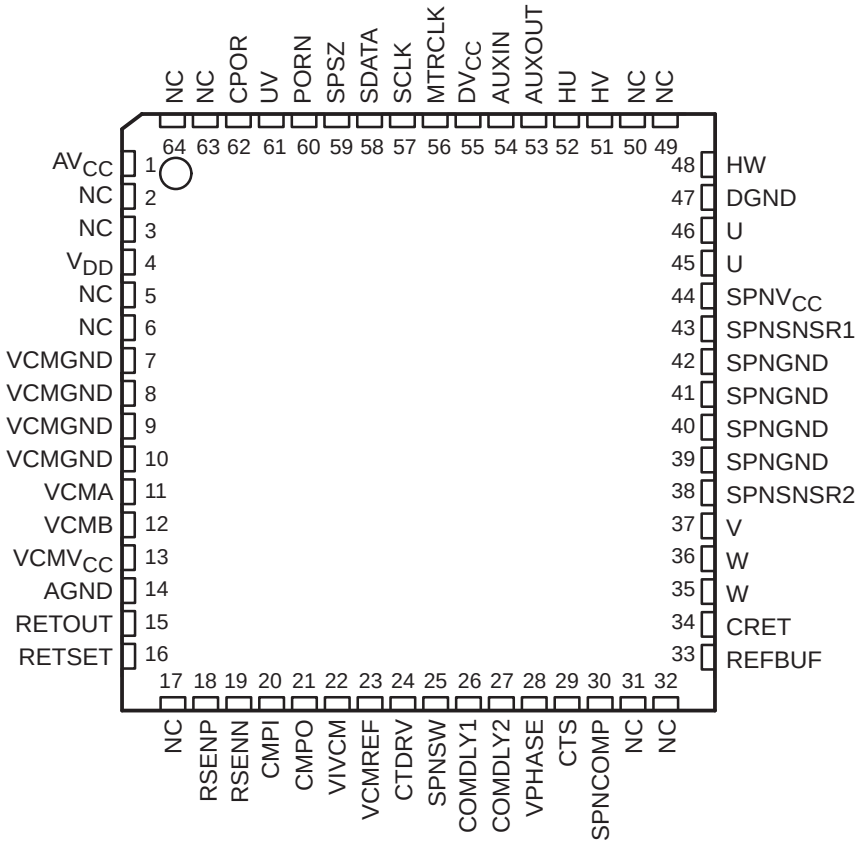
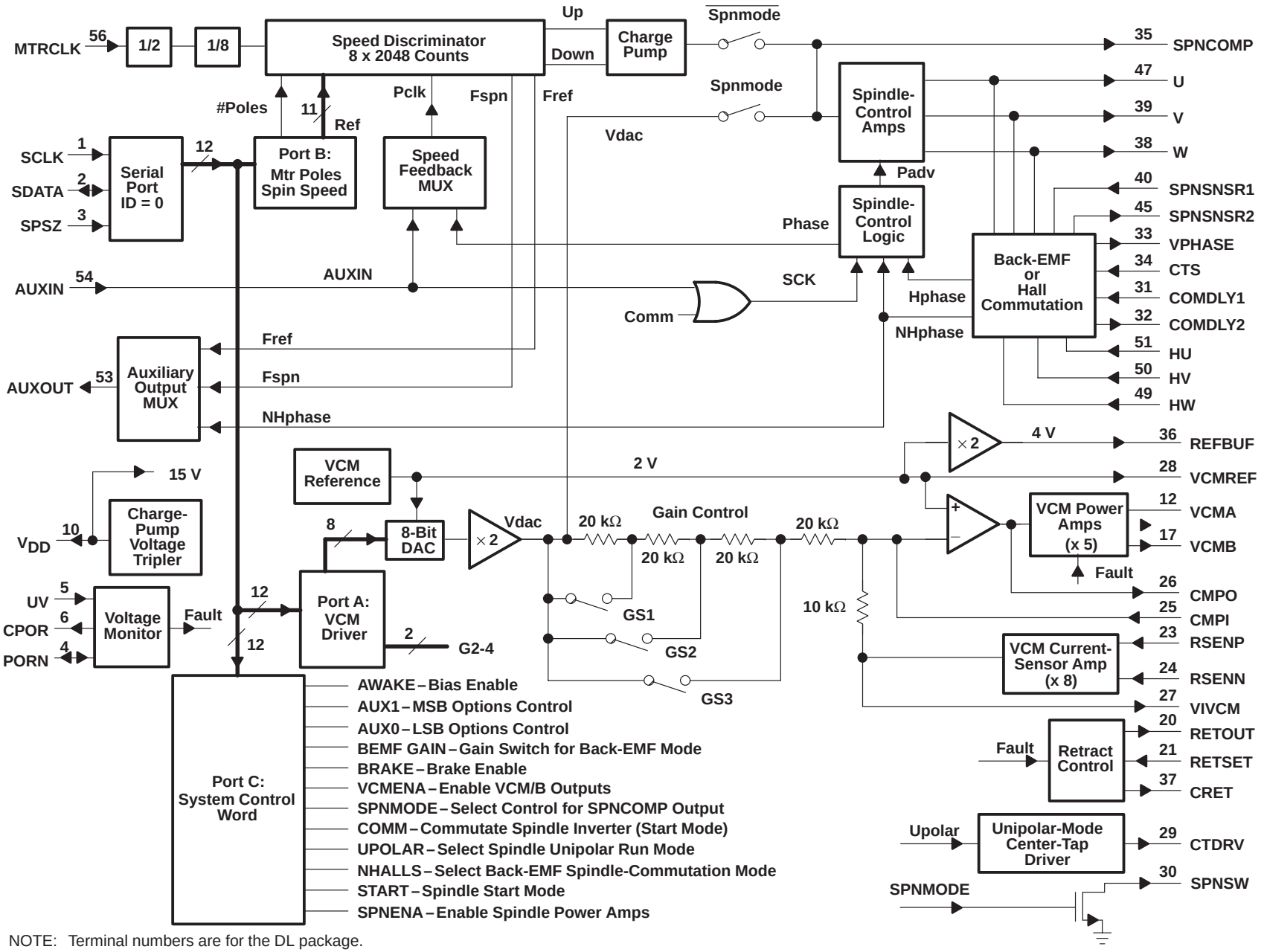
PM PACKAGE
(TOP VIEW)



NC – No internal connection

functional block diagram



NOTE: Terminal numbers are for the DL package.

Terminal Functions

NAME	TERMINAL NO.†	TERMINAL NO.‡	I/O	DESCRIPTION	SUBSYSTEM§
AGND	19	14		Analog GND	VM
AUXIN	54	54	I	Spindle-phase commutate input	SPN
AUXOUT	53	53	O	Spindle-system status output	SPN
AV_{CC}	9	1	I	Analog 5-V supply voltage	VM
CMPI	25	20	I	VCM frequency-compensation input	VCM
CMPO	26	21	O	VCM frequency-compensation output	VCM
COMDLY1	31	26	I	Spindle back-EMF commutation delay control input	SPN
COMDLY2	32	27	O	Spindle back-EMF commutation delay control output	SPN
CPOR	6	62	O	Power-on-reset delay capacitor output	VM
CRET	37	34	O	Retract power full-wave-rectifier output	VM
CTDRV	29	24	O	Center-tap pnp drive output	SPN
CTS	34	29	I	Spindle center-tap sense input	SPN
DGND	48	47		Logic GND	SP
DV_{CC}	55	55	I	Logic power supply voltage	SP
HU	51	52	I	Hall-phase U input	SPN
HV	50	51	I	Hall-phase V input	SPN
HW	49	48	I	Hall-phase W input	SPN
MTRCLK	56	56	I	Spindle-motor reference clock input	SPN
PORN	4	60	I/O	Power-on-reset node, open-drain output/reset input	VM
REFBUF	36	33	O	4-V reference	VCM
RETOUT	20	15	O	Retract voltage set output	VM
RETSET	21	16	I	Retract voltage set input	VM
RSENN	24	19	I	VCM current-sense negative input	VCM
RSENP	23	18	I	VCM current-sense positive input	VCM
SCLK	1	57	I	Serial input clock	SP
SDATA	2	58	I/O	Serial input/output port	SP
SPNCOMP	35	30	O	Spindle charge-pump filter	SPN
SPNGND	13, 14, 15, 16, 41, 42, 43, 44	39, 40, 41, 42		Spindle ground	SPN
SPNSNSR1	40	43	I	Spindle-sense-resistor kelvin input	SPN
SPNSNSR2	45	38	O	Spindle-sense-resistor output	SPN
SPNSW	30	25	O	Spindle compensation capacitor switch	SPN
$SPNV_{CC}$	46	44	I	Spindle-driver supply voltage	SPN
SPSZ	3	59	I	Serial I/O port select. When low, data goes into port. When high, data goes out of port.	SP
U	47	45, 46	O	Spindle-phase U connection	SPN
UV	5	61	I	Undervoltage, power-on-reset voltage sense input	VM

† 56-terminal DL package
‡ 64-terminal PM package
§ SPN = spindle, VCM = voice-coil motor, VM = voltage monitor, SP = serial port

Terminal Functions (Continued)

NAME	TERMINAL NO.†	TERMINAL NO.‡	I/O	DESCRIPTION	SUBSYSTEM§
V	39	37	O	Spindle-phase V connection	SPN
VCMA	12	11	O	VCM driver output A	VCM
VCMB	17	12	O	VCM driver output B	VCM
VCMGND	11	7, 8, 9, 10		VCM driver supply ground	VCM
VCMREF	28	23	O	VCM voltage reference	VCM
$VCMV_{CC}$	18	13		VCM driver supply voltage	VCM
V_{DD}	10	4	O	Charge-pump voltage-tripler output	SPN
VIVCM	27	22	O	VCM current-sense output (VCM = 2 V)	VCM
VPHASE	33	28	O	Spindle-back-EMF-phase voltage	SPN
W	38	35, 36	O	Spindle-phase W connection	SPN

† 56-terminal DL package
‡ 64-terminal PM package
§ SPN = spindle, VCM = voice-coil motor, VM = voltage monitor, SP = serial port

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)¶

Motor supply voltage, $SPNV_{CC}$, $VCMV_{CC}$ (see Note 1) . . . . . 8 V
Power supply voltage, AV_{CC}, DV_{CC} (see Note 1) . . . . . 6 V
Maximum voltage at U, V, W . . . . . 8 V
Spindle current at U, V, W . . . . . 1.4 A
VCM current, VCMA, VCMB . . . . . 0.41 A
Operating virtual junction temperature, T_J . . . . . 150°C
Thermal resistance (DL package): Junction-to-ambient, $R_{\theta JA}$ (see Note 2) . . . . . 89°C/W
Junction-to-case, $R_{\theta JC}$ (see Note 2) . . . . . 14°C/W
Thermal resistance (PM package): Junction-to-ambient, $R_{\theta JA}$ (see Note 2) . . . . . 71°C/W
Junction-to-case, $R_{\theta JC}$ (see Note 2) . . . . . 14°C/W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . –55°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 250°C

¶ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to ground.
2. The device is mounted on a printed-circuit board with 0.22 square inches of copper connected to the package tabs.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DL	1125 mW	9.0 mW/°C	720 mW
PM	1125 mW	9.0 mW/°C	720 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, DV_{CC}, AV_{CC}, $SPNV_{CC}$, $VCMV_{CC}$		4.5	5	5.5	V
High-level input voltage, V_{IH}	SCLK, SDATA, AUXIN, MTRCLK, PORN, HU, HV, HW, SPSZ	3.5		DV_{CC}+0.3	V
Low-level input voltage, V_{IL}				1.5	V
Setup time, t_{su}	Level change on SDATA or SPSZ before SCLK↓			25	ns
Speed reference clock frequency	MTRCLK		1	12	MHz
Speed reference clock duty cycle		25%	50%	75%	
Speed reference clock duration		20.8	41.6	62.5	ns
Clock frequency	SCLK		1	10	MHz
Clock duty cycle		25%	50%	75%	
Pulse duration, t_w		25	50	75	ns
Operating free-air temperature, T_A		0		70	°C
Operating virtual junction temperature, T_J		0		150	°C

electrical characteristics over recommended supply voltage range, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level output voltage, V_{OH}		I_O = 5 µA	3.5			V
Low-level output voltage, V_{OL}		I_O = 5 µA			1.5	V
Operating supply current, I_{CC}	DV_{CC}, AV_{CC}			20		mA
Sleep supply current, I_{CC}				3		mA
High-level input current, I_{IH}					1	µA
Low-level input current, I_{IL}					–1	µA

voltage and temperature monitor electrical characteristics over recommended supply voltage range, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power-on-reset voltage	UV			1.21		V
Power-on-reset sense bias current					100	nA
Hysteresis				25		mV
Internal power-on-reset threshold voltage, AV_{CC}				4		V
Power-on-reset timing voltage	CPOR	See Note 4		1.21		V
Power-on-reset timing current				5		µA
Output voltage	PORN	I_{PORN}= 1 mA		0.4	0.8	V
Output leakage current					10	µA
Charge-pump voltage-tripler output voltage	V_{DD}		12	13	15	V
Charge-pump voltage-tripler output voltage load regulation		See Note 5		0.25		V/µA
Thermal shutdown hysteresis				20		mV
Voltage monitor accuracy				10 %		
Thermal shutdown temperature				160		°C

NOTES: 3. PORN reset timing is time reset = $C_{CPOR} \times (V_{CPOR}/I_{CPOR})$.
4. V_{DD} can be used to drive external NMOS switches; however, the effective dc loading should be less than 1 µA.

voice-coil motor driver electrical characteristics over recommended range of supply voltage, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Total output drain-to-source on-state resistance, $2 \times r_{DS(on)}$	VCMA, VCMB			2	3	Ω
Total VCM driver voltage drop		I_O = 200 mA			0.6	V
		I_O = 400 mA			1.2	V
VCM driver voltage drop on retract		I_{CRET} = 50 mA, RETSET grounded			1.3	V
VCM gain accuracy				±4%		
VCM differential linearity					±1.6%	
Slew rate				.05		V/µs
Control voltage	RETSET			0.7		V
Pullup resistance	CRET, RETOUT			20		Ω
Output voltage	REFBUF		3.88	4	4.12	V
Output impedance		f = 10 kHz		6.1		Ω
Source current					7	mA
Output voltage	VCMREF		1.94	2	2.06	V
Clamp voltage	CRET	See Note 6		9		V

NOTE 5: Optional Zener diode may be required on CRET for filtering narrow voltage spikes

spindle-motor driver electrical characteristics over recommended supply voltage range, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Total output drain-to-source on-state resistance, $2 \times r_{DS(on)}$	U, V, W			1.3	1.6	Ω
Source-driver output voltage slew rate				0.07		V/µs
Sink-driver output voltage slew rate		See Note 7		0.07		V/µs
Retract clamp diode forward voltage	U, V, W, CRET	I_{RETOUT} = 50 mA		0.5		V
Center tap driver-output saturation resistance	CTDRV	See Note 8		150		Ω
Speed discriminator count range		See Note 9	8	8333	16384	
Maximum compensation voltage		VCM DAC word = FFhex		4		V
Maximum spin compensation voltage		RUN MODE		5		V
Minimum spin compensation voltage				0.8		V
Charge-pump leakage current	SPNCOMP			3	5	nA
Charge-pump output current					±50	µA
Charge-pump output current matching				1%		
Spindle-driver start current	U, V, W				1.2	A

NOTES: 6. This slew rate is determined by the percentage of programmed current.
7. CTDRV is an open-drain switch.
8. The typical count (1041) $f_{spindle}$ = 3600 (RPM) at f(MTRCLK) = 1 MHz

PRINCIPLES OF OPERATION

voltage monitor

The TLS2205 voltage-monitor circuit is designed to monitor the voltage of the system's 5-V power supply. The device has an internal lockout threshold voltage of 4 V. If the power supply drops below 4 V, an internal fault is generated and PORN goes low. In applications where a more accurate threshold is desired (greater than 4 V), an external resistor divider may be connected to UV. If UV is not used, it must be tied to V_{CC} (refer to Figure 1). The following equations can be used to determine the voltage divider resistor values:

$$V_{CC(trip)} = 1.21 / [R2 / (R1 + R2)]$$

where:

UV sense bias current = 10 nA
R1 is resistor connected from V_{CC} to UV
R2 is resistor connected from UV to ground
$V_{CC(trip)} > 4$ V
Hysteresis at UV $\approx$ 25 mV

Note:

A capacitor (Cuv1) may be considered for short-duration power loss.

The voltage monitor incorporates a deglitch timing delay circuit for applications where PORN is used to reset the system's microprocessor. A delay can be implemented on PORN by connecting a capacitor between CPOR and ground. The reset time (see Figure 2) is calculated by using the following equation:

$$TR = C_{CPOR} \times (V_{CPOR} \div I_{CPOR})$$

where:

TR = reset time in seconds
C_{CPOR} = capacitor value in farads
V_{CPOR} = 1 V
I_{CPOR} = 5 μA

Figure 1 represents the voltage-monitor circuit, and Figure 2 represents the power-on reset (PORN) timing diagram. The following is a functional overview of the voltage monitor system. ($V_{CC(trip)}$ = 4.2 V).

Time 1: During startup, Comp1 resets the R-S flip-flop and allows the C_{CPOR} capacitor to start charging. As the supply voltage increases, V_{CPOR} becomes greater than 1.21 V (band-gap voltage), which allows Comp2 to pull PORN high, disabling the retract control circuit.

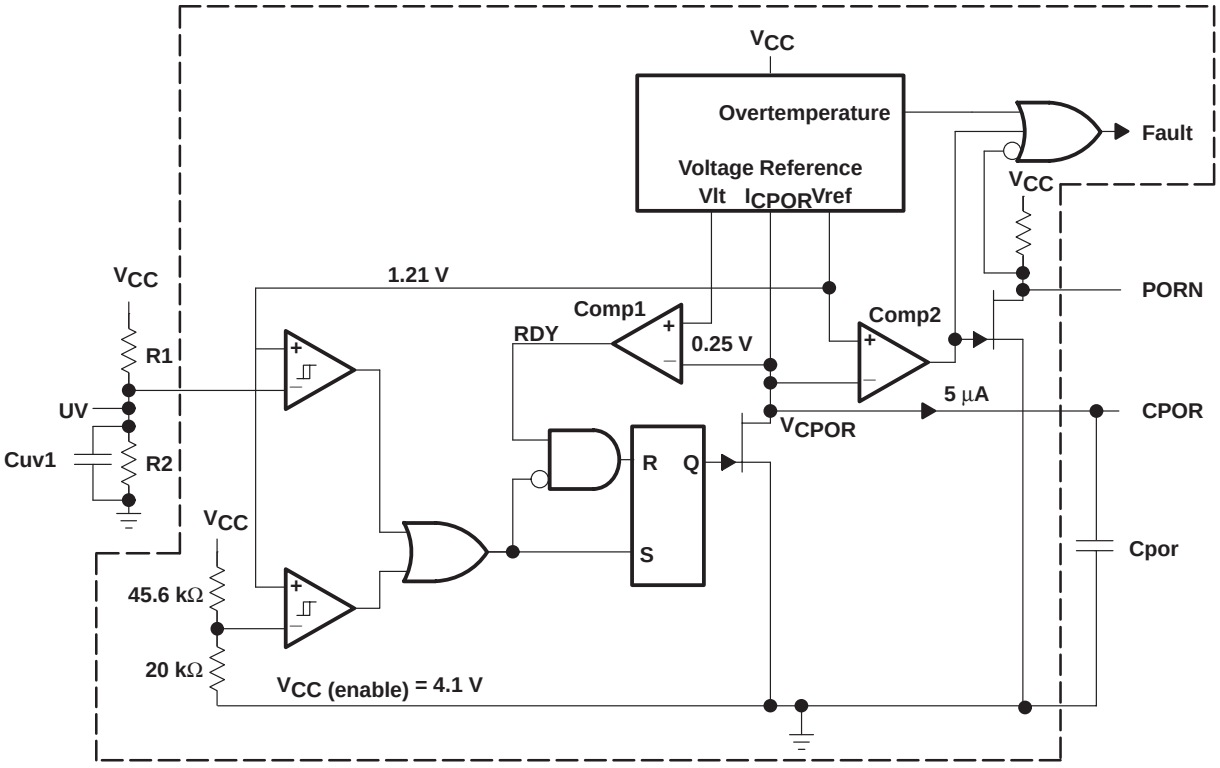
Time 2: Time 2 represents the normal run mode. At this time, the R-S flip-flop is reset, CPOR is high, PORN is high, and the retract control circuit is disabled.

Time 3: An external fault is generated by the microprocessor (or external device) by pulling PORN low. No other parts of the voltage-monitor circuit are affected.

Time 4: If the system's supply voltage drops below the preset value ($V_{CC(trip)}$ = 4.2 V, see Figure 2), the R-S flip-flop is set and allows the capacitor across CPOR to discharge. When V_{CPOR} drops below 1.21 V, PORN is pulled low and a fault is generated that triggers the retract control circuit. Once $V_{CC(trip)}$ increases above the trip level, the R-S flip-flop is reset and C_{CPOR} begins to charge towards V_{CC}. After TR seconds, the voltage across C_{CPOR} is greater than 1.21 V and the retract control circuit is disabled along with PORN being pulled high.

Time 5: Time 5 represents the power down/emergency retract mode. If the system's supply voltage drops below the preset value ($V_{CC(trip)}$ = 4.2 V, see Figure 2), the R-S flip-flop is set and allows the capacitor across CPOR to discharge. When Vcpor drops below 1.21 V, PORN is pulled low and a fault is generated.

PRINCIPLES OF OPERATION



NOTE: Vlt = Low voltage threshold = 0.25 V
V_{CPOR} = Voltage across the power-on-reset capacitor
I_{CPOR} = Current supplied to the CPOR terminal ≃ 5 µA
Vref = Reference voltage = 1.21 V
Area within the dotted line is internal to the device

Figure 1. Voltage Monitor Circuit

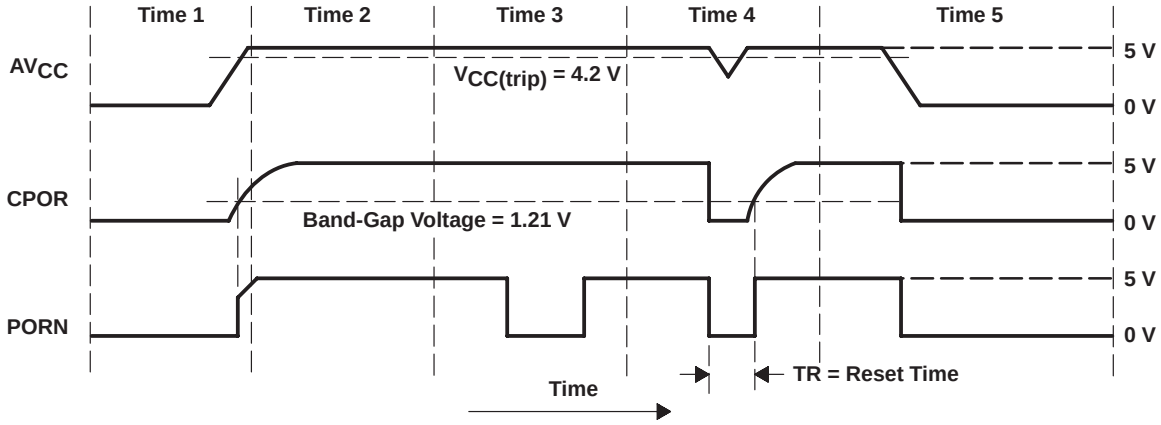


Figure 2. Power-On Reset Timing Diagram

PRINCIPLES OF OPERATION

voice-coil driver system

The voice-coil full-bridge power amplifier is capable of ±0.4-A output current and has a total drain-to-source on-state resistance ($2 \times r_{DS(on)}$) of 2 Ω. The voice-coil control system includes a precision current-sense amplifier that detects load current with a single resistor in series with the voice-coil motor (VCM). The VCM current is commanded via serial port A. Full-scale current is controlled by the value of the VCM current sense resistor (Rsvcm). The retract control circuitry is fully integrated and does not require external isolation of the device power supply terminals such as an external isolation transistor/diodes. Voice-coil driver auxiliary digital control functions include an output-disable and low-power sleep mode following a retract of the VCM to the landing zone. During a fault condition, the VCM drivers are disabled.

VCM current control

The voice-coil motor current is controlled by an internal 8-bit digital-to-analog converter (DAC), four adjustable gain ranges, and the external current-sense resistor (Rsvcm). The four gain ranges (see functional block diagram) are system dependent and provide the current needed to ensure that the head assembly swings across the whole platter. Selecting one of the four gain ranges is accomplished via port A, bits 8 and 9 (see Table 1 for gain settings and Table 4 for bit definitions). During the start mode, the 8-bit DAC is used to start the spindle (see Figure 5). In the run mode, the 8-bit DAC is used to program the VCM current. Port A (bits 0–7) controls the 8-bit DAC (see Table 4). The VCM current-control equation is given as follows:

$$I_{VCM} = I_X [B7 + 1/2\ B6 + 1/4\ B5 + 1/8\ B4 + 1/16\ B3 + 1/32\ B2 + 1/64\ B1 + 1/128\ \ B0–1] [A]$$

where:

$I_X = (V_{ref} \times G)/(16 \times Rsvcm)$
I_X (+ full scale) at V = $FF
I_X (– full scale) at V = $00
V_{ref} (the internal system voltage reference) = 2 V
Rsvcm (the external VCM current sense resistor) typically 0.47 Ω ±1%
G (the VCM current gain scale)
B0–B7 (port-A control bits)

Maximum VCM current is load dependent. The following equation should be used as a guideline to determine maximum VCM current:

$$I_{VCM}max = V_{CC}max / Rtotal$$

where:

$V_{CC}max = 5.5$ V
$Rtotal = Rsvcm + 2 \times r_{DS(on)} + Rvcm$

Table 1. VCM Gain-Range Scale Truth Table

GAIN SWITCH SETTING (see functional block diagram)			SERIAL PORT A GAIN SETTINGS (see Table 4)		
GS1	GS2	GS3	GR0	GR1	GAIN (G)
Open	Open	Open	0	0	0.250
Closed	Open	Open	0	1	0.333
Open	Closed	Open	1	0	0.500
Open	Open	Closed	1	1	1.000

PRINCIPLES OF OPERATION

VCM current-loop stability is accomplished using the filter at CMPI and CMPO. This filter has the following transfer function:

$$\frac{(Rcmp \times (Ccmp2 + Cmp1) \times s + 1)}{Ccmp2 \times s \times (Rcmp \times Ccmp1 \times s + 1)}$$

where:

s is a Laplace operator

VCM retract

The TLS2205 integrated retract circuit eliminates the need for external power supply isolation devices. The retract mode is triggered by the voltage monitor fault logic signal. The retract power path is coupled from the spindle-motor back-EMF to the RETOUT MOS high-side driver via CRET. After the retract control block has been triggered by a loss of power, the following events occur:

1. The system control logic is reset to the power-up state. All bias is disabled (including V_{DD}); all power outputs are disabled.
2. The retract control circuit locks the VCMB low-side driver on and disables the VCMB high-side driver.
3. The retract control circuit disables the VCMA low- and high-side drivers.
4. RETOUT is enabled, and RETSET is used to control the voltage applied to RETOUT.

The spindle back-EMF-mode voltage supplies the energy necessary to retract the VCM (see Figure 3). The energy stored in the capacitor (CV_{DD}) connected to V_{DD} is used to control the RETOUT and VCMB power devices. The value of this capacitor can be calculated based on ~ 2 μA of retract-mode discharge current and the time to retract (Δt) the VCM. The RETOUT control equation is:

$$V_{VCMA} = V_{be} \times [1 + (Rrset1/Rrset2)]$$

$$CV_{DD} = \frac{2\ \mu A \times (\Delta t)}{V_{VCMA}}$$

where:

V_{be} is the base-to-emitter junction voltage ≈ 0.7 V.

Example:

Assume: Rrset1 = 62 kΩ
Rrset2 = 100 kΩ
Δt = 6 ms max

$$\text{Therefore: } CV_{DD} = \frac{2\ \mu A \times (5\ ms)}{0.7\ V \times (1 + 62\ k\Omega/100\ k\Omega)}$$

$$= 0.009\ \mu F$$

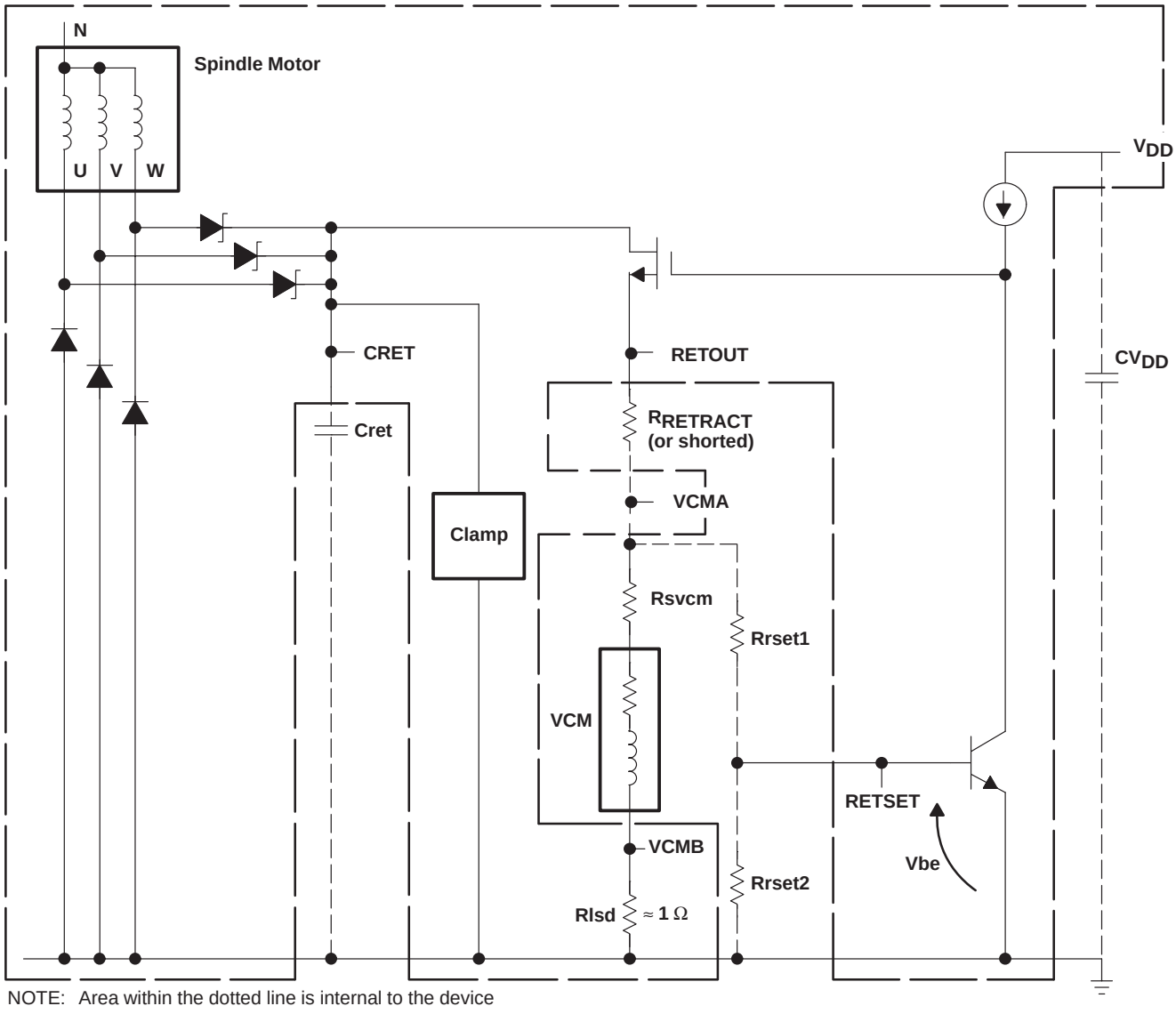
$$\approx 0.01\ \mu F$$

$$\Delta t = \frac{0.01\ \mu F \times [0.7\ V \times (1 + 62\ k\Omega/100\ k\Omega)]}{2\ \mu A}$$

$$= 5.7\ ms$$

PRINCIPLES OF OPERATION

Figure 3 shows a block diagram of the TLS2205 retract equivalent circuit (retract mode only).



NOTE: Area within the dotted line is internal to the device

Figure 3. Retract Equivalent Circuit

spindle-driver system

The spindle-driver system is capable of ±1-A output current and has a total drain-to-source on-state resistance ($2 \times r_{DS(on)}$) of 1.3 Ω. Soft switching on the output drivers eliminates the need for external snubbers or flyback diodes. An internal voltage clamp circuit helps protect against flyback voltages, while internal Schottky diodes provide a low-loss power path for the VCM retract function. Internal logic and analog detection circuitry provide complete sequencing of the power outputs in all run modes. Support for unipolar operation is provided by disabling the spindle high-side drivers and pulling the motor center tap to 5 V using an external pnp or PMOS transistor. CTDRV is used to control the base of the transistor during unipolar operation and is open otherwise. During a fault condition, the spindle-motor drivers are disabled.

PRINCIPLES OF OPERATION

spindle-driver system (continued)

For active braking, all the spindle low-side drivers are disabled and the high-side drivers are enabled, thereby shorting out the spindle windings at or near the supply voltage, $SPNV_{CC}$.

spindle commutation

Hall- or back-EMF-spindle commutation is selected from serial port C. See the port-C system control bit definitions in Table 6 for additional information.

Hall mode

In the Hall mode, the spindle position information is input to the TLS2205 via the HU, HV, and HW logic input terminals. Start current can be controlled with the internal 8-bit DAC, which is normally used to control the VCM current or the internal charge pump. If the DAC option is selected, the VCM driver is normally disabled during spindle start for power conservation. In either case, the spindle motor starts without microprocessor intervention.

back-EMF mode

For the back-EMF mode, the system microprocessor is used in conjunction with the TLS2205 internal circuitry to start the spindle motor.

Start current is controlled the same way as in the Hall mode by using the DAC. Two schemes can be used to start commutation in the back-EMF mode. The first scheme is to use AUXIN; this method requires a pulse generated from the microprocessor as an input signal to AUXIN. Various frequencies and start currents are used to start the spindle motor. The second scheme is to use the COMM bit (bit 4) in port C. This method requires the microprocessor to write to port C to change the state of bit 4. For every 1-to-0 state change of bit 4, the spindle inverters advance one state. Different frequencies and start currents are used to start the spindle motor. Once the motor has reached approximately 10% of its rated speed, the TLS2205 may be switched into the run mode via port C.

Figure 4 shows the TLS2205 commutation delay circuit and the required external components.

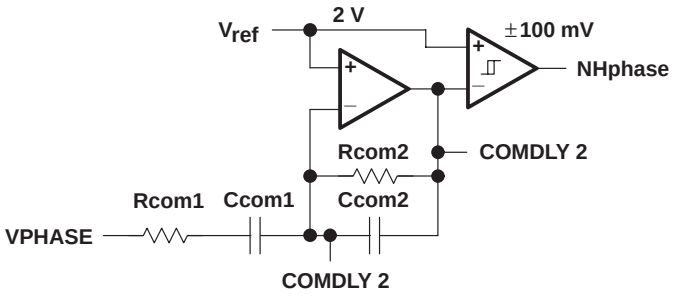


Figure 4. Commutation Delay Circuit

This circuit is composed of an operational amplifier (OPA) followed by a hysteresis comparator. The TLS2205 spindle inverter is advanced for every transition of the NHphase signal. The transition of NHphase occurs every time the COMDLY2 signal crosses the common-mode reference, V_{ref}. The required external components are defined as:

Rcom1 – Integrator gain-set resistor
Ccom1 – DC-blocking capacitor
Rcom2 – Integrator dc-set resistor
Ccom2 – Integrator gain-set capacitor

PRINCIPLES OF OPERATION

back-EMF mode (continued)

The transfer function between COMDLY2 and VPHASE is :

$$Vcomdly2 = \frac{s \times (Rcom2 \times Ccom1) \times VPHASE}{[1+s \times (Rcom1 \times Ccom1)] \times [1+ s \times (Rcom2 \times Ccom2)]}$$

where:

s is a Laplace operator

The component design procedures include the following:

- Choose Rcom2 with a value as large as possible to permit small capacitor values. The typical value for Rcom2 is 1 MΩ.
- Calculate Ccom2 so that there is at least 45° of phase shift at the phase frequency where the TLS2205 is switched into the internally commutated mode. The approximate value is 10% of the target frequency.
- Calculate Rcom1 based on the desired COMDLY2 signal swing at the target frequency. The recommended signal swing is 1.25 V peak. Near the target frequency the integrator function, VCOMDLY2/VPHASE, becomes:

$$\frac{VCOMDLY2}{VPHASE}[Mag] = \frac{1}{(Rcom1 \times Ccom2) \times (3 \times \text{num motor poles}/2) \times Wmotor}$$

$$\frac{VCOMDLY2}{VPHASE}[Phase] = -90°$$

$$VCOMDLY2 = \frac{0.433 \times Kb \times Wmotor \times \sin(Wmotor \times t)}{(Rcom1 \times Ccom2) \times (3 \times \text{num motor poles}/2) \times Wmotor}$$

$$VCOMDLY2 = \frac{0.433 \times Kb \times \sin(Wmotor \times t)}{(Rcom1 \times Ccom2) \times (3 \times \text{num motor poles}/2)}$$

The peak value of this function is independent of the frequency.

$$Rcom1 = \frac{0.433 \times Kb}{1.25 \times Ccom2 \times (3 \times \text{Num Motor Poles}/2)}$$

- Choose Ccom1 such that the dc-blocking pole, 1/(Rcom1 × Ccom1), occurs at a frequency below the integration pole, 1/(Rcom2 × Ccom2). Typically the dc-blocking pole is placed at 1/2 the integration pole.

  Where:

  Wmotor = Mechanical frequency of the motor, r/s

  Kb = Back-EMF constant, V/(r/s)

The internal speed-regulation feedback loop then takes control of spindle commutation, and further microprocessor intervention is not required. Figure 5 shows the timing relationships for the spindle-motor-control sequencing in both Hall and back-EMF modes. Internal logic and analog filtering provide the commutation function in the commonly used back-EMF mode. In this mode, VPHASE (the difference between the undriven phase and the center tap voltage) is filtered to generate a signal that determines commutation timing (NHphase).

PRINCIPLES OF OPERATION

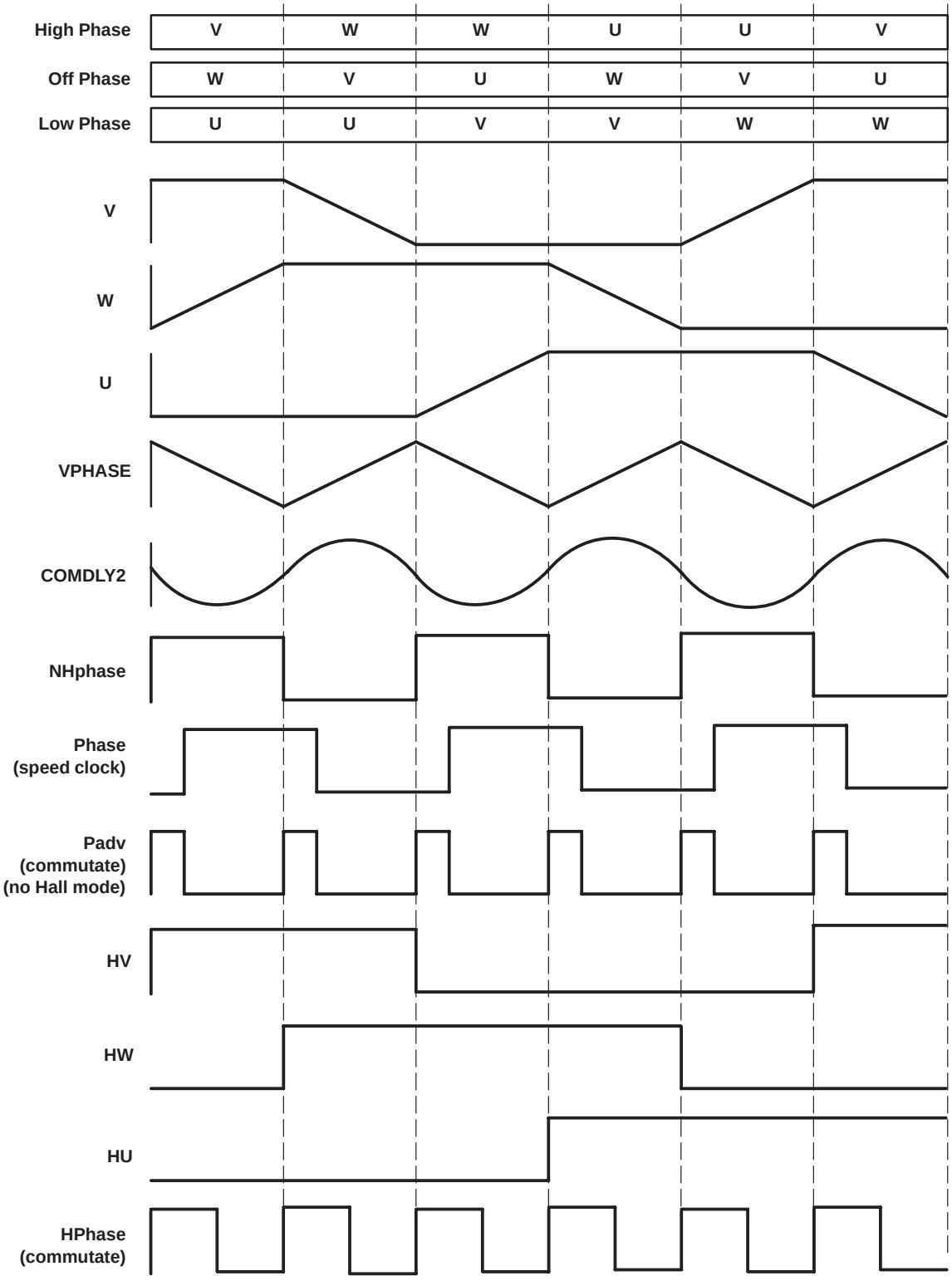


Figure 5. Spindle-Motor Control Sequencing

PRINCIPLES OF OPERATION

spindle-current control

Spindle-current control is accomplished by regulating the current through the external sense resistor, Rsspn, via the spindle low-side drivers (LSD). Figure 6 illustrates the arrangement for the spindle-current control (port C, bit 5) during the start mode (SPNMODE = 1) and the run mode (SPNMODE = 0). During startup (SPNMODE = 1), the 8-bit DAC is used to command the spindle start current. Upon switching to the run mode (SPNMODE = 0), the 8-bit DAC is used to control the VCM and the spindle motor is switched into closed-loop operation (see Figure 6). The transconductance function is:

$$I_{spindle} = (0.079\ SPNCOMP - 0.057) / Rsspn$$

Note:

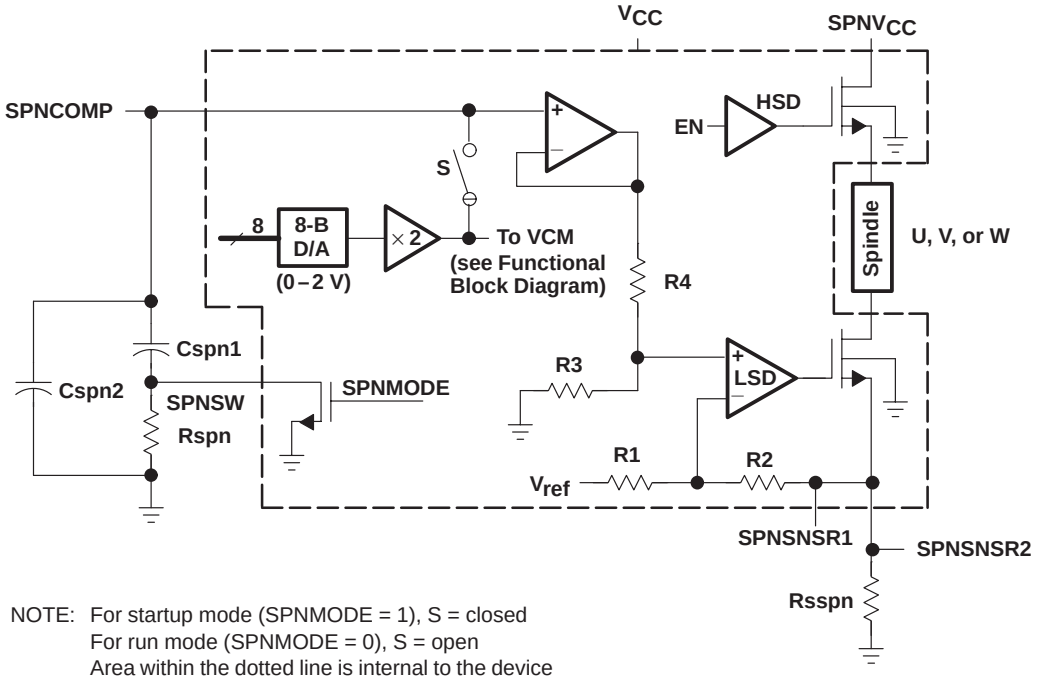
Rsspn is typically 0.2 Ω
V_{gs} ~ 1 V

Maximum spindle current is load dependent. The following equation should be used as a guideline to determine maximum spindle current:

$$I_{spindle} = V_{CC}(max) / Rtotal$$

where:

$V_{CC}(max) = 5.5$ V
$Rtotal = Rsspn + 2 \times r_{DS(on)} + Rspindle$



NOTE: For startup mode (SPNMODE = 1), S = closed
For run mode (SPNMODE = 0), S = open
Area within the dotted line is internal to the device

Figure 6. Spindle-Current Control

PRINCIPLES OF OPERATION

spindle-speed control

The TLS2205 provides a frequency-locked-loop speed-control system. Figure 7 is an illustration of the spindle-speed control loop. This system operates by generating a once-around signal from either Hall or back-EMF state changes. This signal is then divided by either 12 (for 8-pole motor) or 18 (for 12-pole motor) (port B bit 11). This signal is called Fspn. Fspn is a once-around spindle-motor clock. Fspn is compared to a signal that is generated from the MTRCLK (Fref). Fref is generated by dividing the MTRCLK by 16, then dividing again by the value stored in the spindle-reference counter (port B bits 0–10). The Fref and Fspn signals are compared, and the time domain error is fed to the charge pump every other rotation. The charge-pump output is a speed error signal that is filtered by a PI filter at SPNCOMP. The output of this filter commands the spindle current. The spindle rotation TACH output (Fspn) or the back-EMF commutation clock (NHphase) can be directly measured at AUXOUT. AUXIN can be used to provide an external index signal for motor commutation instead of using the speed feedback circuit. See Table 7 for a description of the spindle-motor operating modes.

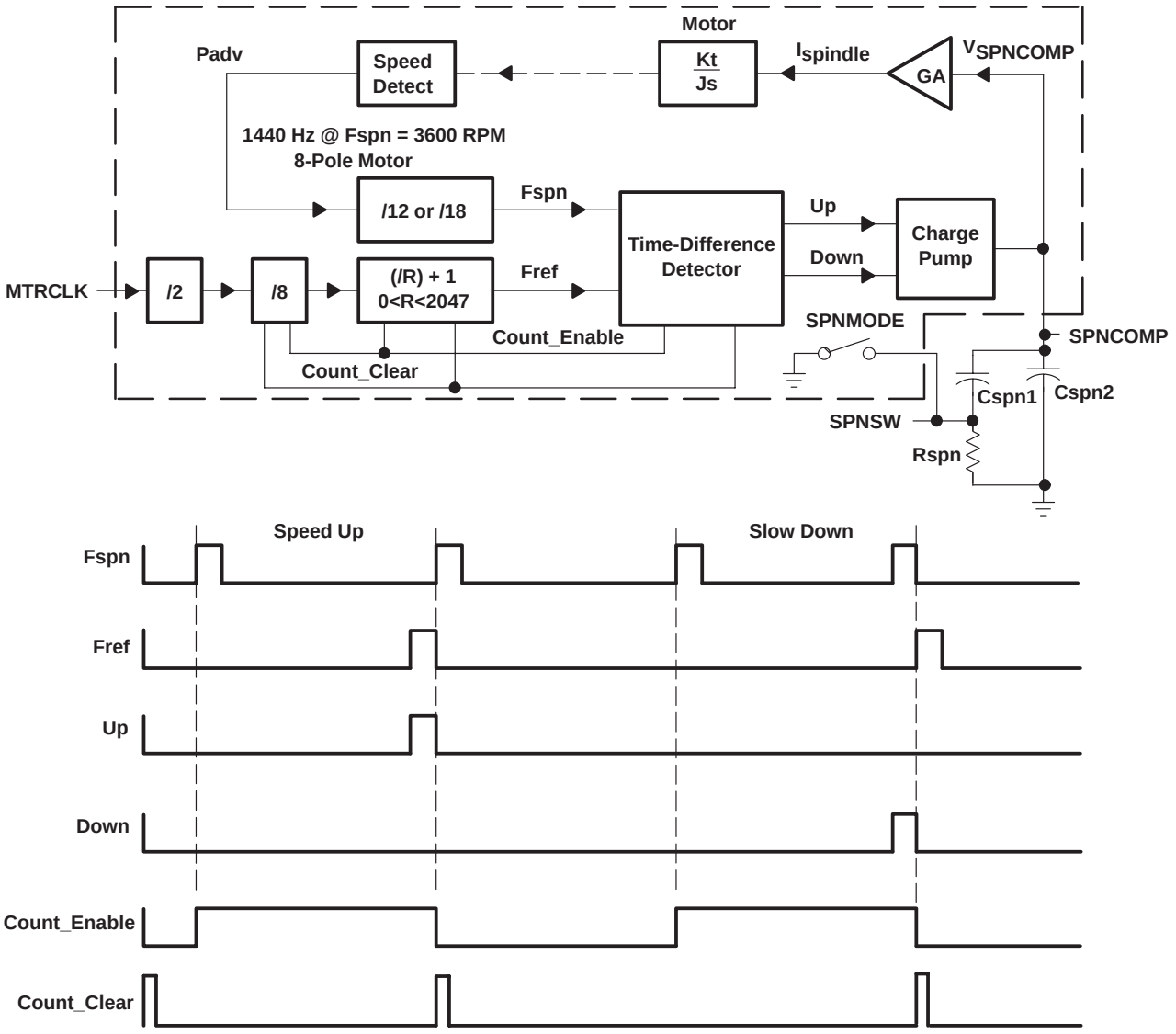
Spindle rotational speed is calculated from the equation below:

$$f_{spindle} = f_{MTRCLK} / [(16 \times R) + 1] \text{ [Hz]}$$

where:

R is the value stored in port B bits 0–11 ($0 < R < 2047$)
Spindle-speed regulation $\cong 1 / [(8 \times R) + 1]$ (%)

PRINCIPLES OF OPERATION



NOTE: Area within dotted line is internal to the device

Figure 7. Spindle-Control Loop Block Diagram and Timing Waveforms

serial port

The TLS2205 serial port is designed to receive 16-bit data in three-wire serial format and distribute the data to internal data and control ports. The serial-port interface is designed to be compatible with the Texas Instruments TMS320C2x digital signal processor (DSP) family or standard 8- or 16-bit microprocessors. Data can be transmitted in either 8- or 16-bit format. The data is sent MSB first for the 16-bit word. The first four MSBs determine the port address. The other 12 bits are used for data or port control functions. The first two MSBs must both be 0 to select the device. The received data is routed to one of three internal 12-bit register ports. Port A controls the VCM DAC and gain range of eight data bits with four gain ranges. Port B is used to set the spindle reference counter. Port C is used for system controls.

PRINCIPLES OF OPERATION

serial-port timing

The TLS2205 is designed to receive data in four basic formats: TMS320C2x burst mode, TMS320C2x continuous mode, 8-bit microprocessor format mode, and 16-bit microprocessor format mode.

The serial port uses three control lines: SCLK (serial-port clock), SDATA (serial-port data), and SPSZ (serial-port select not). The SCLK line is a serial data clock with data rates up to 12 MHz; SCLK should have a 50% duty cycle. The SDATA line is the actual serial data input and must be synchronous with the leading edge of SCLK. SPSZ is the serial-port select input and is internally tied low to be synchronous with the leading edge of SCLK.

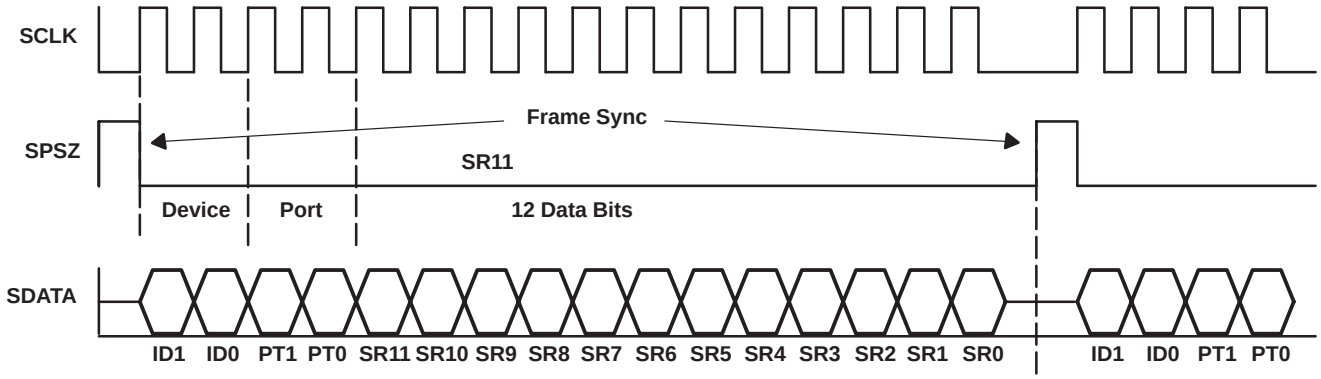
If the TMS320C2x DSP is used in burst or continuous modes, the following bits in the ST1 register should be set (1) or reset (0) as indicated:

BIT NAME	BIT #	SET/RESET	RESULT
TXM (transmit mode)	2	1	FSX is configured as an output
FO (format)	3	0	16-bit mode selected
FSM (framing sync)	5	1	A framing sync is generated

Refer to the TMS320C2x User's Guide for further details.

burst mode

In the serial-port burst-mode operation, transfers are separated in time by periods of no serial-port activity (the serial port does not operate continuously). For burst-mode operation, the SPSZ line must be low on the negative-going edge of SCLK before data is read in; then 16 data bits can be read in. All continuing data bits are ignored until the SPSZ line is toggled from low to high to low. Then data is valid on the first negative-going clock. See Figure 8 for details.



NOTE: ID1 must be the first bit shifted into the register; after 15 shifts, the TLS2205 is selected and the desired port is loaded with valid data.

Figure 8. Serial-Port Burst-Mode Operation

PRINCIPLES OF OPERATION

continuous mode

In the continuous-mode serial-port operation, transfers are continuous in time. In the continuous mode, the SPSZ line is toggled from high to low every falling edge (16 SCLK cycles). See Figure 9 for details.

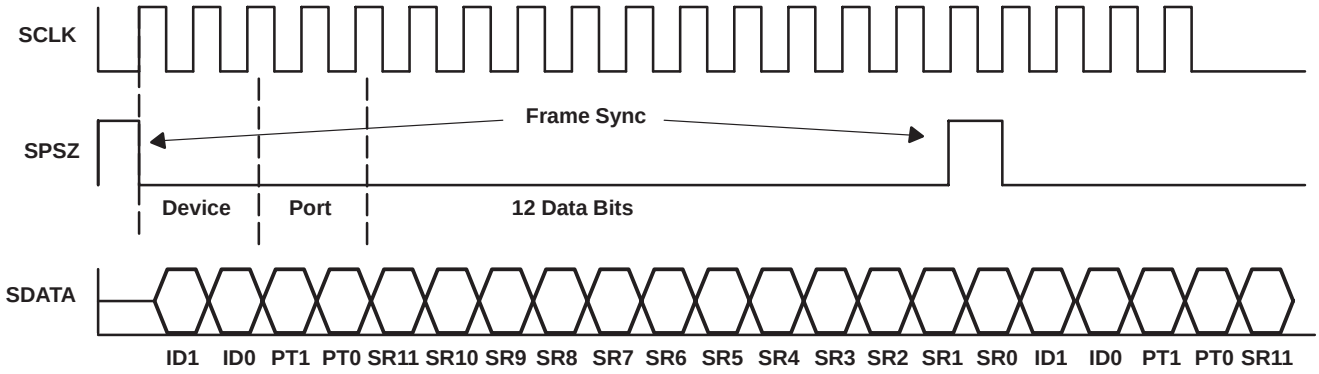


Figure 9. Serial-Port Continuous-Mode Operation

8-bit/16-bit microprocessor mode

In 8- or 16-bit serial-port operation, transfer of data must meet the following criteria:

1. SDATA must change on the leading edge of SCLK.
2. SPSZ must go high after the falling edge of SCLK at the end of byte 1 of the data transmission.
3. SPSZ must go low on the leading edge of SCLK during the first bit of the second byte of the data transmission.
4. SPSZ must stay low until SCLK goes low on the last bit of the second byte of the data transmission.

After the second byte has been transmitted, the data is decoded and sent to the proper port. If the SPSZ line goes high during an invalid bit time, the serial port resets and waits for a valid address. See Figure 10 for details.

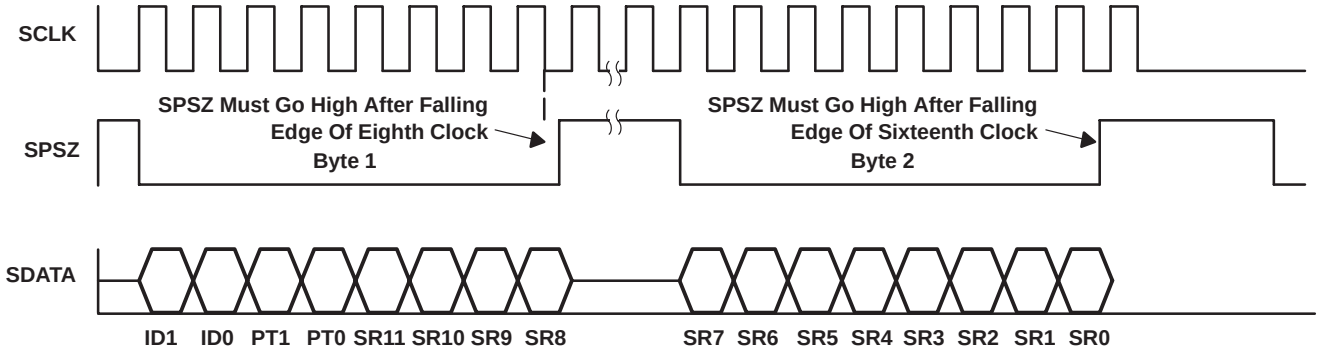


Figure 10. Serial-Port Microprocessor-Mode Operation

NOTE: ID1 must be the first bit shifted into the register; after 15 shifts, the TLS2205 is selected and the desired port is loaded with valid data.

port and data-bit definitions

The TLS2205 incorporates three programmable ports that must be programmed via the serial port (SCLK, SDATA, and SPSZ). ID0 must be the first bit shifted into the register; after 15 shifts, the following occurs:

1. If ID0 = 0 and ID1 = 0, the TLS2205 is selected (see Table 2) and the rest of the data is processed.
2. PT0 and PT1 determine which port is selected (see Table 3).
3. The 16 bits of data are serially loaded into the serial port register.
4. The selected port is loaded with all 16 bits of data. Port A controls the VCM (see Table 4), port B controls the spindle motor (see Table 5), and port C controls the device functions (see Table 6).

Table 2. Device Select

DEVICE SELECT	ID1	ID0	DESCRIPTION
Chip selected	0	0	The TLC2205 serial port is selected.
Chip not selected	0	1	
	1	0	
	1	1	

Table 3. Port Selection

PORT SELECT	PT1	PT0	DESCRIPTION
No port	0	0	Null
A	0	1	VCM port A
B	1	0	Spindle-speed port B
C	1	1	System control port C

PRINCIPLES OF OPERATION

Table 4. Port-A Definition (VCM Control)

BIT #	NAME	DESCRIPTION
0	B0	VCM DAC control word LSB
1	B1	VCM DAC control word
2	B2	VCM DAC control word
3	B3	VCM DAC control word
4	B4	VCM DAC control word
5	B5	VCM DAC control word
6	B6	VCM DAC control word
7	B7	VCM DAC control word MSB
8	GR0	VCM gain-control LSB
9	GR1	VCM gain-control MSB
10	—	Future expansion
11	—	Future expansion
12	PT0	Port-select LSB
13	PT1	Port-select MSB
14	ID0	Device-select LSB
15	ID1	Device-select MSB

Table 5. Port-B Definition (Spindle-Speed Regulator Control Word)

BIT #	NAME	DESCRIPTION	COUNT
0	R0	Spindle reference-counter LSB	1
1	R1	Spindle reference counter	2
2	R2	Spindle reference counter	4
3	R3	Spindle reference counter	8
4	R4	Spindle reference counter	16
5	R5	Spindle reference counter	32
6	R6	Spindle reference counter	64
7	R7	Spindle reference counter	128
8	R8	Spindle reference counter	256
9	R9	Spindle reference counter	512
10	R10	Spindle reference-counter MSB	1024
11	MTR POLE	Spindle-motor pole switch (8 or 12) 0 = 8 pole, 1 = 12 pole	
12	PT0	Port-select LSB	
13	PT1	Port-select MSB	
14	ID0	Device-select LSB	
15	ID1	Device-select MSB	

PRINCIPLES OF OPERATION

Table 6. Port-C Definition (System Control Functions)

BIT #	NAME	SUBSYSTEM	DESCRIPTION
0	SPNENA	SPN	Spindle power-inverter enable
1	START	SPN	Spindle-operation mode
2	NHALLS	SPN	No Hall-commutation-mode select
3	UPOLAR	SPN	Spindle-inverter unipolar select
4	COMM	SPN	Spindle-inverter advance (no hall mode)
5	SPNMODE	SPN	Select DAC current-control mode
6	VCMENA	VCM	VCM power output enable
7	BRAKE	SPN	Spindle BRAKE enable
8	BEMF GAIN	SPN	Back-EMF amplifier sense gain
9	AUX0	SYS	AUXOUT function select MSB
10	AUX1	SYS	AUXOUT function select LSB
11	AWAKE	SYS	System power enable
12	PT0	SYS	Port-select LSB
13	PT1	SYS	Port-select MSB
14	ID0	SYS	Device-select LSB
15	ID1	SYS	Device-select MSB

Port-C system control bit definitions

AWAKE

This bit controls the dc bias conditions in the device. When this bit is low, the device is in the sleep mode and all dc bias sources, with the exception of the voltage monitor, are disabled. All logic, with the exception of the serial register, is disabled, and device power dissipation is minimized. When this bit is high, the device is awake and power dissipation is maximum.

AUX1

AUX1 is the MSB of the auxiliary logic control functions (see Table 7).

AUX0

AUX0 is the LSB of the auxiliary logic control functions (see Table 7).

BEMF GAIN

This bit controls the gain of the back-EMF sense amplifier. When the bit is low, the forward back-EMF gain sense (measured at Vphase) is one. When the bit is high, the forward sense gain is five. This function is intended to start the spindle motor in back-EMF mode.

BRAKE

BRAKE enables the high-side power inverters and disables the low-side power drivers. The brake is normally implemented after a retract has occurred and the head has reached the head stop.

VCMENA

VCMENA enables the VCM output drivers. In the disabled state, the VCM output power amplifier outputs go low. However, the power amplifiers still have dc bias applied and can be enabled in a short period of time.

PRINCIPLES OF OPERATION

Port-C system control bit definitions (continued)

SPNMODE

SPNMODE is used to determine whether the spindle charge pump or DAC is driving the spindle-control amplifiers. When SPNMODE is asserted, the spindle current is controlled by the DAC.

COMM

The COMM bit is used to commutate the spindle driver in the start mode. For every low-to-high state change, the spindle inverter advances one step.

UPOLAR

UPOLAR controls the spindle-motor drive mode. When this bit is low, the TLS2205 drives the motor in a standard bipolar mode. When this bit is high, CTDRV is switched low and the internal high-side drivers are disabled. An external pnp transistor can be switched on using CTDRV, and the device operates in the unipolar mode.

NHALLS

The NHALLS bit controls which commutation mode is used by the spindle-control logic. When this bit is 0, the TLS2205 uses the Hall sense inputs (HU, HV, HW) to directly commutate the spindle motor. When this bit is 1, the TLS2205 switches into the back-EMF commutation mode. The Hall inputs have no meaning in the back-EMF commutation mode. However, the Hall logic inputs determine the motor inverter power-up initial state. The Hall inputs are internally tied low.

START

This bit controls the spindle-motor driver logic inputs and auxiliary I/O signals (see Table 7).

SPNENA

The SPNENA bit enables the spindle-motor drivers. The charge-pump control path (SPNCOMP) is not affected by this bit. When this bit is 0, the spindle-motor power drivers are disabled (motor phases U, V, W are Hi-Z) but not powered down. When this bit is 1, the spindle drivers are enabled.

AUXIN/AUXOUT functional description

Port-C controls (for spindle-motor operation in back-EMF mode)

The spindle-motor operation modes are shown in the description section of Table 7. To fully understand this figure, the functional block diagram must be used in conjunction with port C.

As an example:

1. To start the drive (START MODE), START (bit 1) = 0, AUX1 (bit 10) = 1, and AUX0 (bit 9) = 1. As a result, Phase is the signal seen on the internal PCLK line, SCK is the signal seen on the internal PADV line, and NHphase is the signal seen at AUXOUT.
2. Once the spindle is spinning at approximately 20% of rated speed, the drive is switched into RUN MODE 0 (START = 0, AUX1 = 0, and AUX0 = 0). As a result, phase is the signal seen on the internal PCLK line and NHphase is the signal seen on the internal PADV line and at AUXOUT.
3. After the spindle reaches operational speed, the drive is switched into RUN MODE 3 (START = 0, AUX1 = 1, AUX0 = 1). As a result, AUXIN is the signal seen on the internal PCLK line, NHphase is the signal seen on the internal PADV line, and Fspn is the signal seen at AUXOUT.

PRINCIPLES OF OPERATION

Table 7. Spindle-Motor Operating Modes

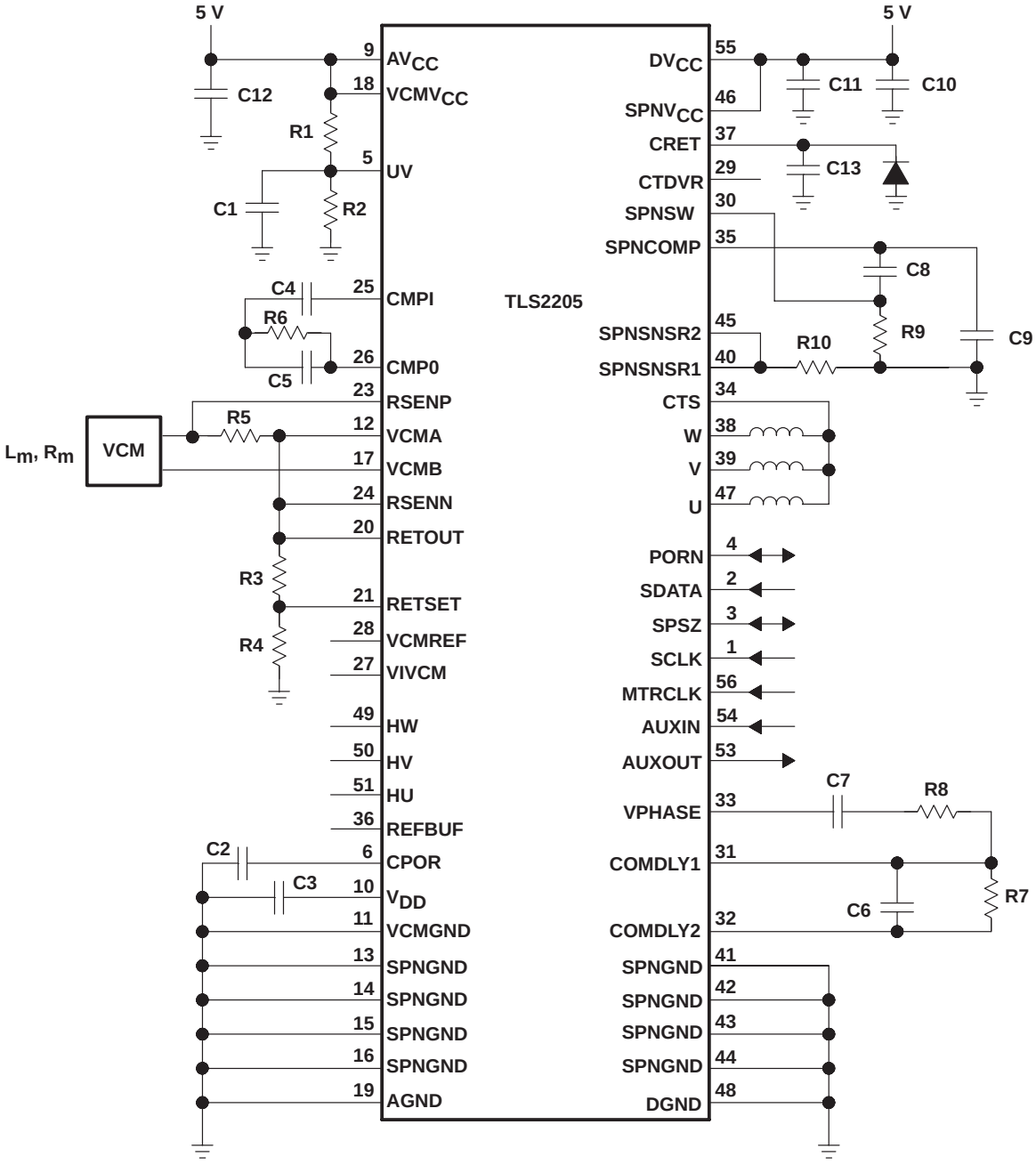
PORT C			AUXOUT	PCLK	PADV	DESCRIPTION
START BIT 1	AUX1 BIT 10	AUX0 BIT 9	MULTIPLEXER OUTPUT	MULTIPLEXER OUTPUT	MULTIPLEXER OUTPUT	
0	0	0	NHphase	Phase	NHphase	RUN MODE0
0	0	1	NHphase	AUXIN	NHphase	RUN MODE1
0	1	0	Fspn	Phase	NHphase	RUN MODE2
0	1	1	Fspn	AUXIN	NHphase	RUN MODE3
1	0	0	Fref	AUXIN	SCK	TEST MODE0 †
1	0	1	Fref	AUXIN	SCK	TEST MODE1 †
1	1	0	Fspn	AUXIN	SCK	TEST MODE2 †
1	1	1	NHphase	Phase	SCK	START MODE

† These test modes were developed for internal chip testing.

descriptions

AUXOUT: The auxiliary logic output multiplexer
AUXIN: The auxiliary logic input (can be used to commutate spindle)
PCLK: The spindle-speed feedback clock (AUXIN or phase)
PADV: The spindle phase-advance clock (back-EMF mode)
START: Spindle start mode (from port C, bit 1, 1 = enable)
AUX0: Option control (from port C, bit 9)
AUX1: Option control (from port C, bit 10)
COMM: Commutation via serial port (from port C, bit 4)
Fspn: The once-around signal and the frequency of PCLK divided by 12 for an 8 pole motor (bit 11 on port B set low), or divided by 18 for a 12 pole motor (bit 11 on port B set high).
Fref: The divided output of the speed-discriminator reference frequency (MTRCLK)
Phase: The spindle-control logic output of the spindle even states (see Figure 4, SC 0,2,4)
NHphase: No Halls phase is the back-EMF zero-crossing clock
Hphase: Halls-phase clock from external Hall sensors
SCK: Start clock, AUXIN ORed with COMM (from port C, bit 4)
RUN MODE 0: Speed feedback information comes from motor commutation, AUXOUT = NHphase
RUN MODE 1: Speed feedback information comes from AUXIN, AUXOUT = NHphase
RUN MODE 2: Speed feedback information comes from motor commutation, AUXOUT = Fspn
RUN MODE 3: Speed feedback information comes from AUXIN, AUXOUT = Fspn
TEST MODE 0: AUXOUT = Fref: Fref = MTRCLK/N; N = value stored in port-B reference counter
TEST MODE 1: AUXOUT = Fref: Fref = MTRCLK/(16 × N); N = same as above
TEST MODE 2: AUXOUT = Fspin: Fspin = AUXIN/12 or 18 depending on number of motor poles (port B, bit 11)
START MODE: Spindle commutation is controlled externally via AUXIN

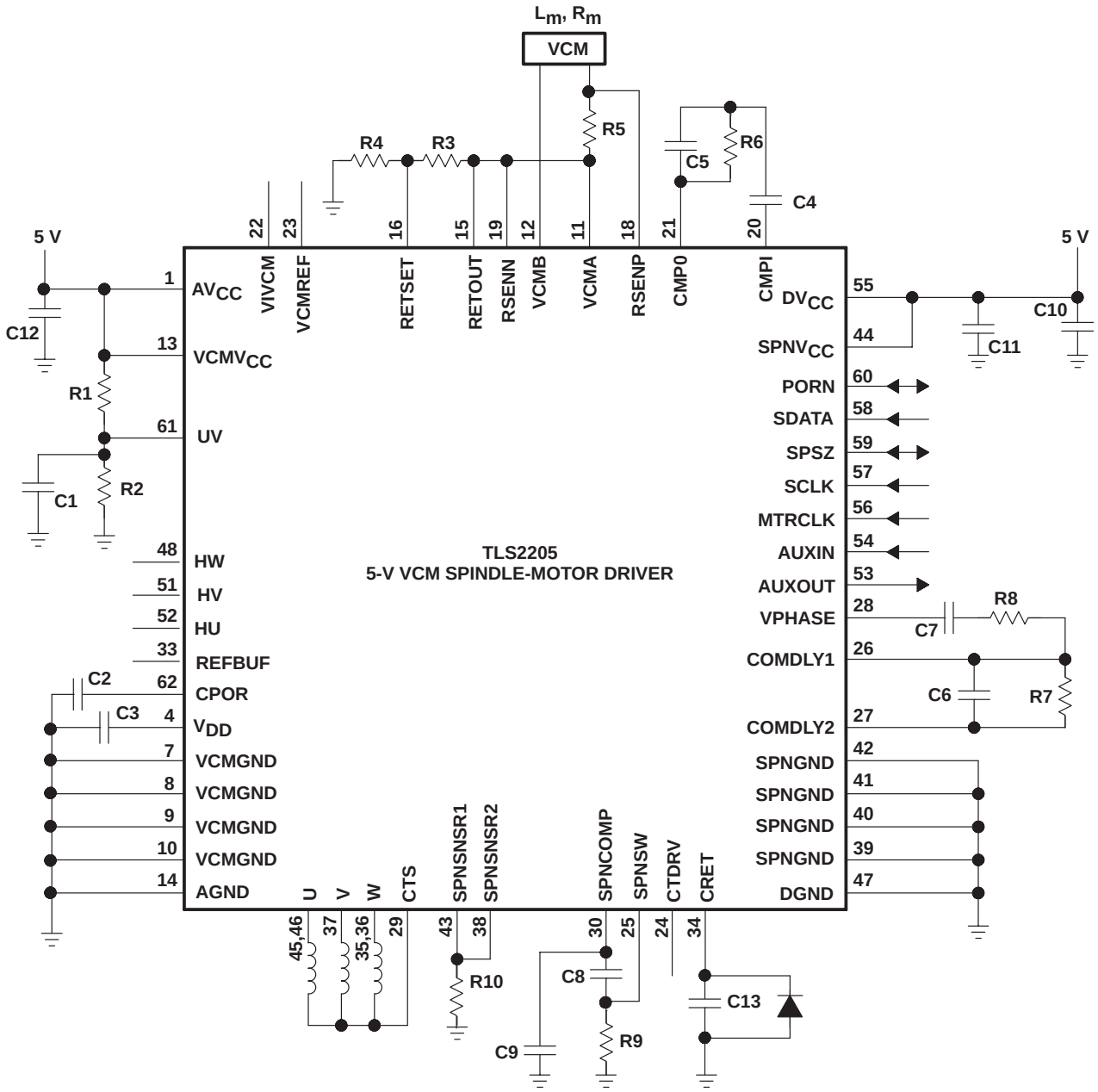
APPLICATION INFORMATION



Pin numbers shown are for the DL package; see Table 8 for external component values.

Figure 11. Spindle Motor-Driver Application

APPLICATION INFORMATION



Pin numbers shown are for the PM package; see Table 8 for external component values.

Figure 12. Spindle Motor-Driver Application

APPLICATION INFORMATION

Table 8. External Components and Approximate Values

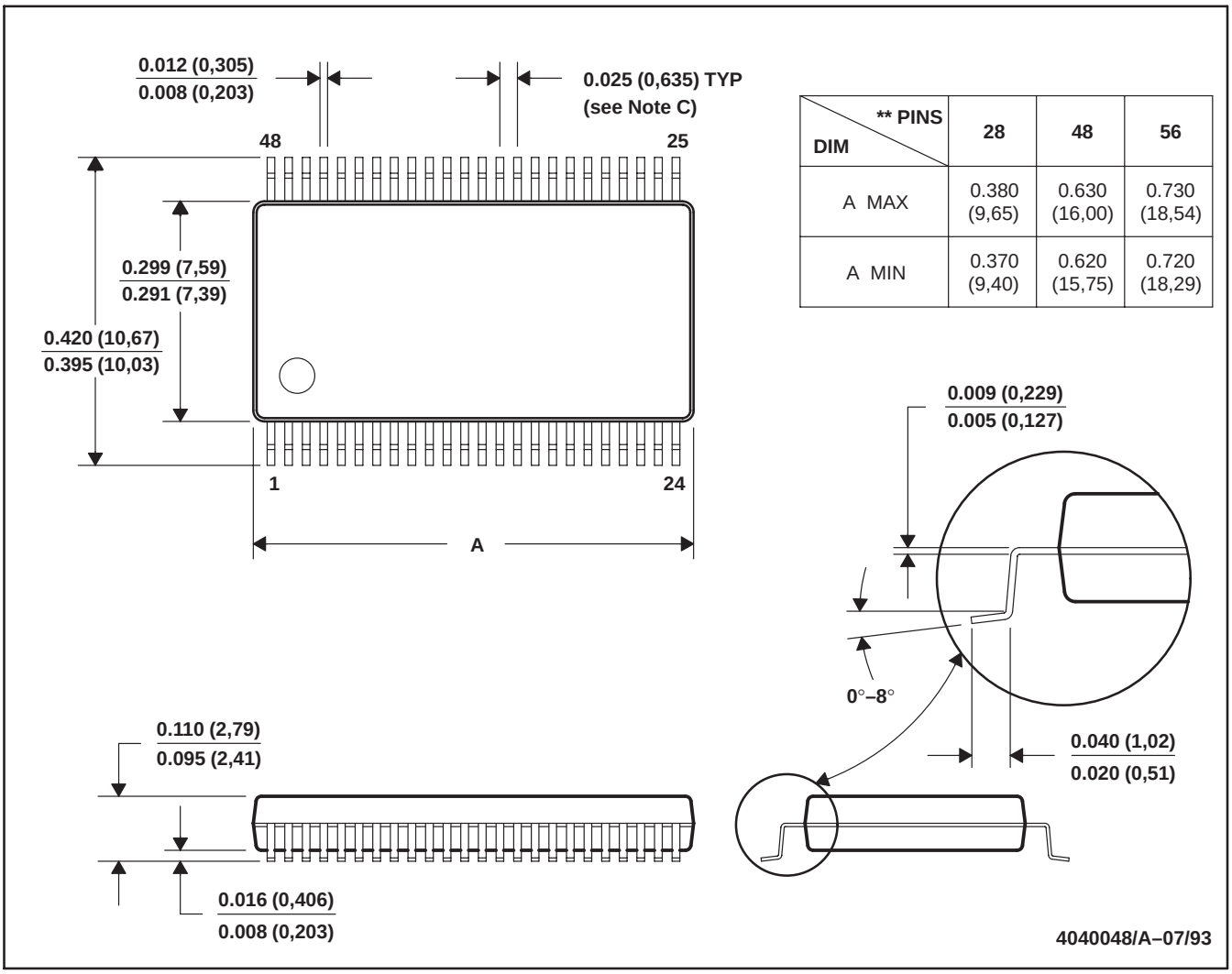
NAME	ALIAS	SUBSYSTEM†	DESCRIPTION	VALUE
R1	Ruv1	VM	External voltage-set resistor	100 kΩ
R2	Ruv2	VM	External voltage-monitor set resistor	270 kΩ
R3	Rrset1	SPN	Retract velocity-limit-set resistor	62 kΩ
R4	Rrset2	SPN	Retract velocity-limit set resistor	100 kΩ
R5	Rsvcm	VCM	VCM current-control resistor	0.33 kΩ
R6	Rcmp	VCM	VCM frequency-compensation resistor	82 kΩ
R7	Rcom2	SPN	Spindle commutation-control resistor	1 MΩ
R8	Rcom1	SPN	Spindle commutation-control resistor	56 kΩ
R9	Rspn	SPN	Spindle speed-regulator compensation resistor	470 kΩ
R10	Rsspn	SPN	Spindle transconductance-control resistor	0.33 Ω
C1	Cuv1	VM	External voltage-set capacitor	1 µF
C2	Cpor	VM	Reset-time-delay capacitor	0.02 µF
C3	CV_{DD}	VM	Charge-pump storage capacitor	0.01 µF
C4	Ccmp2	VCM	VCM frequency-compensation capacitor	120 pF
C5	Ccmp1	VCM	VCM frequency-compensation capacitor	1500 pF
C6	Ccom2	SPN	Spindle commutation-delay capacitor	2000 pF
C7	Ccom1	SPN	Spindle commutation-delay capacitor	0.2 µF
C8	Cspn1	SPN	Spindle-speed-regulator frequency-compensation capacitor	0.68 µF
C9	Cspn2	SPN	Spindle-speed-regulator frequency-compensation capacitor	0.048 µF
C10	$CV_{CC}1$	All	Power-supply bypass capacitor	0.1 µF
C11	$CV_{CC}2$	All	Power-supply bypass capacitor	47 µF
C12	$CV_{CC}3$	All	Power-supply bypass capacitor	0.1 µF
C13	Cret	SPN	Option filter of back-EMF-mode voltage capacitor	1 µF

† SPN = spindle, VCM = voice-coil motor, VM = voltage monitor

MECHANICAL DATA

DL/R-PDSO-G** **PLASTIC SHRINK SMALL-OUTLINE PACKAGE**

48-PIN SHOWN

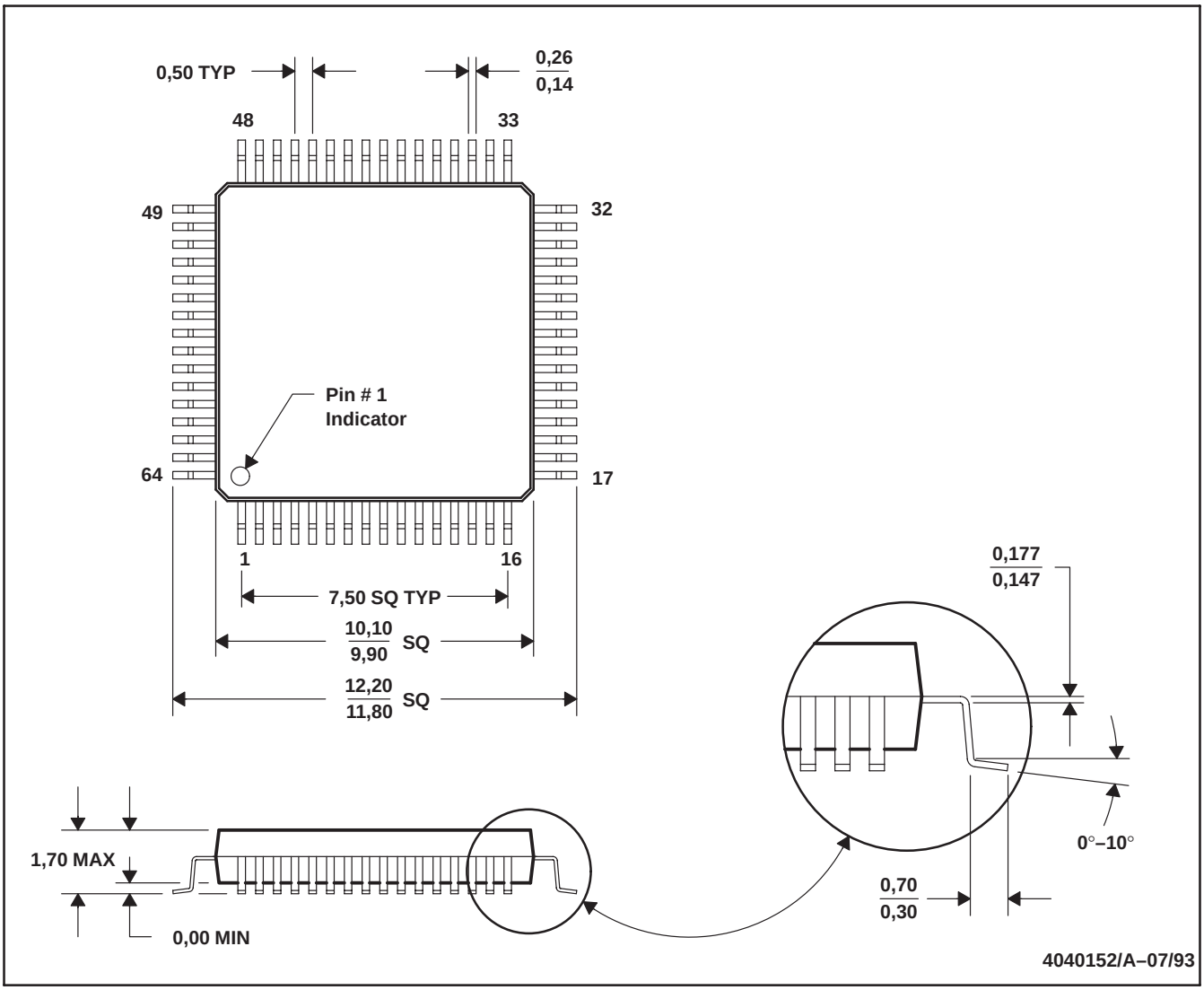


DIM \ ** PINS	28	48	56
A MAX	0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN	0.370 (9,40)	0.620 (15,75)	0.720 (18,29)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads are within 0.0035 (0,089) radius of true postion at maximum material condition.
D. Body dimensions do not include mold flash, protrusion, or gate burr.
E. Mold flash, protrusion, or gate burr shall not exceed 0.015 (0,381).
F. Lead tips coplanar within 0.004 (0,102).
G. Lead length measured from lead top to point 0.010 (0,254) above seating plane.

MECHANICAL DATA

PM/S-PQFP-G64 **PLASTIC QUAD FLAT PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Maximum deviation from coplanarity is 0,08 mm.
D. Body dimensions do not include mold flash or protrusion.

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