



# High-Speed CMOS CrossbarSwitch™ Clocked 4 Port x 4, 4 Port x 8

QS3B441  
QS3B481

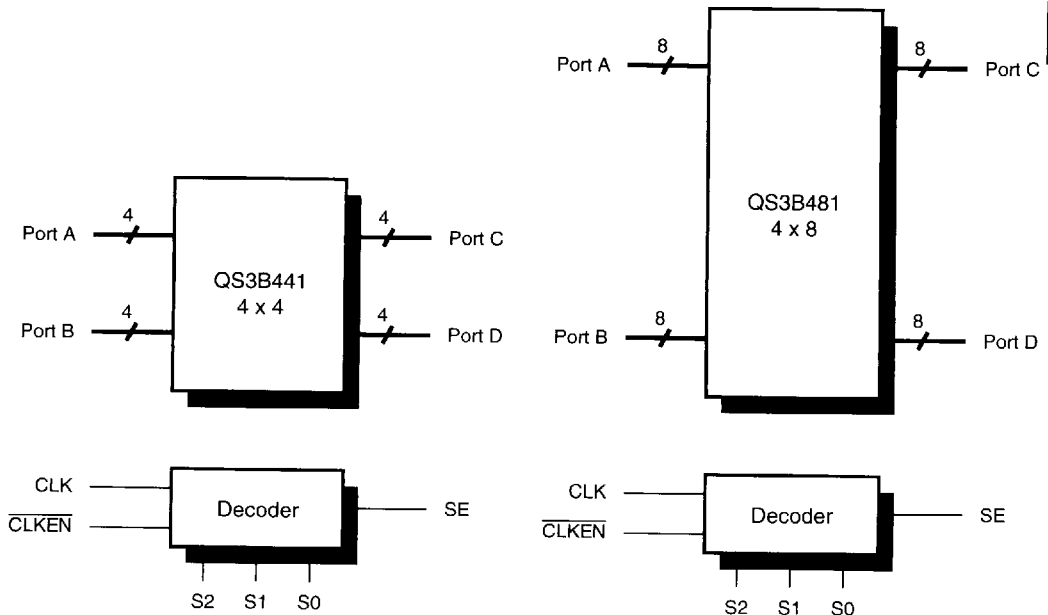
## FEATURES/BENEFITS

- Bi-directional analog or digital switching
- 4 ports of 4 bits (3B441)
- 4 ports of 8 bits (3B481)
- Decoded and registered control signals
- Zero added signal skew
- Overriding Switch Enable disconnects all channels
- Available in 24-pin QSOP (3B441) and 40-pin QVSOP (3B441)
- Low power QCMOS™ Technology
- Zero added ground bounce

## DESCRIPTION

The QS3B441 is a QuickSwitch based crossbar switch with four ports of four bits. The QS3B481 has four ports of eight bits. Each port can connect to any other (see table). Data flow is transparent and bi-directional and requires no direction control. In addition all ports are disconnected when SE (switch enable) is LOW. The QuickSwitch crossbar is ideal for implementing switching protocols in networking systems, data bus order changes, and other multi-way datacommunication applications.

## FUNCTIONAL BLOCK DIAGRAM

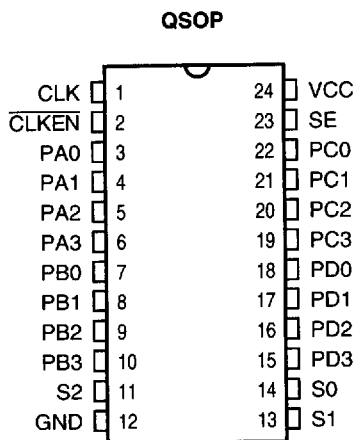


FUNCTION TABLE

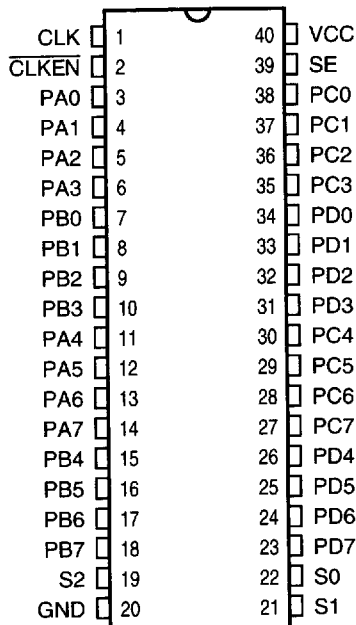
SE	S2	S1	S0	Port A	Port B	Port C	Port D
1	0	0	0	X	Y	X	Y
1	0	0	1	X	X	Y	Y
1	0	1	0	X	Y	Y	X
1	0	1	1	X	X	X	-
1	1	0	0	X	-	X	X
1	1	0	1	-	X	X	X
1	1	1	0	X	X	-	X
1	1	1	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z
0	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z

Note: Selections marked with the same letter (X or Y) indicates ports connected together.

PIN CONFIGURATIONS  
(All Pins Top View)



QVSO



ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground .....	-0.5V to +7.0V
DC Switch Voltage $V_s$ .....	-0.5V to $V_{cc} + 0.3V$
DC Input Voltage $V_{in}$ .....	-0.5V to $V_{cc} + 0.3V$
AC Input Voltage (for a pulse width $\leq 20$ ns) .....	-3.0V
DC Input Diode Current with $V_i < 0$ .....	-20 mA
DC Output Current Max. Sink Current/Pin .....	120 mA
Maximum Power Dissipation .....	0.5 watts
$T_{STG}$ Storage Temperature .....	-65° to +150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to QSI devices that result in functional or reliability type failures.

**CAPACITANCE**

$T_A = 25^\circ\text{C}$ ,  $f = 1\text{ MHz}$ ,  $V_{IN} = 0\text{V}$ ,  $V_{OUT} = 0\text{V}$

Pins	QSOP		QVSOP		Units
	Typ	Max	Typ	Max	
Control Pins	5	7	5	7	pF
QuickSwitch Channels Off	20	—	20	—	pF
QuickSwitch, One to One Channels	40	—	40	—	pF

**Note:** Capacitance is characterized but not tested.

**DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE**

Commercial  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$

Symbol	Parameter	Test Conditions	Min	Typ <sup>(1)</sup>	Max	Unit
$V_{IH}$	Input HIGH Voltage	Guaranteed Logic HIGH for Control Pins	2.0	—	—	V
$V_{IL}$	Input LOW Voltage	Guaranteed Logic LOW for Control Pins	—	—	0.8	V
$ I_{IN} $	Input Leakage Current <sup>(2)</sup>	$0 \leq V_{IN} \leq V_{CC}$	—	—	1	$\mu\text{A}$
$ I_{OZ} $	Off-State Current (Hi-Z) <sup>(2)</sup>	$0 \leq A, B \leq V_{CC}$	—	—	1	$\mu\text{A}$
$R_{ON}$	Switch On Resistance	$V_{CC} = \text{Min.}, V_{IN} = 0.0\text{V}, I_{ON} = 30\text{ mA}$ $V_{CC} = \text{Min.}, V_{IN} = 2.4\text{V}, I_{ON} = 15\text{ mA}$ $V_{CC} = \text{Min.}, V_{IN} = 4.0\text{V}, I_{ON} = 15\text{ mA}$	—	10 15 27	—	$\Omega$

**Notes:**

1. Typical values indicate  $V_{CC} = 5.0\text{V}$  and  $T_A = 25^\circ\text{C}$ .
2. Measured by voltage drop between A and B pin at indicated current through the switch. ON resistance is determined by the lower of the voltages on the two (A, B) pins.

**POWER SUPPLY CHARACTERISTICS**

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Max	Unit
$I_{CCQ}$	Quiescent Power Supply Current <sup>(4)</sup>	$V_{CC} = \text{Max.}, V_{IN} = \text{GND or } V_{CC}, f = 0$	300	$\mu\text{A}$
$I_{CCQ}$	Quiescent Power Supply Current <sup>(5)</sup>	$V_{CC} = \text{Max.}, V_{IN} = \text{GND or } V_{CC}, f = 0$	600	$\mu\text{A}$
$\Delta I_{CC}$	Power Supply Current <sup>(2)</sup> per Input HIGH	$V_{CC} = \text{Max.}, V_{IN} = 3.4\text{V}, f = 0$ per Control Input	2.5	$\text{mA}$
$Q_{CCD}$	Dynamic Power Supply Current per MHz <sup>(3)</sup>	$V_{CC} = \text{Max.}, A \text{ and } B \text{ Pins Open, Control Inputs Toggling @ } 50\% \text{ Duty Cycle}$	1.0	$\text{mA/MHz}$

**Notes:**

1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per TTL driven input ( $V_{IN} = 3.4\text{V}$ , control inputs only). A and B pins do not contribute to  $I_{CC}$ .
3. This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The A and B inputs generate no significant AC or DC currents as they transition. This parameter is guaranteed by design, but not tested.
4.  $I_{CCQ}$  for QS3B441.
5.  $I_{CCQ}$  for QS3B481.

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## QS3B441, QS3B481 ADVANCE INFORMATION

### SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$

$C_{LOAD} = 50\text{ pF}$ ,  $R_{LOAD} = 500\Omega$  unless otherwise noted.

Symbol	Description	Min	Typ	Max	Unit
t <sub>PLH</sub> t <sub>PHL</sub>	Single Channel Port Propagation Delay <sup>(3)</sup>	—	1.75	—	ns
t <sub>SCS</sub>	Control S Inputs to CLK Setup Time	3	—	—	ns
t <sub>HCS</sub>	Control S Inputs to CLK Hold Time	0	—	—	ns
t <sub>SEC</sub>	$\overline{\text{CLKEN}}$ to CLK Setup Time <sup>(2)</sup>	3	—	—	ns
t <sub>HEC</sub>	$\overline{\text{CLKEN}}$ to CLK Setup Time <sup>(2)</sup>	0	—	—	ns
t <sub>w</sub>	Clock Pulse Width (HIGH)	4	—	—	ns
t <sub>PZL</sub> t <sub>PZH</sub>	Asynchronous Enable to Turn On Delay <sup>(1)</sup>	1.5	—	7.0	ns
t <sub>PLZ</sub> t <sub>PHZ</sub>	Asynchronous Enable to Turn Off Delay <sup>(1,2)</sup>	1.5	—	6.5	ns
I <sub>QCil</sub>	Charge Injection <sup>(4,5)</sup>	—	1.5	—	pC
t <sub>CSO</sub>	CLK to State Change	—	—	7.0	ns

**Notes:**

1. See Test Circuit and Waveforms. Minimums guaranteed but not tested.
2. This parameter is guaranteed by design but not tested.
3. The bus switch contributes no propagation delay other than the RC delay of the ON resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 50 pF. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
4. Measured at switch turn off, A to C, load = 50 pF in parallel with 10 meg scope probe,  $V_{IN}$  at A = 0.0V.
5. This parameter is characterized but not production tested.

### TIMING DIAGRAM

