

SN54F109, SN74F109 DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

D2932, MARCH 1987

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These devices contain two independent J-K positive-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the J and K input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by grounding K and trying J high. They also can perform as D-type flip-flops if J and K are tied together.

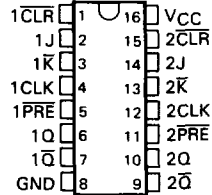
The SN54F109 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74F109 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(EACH FLIP-FLOP)

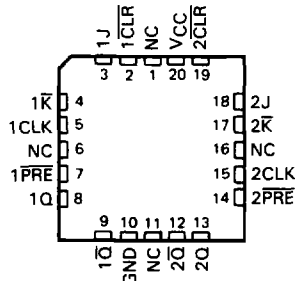
INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q ₀	Q̄ ₀
H	H	↑	H	H	H	L
H	H	L	X	X	Q ₀	Q̄ ₀

*The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH}. Furthermore, this configuration is nonstable; that is, it will not persist when either Preset or Clear returns to its inactive (high) level.

SN54F109 . . . J PACKAGE
SN74F109 . . . D OR N PACKAGE
(TOP VIEW)

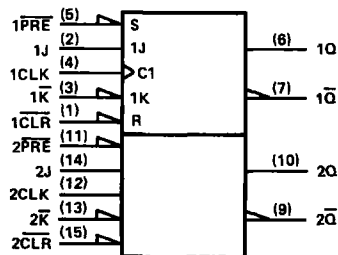


SN54F109 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, and N packages.

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Data Sheets

SN54F109, SN74F109
DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS
WITH CLEAR AND PRESET

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	-0.5 V to 7 V
Input voltage [†]	-1.2 V to 7 V
Input current [†]	-30 mA to 5 mA
Voltage applied to any output in the high state	-0.5 V to V_{CC}
Current into any output in the low state	40 mA
Operating free-air temperature range: SN54F109	-55°C to 125°C
SN74F109	0°C to 70°C
Storage temperature range	-65°C to 150°C

[†]The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F109			SN74F109			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			-18			-18	mA
I_{OH}	High-level output current			-1			-1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54F109			SN74F109			UNIT
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IK}	$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$			-1.2			-1.2	V
V_{OH} [¶]	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -1\text{ mA}$	2.5	3.4		2.5	3.4		V
V_{OL}	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 20\text{ mA}$		0.30	0.5		0.30	0.5	V
I_I	$V_{CC} = 5.5\text{ V}$, $V_I = 7\text{ V}$			0.1			0.1	mA
I_{IH}	$V_{CC} = 5.5\text{ V}$, $V_I = 2.7\text{ V}$			20			20	μA
I_{IL}	J, \bar{K} , CLK	$V_{CC} = 5.5\text{ V}$, $V_I = 0.5\text{ V}$			-0.6			mA
	\bar{PRE} or \bar{CLR}				-1.8			
I_{OS} [§]	$V_{CC} = 5.5\text{ V}$, $V_O = 0$	-60		-150	-60		-150	mA
I_{CC}	$V_{CC} = 5.5\text{ V}$, See Note 1		11.7	17		11.7	17	mA

[‡] All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

[§] Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

[¶] For the SN74F109 at $V_{CC} = 4.75\text{ V}$ and $I_{OH} = -1\text{ mA}$, $V_{OH\text{ min}} = 2.7\text{ V}$.

NOTE 1: I_{CC} measured with J, \bar{K} , CLK, and \bar{PRE} grounded, then with J, \bar{K} , CLK, and \bar{CLR} .

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		$V_{CC} = 5\text{ V},$ $T_A = 25^\circ\text{C}$		$V_{CC} = 4.5\text{ V to } 5.5\text{ V},$ $T_A = \text{MIN to MAX}^\dagger$				UNIT
		'F109		SN54F109		SN74F109		
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	100	0	70	0	90	MHz
t_{su}	Setup time before CLK \uparrow	Data high	3	3	3	3		ns
		Data low	3	3	3	3		
t_{h}	Hold time after CLK \uparrow	Data high	1	1	1	1		ns
		Data low	1	1	1	1		
t_{w}	Pulse duration	CLK high, $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low	4	4	4	4		ns
		CLK low	5	5	5	5		
t_{su}	Inactive-state setup time before CLK \uparrow	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ to CLK	2	2	2	2		ns

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5\text{ V},$ $C_L = 50\text{ pF},$ $R_L = 500\ \Omega,$ $T_A = 25^\circ\text{C}$			$V_{CC} = 4.5\text{ V to } 5.5\text{ V},$ $C_L = 50\text{ pF},$ $R_L = 500\ \Omega,$ $T_A = \text{MIN to MAX}^\dagger$				UNIT
			'F109			SN54F109		SN74F109		
			MIN	TYP ‡	MAX	MIN	MAX	MIN	MAX	
f_{max}			100	150	70		90		MHz	
t_{PLH}	CLK	Q or \overline{Q}	3	4.9	7	3	9	3	8	ns
t_{PHL}			3.6	5.8	8	3.6	10.5	3.6	9.2	
t_{PLH}	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or \overline{Q}	2.4	4.8	7	2.4	9	2.4	8	ns
t_{PHL}			2.7	6.6	9	2.7	11.5	2.7	10.5	

† For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.

‡ All typical values are at $V_{CC} = 5\text{ V}, T_A = 25^\circ\text{C}$.

NOTE 2: See General Information for load circuits and waveforms.

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Data Sheets