RC4444
4 x 4 x 2 Balanced Switching Crosspoint Array

Description

The RC4444 is a monolithic dielectrically isolated crosspoint array arranged into a 4 x 4 x 2 matrix. The primary application is for balanced switching of 600Ω transmission lines. The ring and tip are selected by selective biasing of the P+ and P- gate.

Designed to replace reed relays in telephone switchboards, it does not require a constant gate drive to keep the SCR in the "ON" condition. It is several orders faster, with no bouncing, and has a much longer operating life than its mechanical counterpart.

The 16 SCR pairs with the gating system are packaged in a 24-pin dual in-line package.

Features

- Low bi-directional R_{ON}
- High R_{OFF}
- Excellent matching of gates
- Low capacitance
- High rate firing
- Predictable holding current

Block Diagram

Linear

65-2413

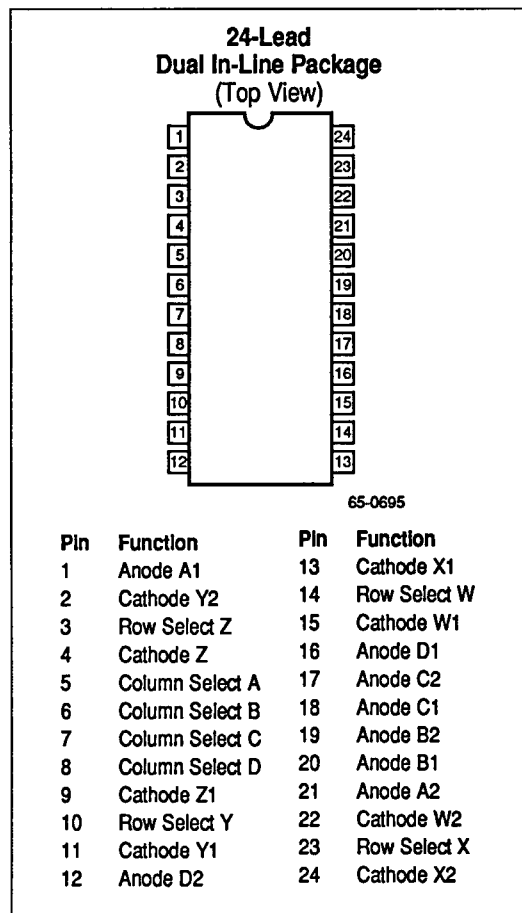# RC4444
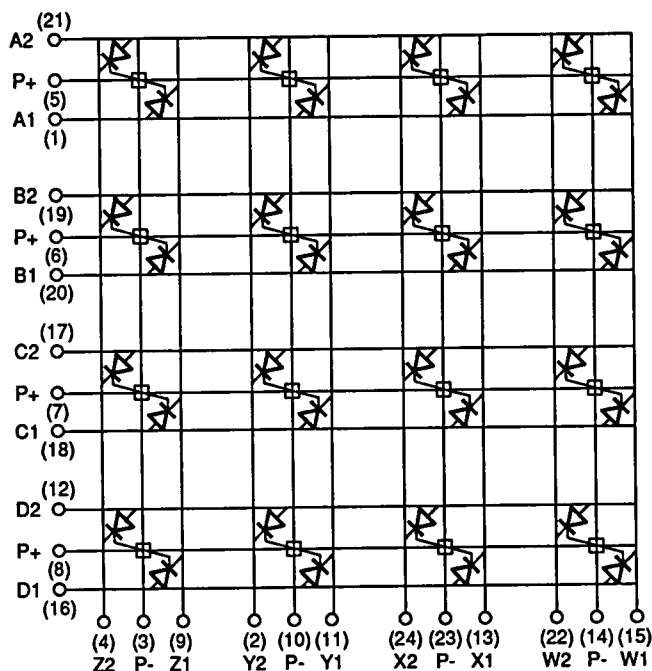
Absolute Maximum Ratings

Operating Voltage ....+25V
Operating Current per Crosspoint ....100 mA
Storage Temperature Range ....-65°C to +150°C
Operating Temperature Range ....0°C to +70°C
Lead Soldering Temperature ....+300°C
    (60 sec)

Notes: 1. Maximum voltage from anode to cathode.

Thermal Characteristics

	24-Lead Plastic DIP	24-Lead Ceramic DIP
Max. Junction Temp.	+125°C	+175°C
Max. P_D T_A < 50°C	555 mW	1042 mW
Therm. Res θ_{JC}	—	60°C/W
Therm. Res. θ_{JA}	135°C/W	120°C/W
For T_A > 50°C Derate at	7.41 mW/°C	8.33 mW/°C

Connection Information

24-Lead
Dual In-Line Package
(Top View)

65-0695

Pin	Function	Pin	Function
1	Anode A1	13	Cathode X1
2	Cathode Y2	14	Row Select W
3	Row Select Z	15	Cathode W1
4	Cathode Z	16	Anode D1
5	Column Select A	17	Anode C2
6	Column Select B	18	Anode C1
7	Column Select C	19	Anode B2
8	Column Select D	20	Anode B1
9	Cathode Z1	21	Anode A2
10	Row Select Y	22	Cathode W2
11	Cathode Y1	23	Row Select X
12	Anode D2	24	Cathode X2

Ordering Information

Part Number	Package	Operating Temperature Range
RC4444N	N	0°C to +70°C
RC4444D	D	0°C to +70°C

Notes:
N = 24-lead 600 wide plastic DIP
D = 24-Lead 600 wide Ceramic DIP

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Electrical Characteristics

(0°C ≤ T_A ≤ +70°C unless otherwise specified)

Parameters	Test Conditions	Min	Typ	Max	Units
Anode-Cathode Breakdown Voltage	I_{AK} = 25 µA	25			V
Cathode-Anode Breakdown Voltage	I_{AK} = 25 µA	25			V
Base-Cathode Breakdown Voltage	I_{BK} = 25 µA	25			V
Cathode-Base Breakdown Voltage	I_{KB} = 25 µA	25			V
Base-Emitter Breakdown Voltage	I_{BE} = 25 µA	25			V
Emitter-Cathode Breakdown Voltage	I_{EK} = 25 µA	25			V
OFF State Resistance	V_{AK} = 10V	100			MΩ
Dynamic ON Resistance	Center Current = 10 mA	4.0		12	Ω
	Center Current = 20 mA	2.0		10	
Holding Current		0.9		3.8	mA
Enable Current	V_{BE} = 1.5V (Fig. 2)	4.0			mA
Anode-Cathode ON Voltage	I_{AK} = 10 mA			1.0	V
	I_{AK} = 20 mA			1.1	
Gate Sharing Current	Under Select Conditions	0.8		1.25	mA/mA
Ratio at Cathodes	with Anodes Open (fig. 1)	0.8		1.25	mA/mA
Inhibit Voltage	V_B = 3.0V (Fig. 3)			0.3	V
Inhibit Current	V_B = 3.0V (Fig. 3)			0.1	mA
OFF State Capacitance	V_{AK} = 0V			2.0	pF
Turn-ON Time	(Fig. 5)			1.0	µs
Minimum Voltage Ramp	Which Could Fire the SCR Under Transient Conditions (Figure 5)	800			V/µs

RC4444

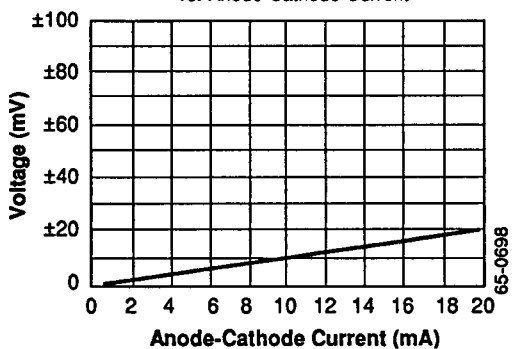## Typical Performance Characteristics

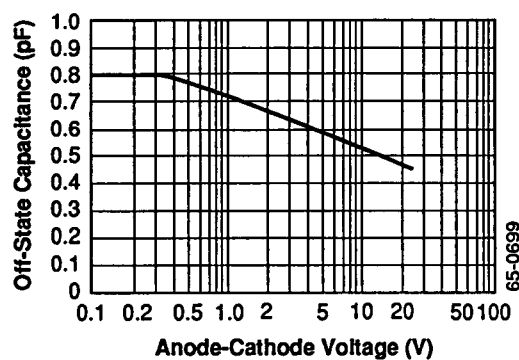Holding Current vs. Ambient Temperature
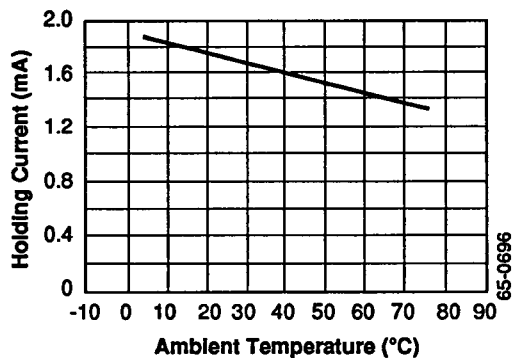
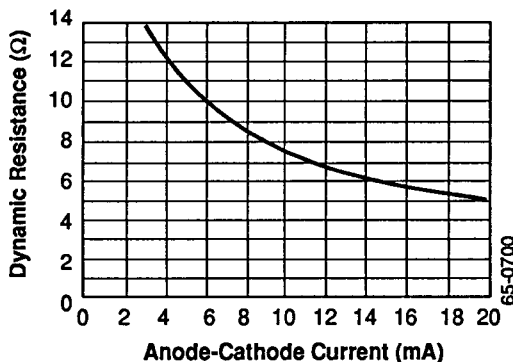Anode-Cathode on Voltage vs. Current and Temperature
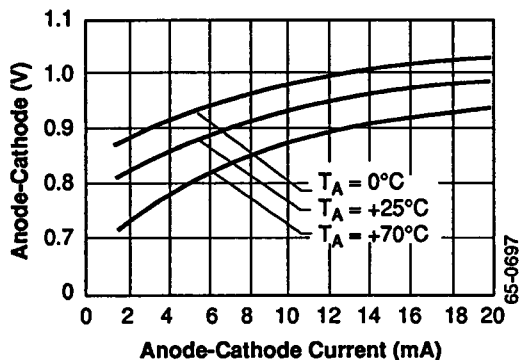
Difference In Anode-Cathode on Voltage (Between Associate Pairs of SCRs) vs. Anode-Cathode Current
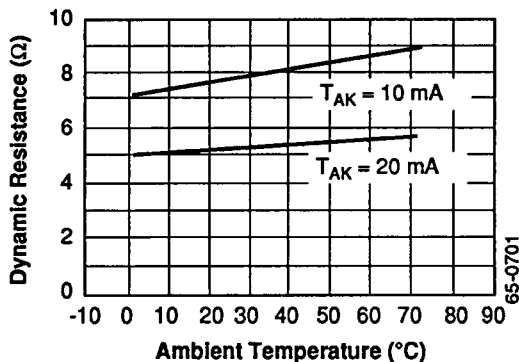

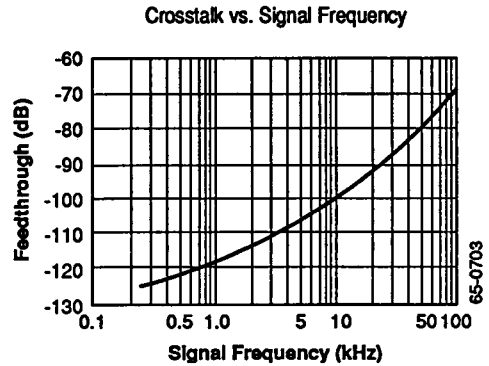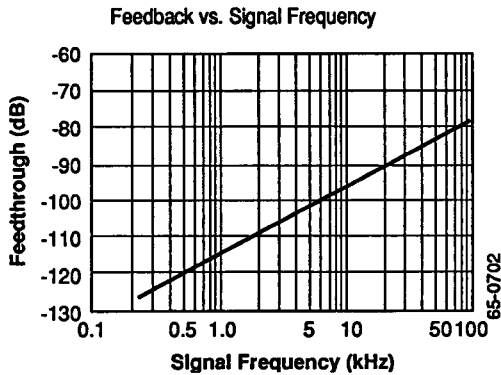Off-site Capacitance vs. Anode-Cathode Voltage

Dynamic on Resistance vs. Anode-Cathode Current

Dynamic on Resistance vs. Ambient Temperature

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Typical Performance Characteristics (Continued)

Feedback vs. Signal Frequency

Crosstalk vs. Signal Frequency

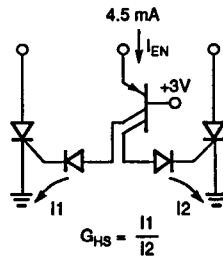## Test Circuits

$$G_{HS} = \frac{I1}{I2}$$

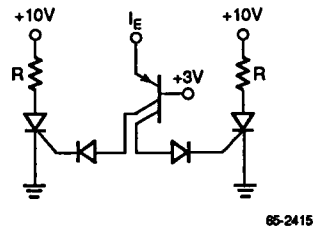Figure 1. Test Circuit for Gate Sharing Current Ratio

Figure 2. Enable Current (Both SCRs Must Turn On)
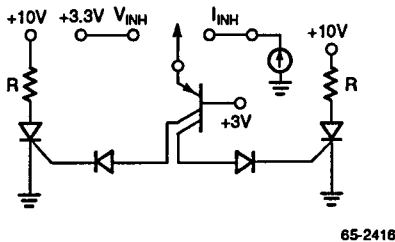

Figure 3. Inhibit Voltage and Inhibit Current (Both SCRs Must Remain Off)
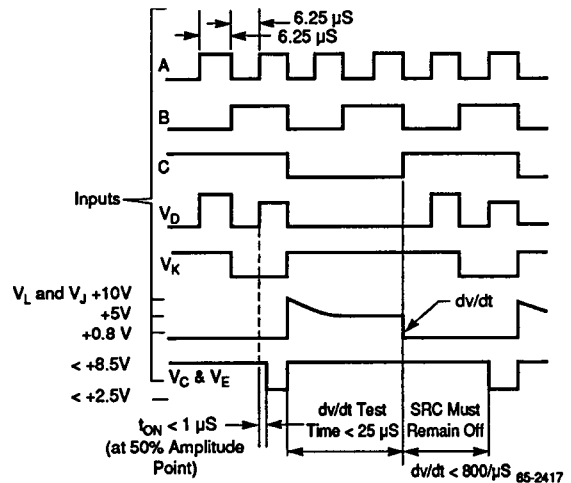
Figure 4. Test Waveforms for dv/dt and t_{on}

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Test Circuits (Continued)

Figure 5. Test Circuit for dv/dt and t_{ON}

65-2418

$T_A = +25°C$, $V_I = 12$ dBm, Crosspoints Off
Feedthrough = $20 \, Log_{10} \, (V_O/V_I)$

65-2049

Figure 6. Test Circuit for Feedthrough vs.
Frequency

$T_A = +25°C$, $V_I = 12$ dBm, Crosspoinst On
Feedthrough = $20 \, Log_{10} \, (V_{O2}/V_{O1})$

65-2050

Figure 7. Test Circuit for Crosstalk vs.
Frequency

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Typical Applications

The RC4444 crosspoint switch is designed to provide a low-loss analog switching element for telephony signals. It can be addressed and cont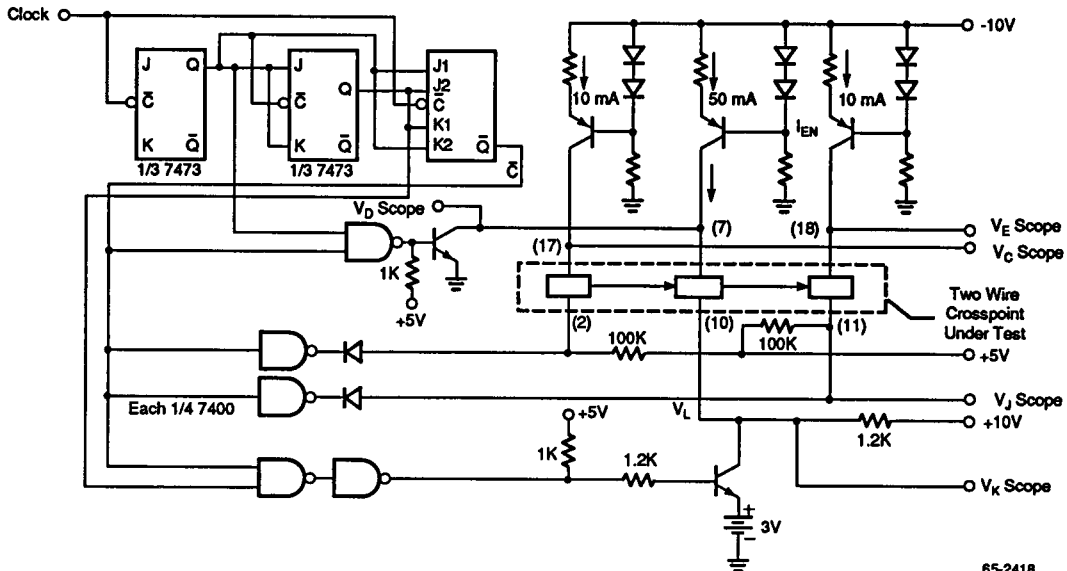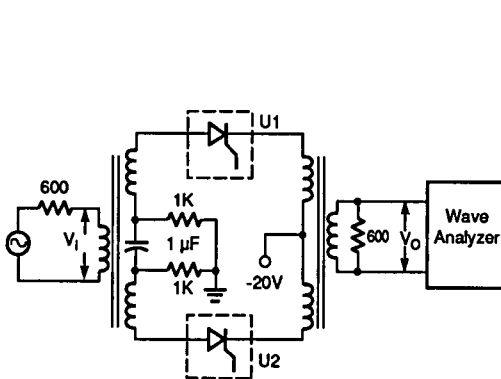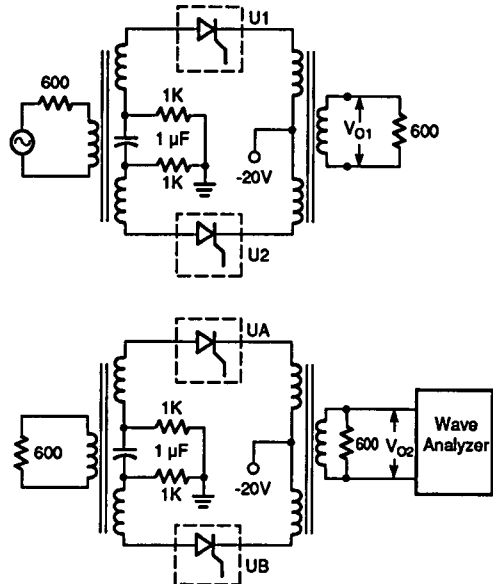rolled from standard binary decoders and is CMOS compatible. With proper system organization, the RC4444 can significantly reduce the size and cost of existing crosspoint matrices.

Signal Path Considerations

The RC4444 is a balanced 4 x 4 2-wire crosspoint array. It is ideal for balanced transmission systems, but may be applied effectively in a number of single ended applications. Multiple chips may be interconnected to form larger crosspoint arrays. The major design constraint in using SCR crosspoints is that a forward DC current must be maintained through the SCR to retain an AC signal path. This requires that each subscriber-input to the array be capable of sourcing DC current as well as its AC signal. With each subscriber acting as a DC source, each trunk output then acts as a current sink. The instrument-to-trunk connection in Figure 8 shows this configuration. However, with each subscriber acting as a DC source, some method of interconnecting them without a trunk must be provided. Such a local or intercom termination is shown in Figure 9. Here both subscribers source DC current and exchange AC signals. The central current sink accepts current from both subscribers while the high output impedance of the current sink does not disturb the system.

These configurations are system compatible. The DC current restriction is not a restriction in the design of an efficient crosspoint array. Because of the current sink terminations, a signal path may use differing numbers of crosspoints in any connection or in two sides of the same connection further relaxing restrictions in array design.

Figure 10 demonstrates circuit operation. S1, S2 and S3 are open. The Crosspoint SCRs are off as they have not gate drive or DC current path through S1. By closing S2 and S3, gate drive is provided, but the SCRs still remain off as there is no DC current path to hold them on. Close S1 and the circuit is enabled, but with S2 and S3 off there is still no signal path. Closing S2 and S3 with S1 closed — current is injected into both gates and they switch on. DC current through R_L splits around the center-tapped winding and flows through each SCR, back through the lower winding and through S1 to ground. If S2 and S3 are opened, that current path still remains and the SCRs remain on. If an AC signal is injected at either G1 or G2, it will be transmitted to the other signal port with negligible loss in the SCRs. To disconnect the AC signal path, the SCRs must be commutated off. By opening S1 the DC current path is interrupted and the SCRs switch off. The AC signal path is disconnected. With S1 closed, the circuit is enabled and may be addressed again from S2 and S3. This circuit demonstrates a balanced transmission configuration. The transmission characteristics of the SCRs simulate a relay contact in that the AC signal does not incur a contact voltage drop across the crosspoint. The memory characteristics of the crosspoint are demonstrated by the selective application of S1, S2, and S3.

The selection of R_L is governed by the power supply voltage and the desired DC current. If 10 mA is to flow through each SCR then R_L must pass 20 mA. Thus, $(+V_S - V_{AK})/R_L = 20$ mA. The selection of Rp is governed by the characteristics for crosspoint turn on. Adequate enable current must be injected into the column select and Rp should drop at least 1.5V. The PNP transistor has a typical gain of one. Thus, Rp should pass at least 2 mA to provide 4 mA column select current.

Linear

RC4444

Addressing Considerations

The RC4444 crosspoint switch is addressed by selecting and turning on the PNP transistor that controls the SCR pair desired. The drive requirements of the RC4444 can be met with standard CMOS outputs. A particular crosspoint is addressed by putting a logical "1" on the emitter and a logical "0" on the base of the appropriate transistor. A resistor in the base circuit of the transistor is required to limit the current and must also drop 1.5V to assure forward bias of the two diodes in the collector circuits.

The gate current required for SCR turn on is 1 mA typically. CMOS one-of-n decoders are available that provide both active high and active low outputs and are well suited for standard addressing organizations. The major design constraint in organizing the addressing structure is that any signal path which is to be addressed must create a DC path from a source to a sink. If that path requires two crosspoints, they must be addressed simultaneously. Of course, once the path is selected, the addressing hardware is free to initiate other signal paths. To meet the DC path requirement, crosspoint arrays should be designed in block such that any give DC path required only one crosspoint per block. A signal path, however, may still use two crosspoints in the same block by sequentially addressing two DC paths to the same terminator. For example, the left or right pairs of crosspoints in Figure 9 must be addressed simultaneously but the left pair may be addressed in sequence after addressing the right pair. This is not a difficult constraint to meet and it does not require unnecessary addressing hardware.
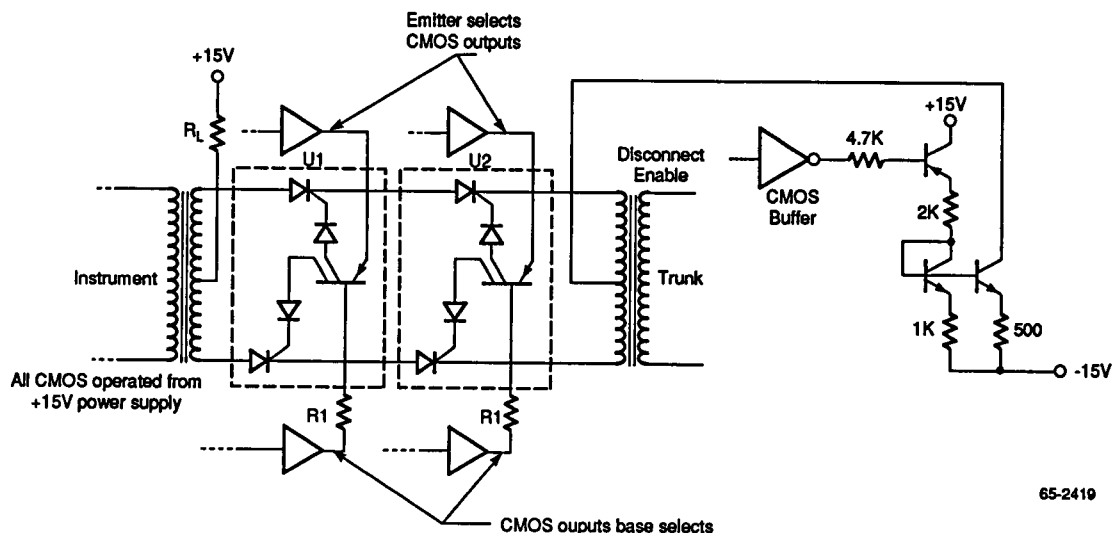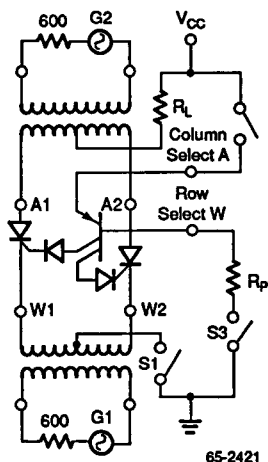

Figure 8. Instrument-to-Trunk Connection
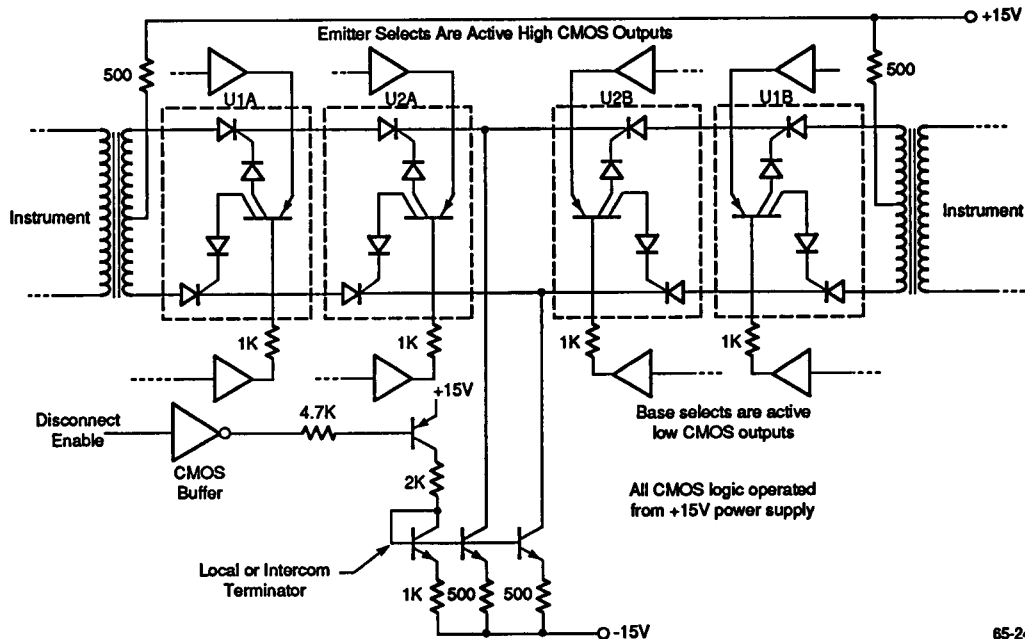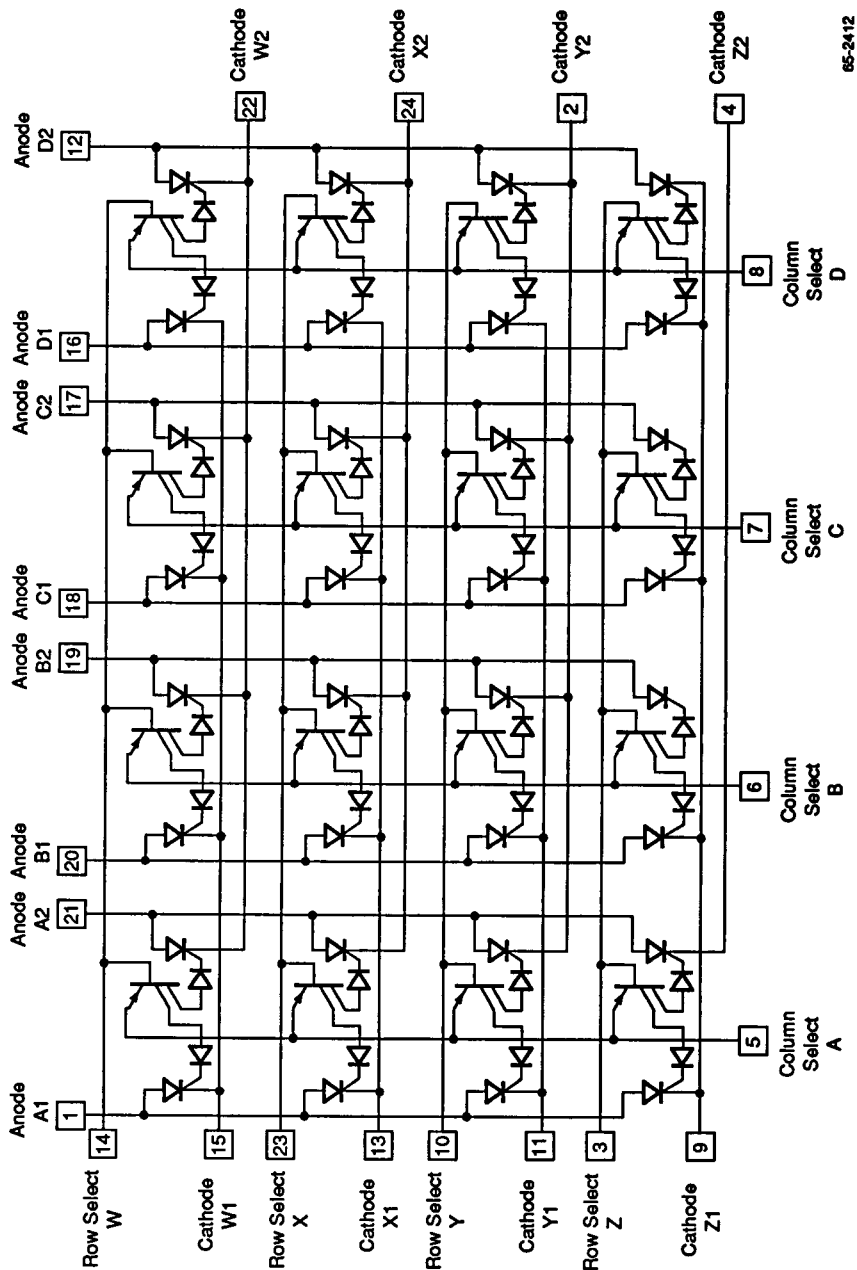
Figure 9. Typical Instrument-to-Instrument Connection

S1	S2	S3	Line Condition
On	X	Off	Enabled, Not Connected
On	Off	X	Enabled, Not Connected
On	On	On	Addressed and Connected
On	X	X	G1 Connected to G2
Off	X	X	Disconnected

X = Don't Care

Figure 10. Crosspoint Operation Demonstration Circuit

RC4444

Simplified Schematic Diagram

65-2412