- **Free-Running CLKA and CLKB May Be Asynchronous or Coincident**
- **Two Independent 64 × 36 Clocked FIFOs Buffering Data in Opposite Directions**
- **Mailbox Bypass Register for Each FIFO**
- **Dynamic Port B Bus Sizing of 36 Bits (Long Word), 18 Bits (Word), and 9 Bits (Byte)**
- **Selection of Big- or Little-Endian Format for Word and Byte Bus Sizes**
- **Three Modes of Byte Order Swapping on Port B**
- **Almost Full and Almost Empty Flags**
- **Microprocessor Interface Control Logic**
- **$\overline{\text{EFA}}$, $\overline{\text{FFA}}$, $\overline{\text{AEA}}$, and $\overline{\text{AFA}}$ Flags Synchronized by CLKA**
- **$\overline{\text{EFB}}$, $\overline{\text{FFB}}$, $\overline{\text{AEB}}$, and $\overline{\text{AFB}}$ Flags Synchronized by CLKB**
- **Passive Parity Checking on Each Port**
- **Parity Generation Can Be Selected for Each Port**
- **Low-Power Advanced BiCMOS Technology**
- **Supports Clock Frequencies up to 67 MHz**
- **Fast Access Times of 10 ns**
- **Available in 132-Pin Quad Flatpack (PQ) or Space-Saving 120-Pin Shrink Quad Flatpack (PCB)**

## description

The SN74ABT7815 is a high-speed, low-power BiCMOS bidirectional clocked FIFO memory. It supports clock frequencies up to 67 MHz and has read access times as fast as 10 ns. Two independent 64 × 36 dual-port SRAM FIFOs on board the chip buffer data in opposite directions. Each FIFO has flags to indicate empty and full conditions and two programmable flags (almost full and almost empty) to indicate when a selected number of words is stored in memory. FIFO data on port B may be input and output in 36-bit, 18-bit, and 9-bit formats with a choice of big- or little-endian configurations. Three modes of byte order swapping are possible with any bus size selection. Communication between each port may bypass the FIFOs via two 36-bit mailbox registers. Each mailbox register has a flag to signal when new mail has been stored. Parity is checked passively on each port and may be ignored if not desired. Parity generation can be selected for data read from each port.

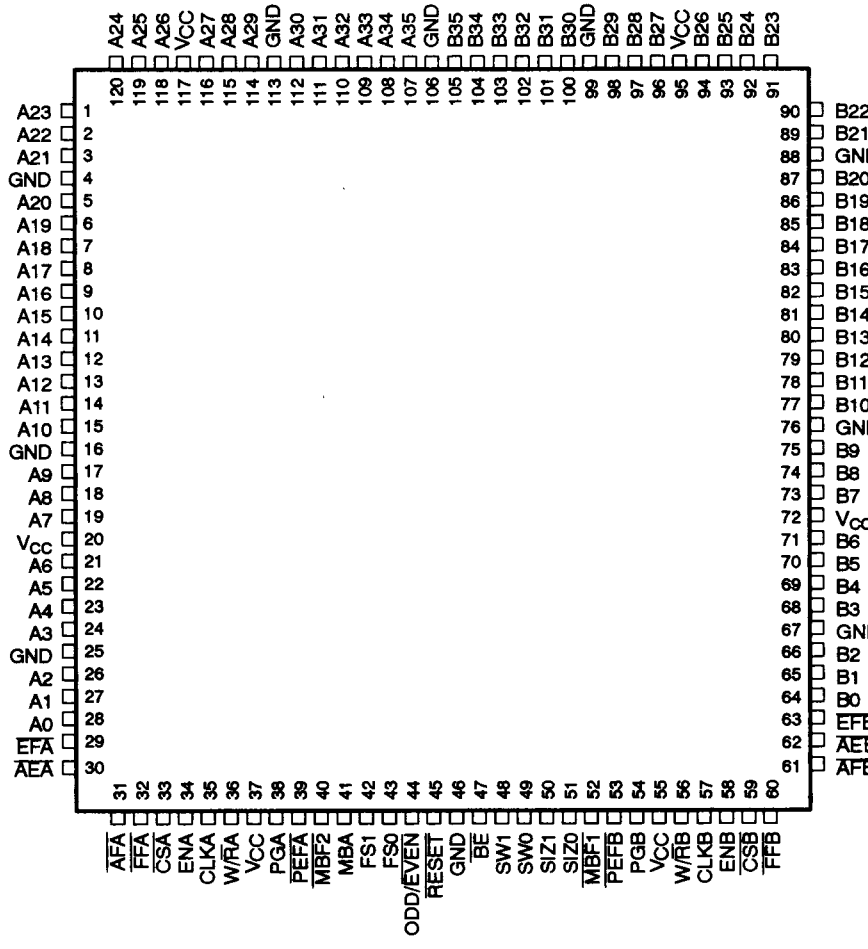
The SN74ABT7815 is a clocked FIFO, which means each port employs a synchronous interface. All data transfers through a port are gated to the low-to-high transition of a continuous (free-running) port clock by enable signals. The continuous clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple bidirectional interface between microprocessors and/or buses controlled by a synchronous interface.

The full flag and almost full flag of a FIFO are two-stage synchronized to the port clock that writes data to its array. The empty flag and almost empty flag of a FIFO are two-stage synchronized to the port clock that reads data from its array.

PRODUCT PREVIEW

PRODUCT PREVIEW

**PCB PACKAGE**
**(TOP VIEW)**



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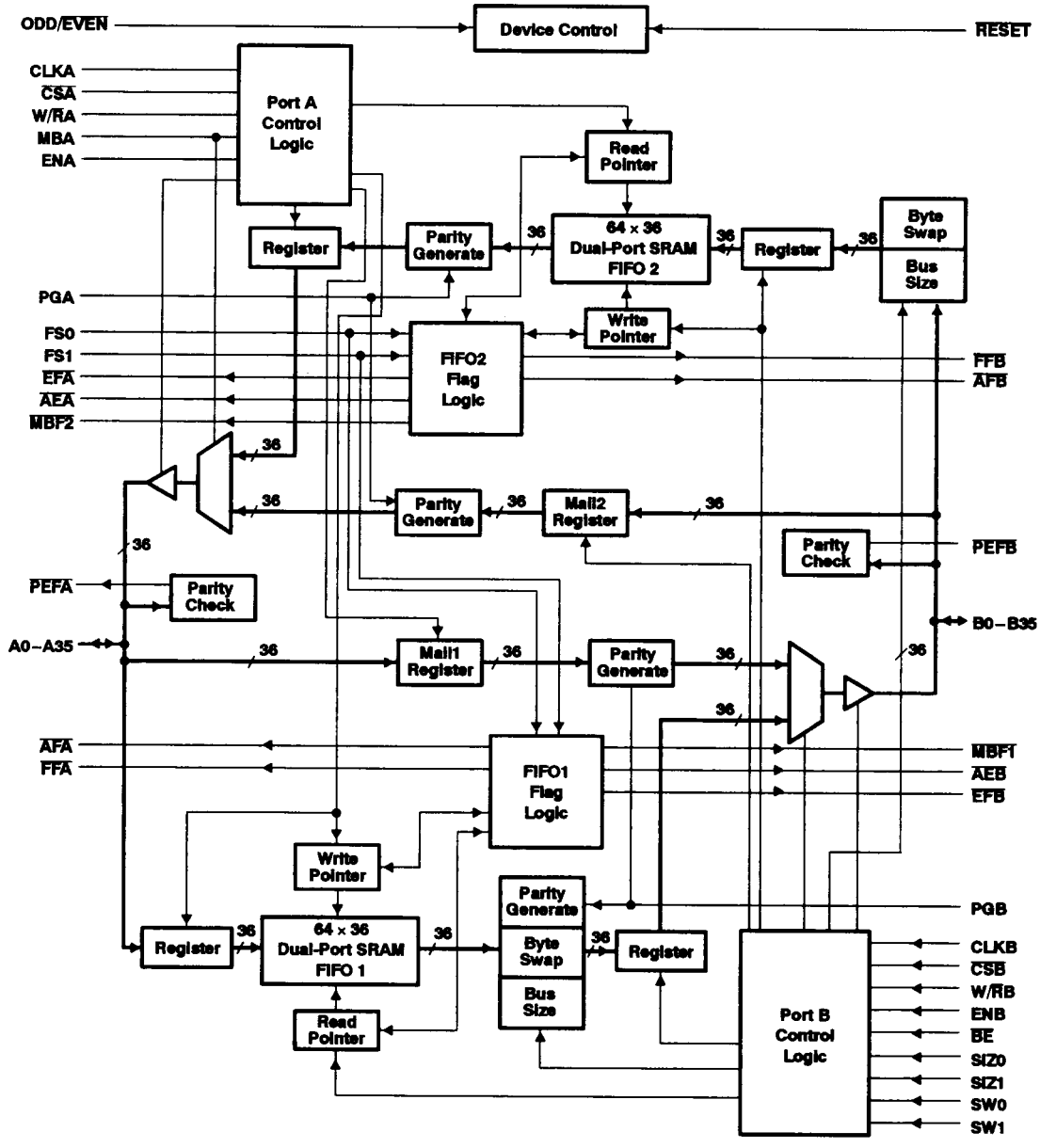
## functional block diagram




PRODUCT PREVIEW

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## Terminal Functions

| PIN NAME | I/O | DESCRIPTION |
|---|---|---|
| A0–A35 | I/O | Port A data. 36-bit bidirectional data port for side A. |
| $\overline{AEA}$ | O | FIFO2 almost empty flag. $\overline{AEA}$ is synchronous to CLKA and is low when the number of 36-bit long words in FIFO2 is less than or equal to the selected offset value. |
| $\overline{AEB}$ | O | FIFO1 almost empty flag. $\overline{AEB}$ is synchronous to CLKB and is low when the number of 36-bit long words in FIFO1 is less than or equal to the selected offset value. |
| $\overline{AFA}$ | O | FIFO1 almost full flag. $\overline{AFA}$ is synchronous to CLKA and is low when the number of 36-bit empty locations in FIFO1 is less than or equal to the selected offset value. |
| $\overline{AFB}$ | O | FIFO2 almost full flag. $\overline{AFB}$ is synchronous to CLKB and is low when the number of 36-bit empty locations in FIFO2 is less than or equal to the selected offset value. |
| B0–B35 | I/O | Port B data. 36-bit bidirectional data port for side B. |
| $\overline{BE}$ | I | Big-endian select. Selects the bytes on port B for use with byte or word data transfers. A low on $\overline{BE}$ selects the most significant bytes of B0–B35 for use, and a high selects the least significant bytes. |
| CLKA | I | Port A clock. CLKA is a continuous clock that synchronizes all data transfers through port A and may be asynchronous or coincident to CLKB. $\overline{EFA}$, $\overline{FFA}$, $\overline{AFA}$, and $\overline{AEA}$ are all synchronous to the low-to-high transition of CLKA. |
| CLKB | I | Port B clock. CLKB is a continuous clock that synchronizes all data transfers through port B and may be asynchronous or coincident to CLKA. Port B byte swapping and data port sizing operations are also synchronous to the low-to-high transition of CLKB. $\overline{EFB}$, $\overline{FFB}$, $\overline{AFB}$, and $\overline{AEB}$ are synchronous to the low-to-high transition of CLKB. |
| $\overline{CSA}$ | I | Port A chip select. $\overline{CSA}$ must be low to enable a low-to-high transition of CLKA to read or write data on port A. The A0–A35 outputs are in the high-impedance state when $\overline{CSA}$ is high. |
| $\overline{CSB}$ | I | Port B chip select. $\overline{CSB}$ must be low to enable a low-to-high transition of CLKB to read or write data on port B. The B0–B35 outputs are in the high-impedance state when $\overline{CSB}$ is high. |
| $\overline{EFA}$ | O | FIFO2 empty flag. $\overline{EFA}$ is synchronized to the low-to-high transition of CLKA. When $\overline{EFA}$ is low, FIFO2 is empty, and reads are disabled. $\overline{EFA}$ is forced low when FIFO2 is reset and goes high on the second low-to-high transition of CLKA after data is loaded to empty memory. |
| $\overline{EFB}$ | O | FIFO1 empty flag. $\overline{EFB}$ is synchronized to the low-to-high transition of CLKB. When $\overline{EFB}$ is low, FIFO1 is empty, and reads are disabled. $\overline{EFB}$ is forced low when FIFO1 is reset and goes high on the second low-to-high transition of CLKB after data is loaded to empty memory. |
| ENA | I | Port A master enable. ENA must be high to enable a low-to-high transition of CLKA to read or write data on port A. |
| ENB | I | Port B master enable. ENB must be high to enable a low-to-high transition of CLKB to read or write data on port B. |
| $\overline{FFA}$ | O | FIFO1 full flag. $\overline{FFA}$ is synchronized to the low-to-high transition of CLKA. When $\overline{FFA}$ is low, FIFO1 is full, and writes to its array are disabled. $\overline{FFA}$ goes low when FIFO1 is reset and goes high on the second low-to-high transition of CLKA after reset. |
| $\overline{FFB}$ | O | FIFO2 full flag. $\overline{FFB}$ is synchronized to the low-to-high transition of CLKB. When $\overline{FFB}$ is low, FIFO2 is full, and writes to its array are disabled. $\overline{FFB}$ goes low when FIFO2 is reset and goes high on the second low-to-high transition of CLKB after reset. |
| FS0, FS1 | I | Flag offset selects. The low-to-high transition of $\overline{RESET}$ latches the value of the FS0 and FS1, which selects one of four preset values for the almost empty and almost full offsets. |
| MBA | I | Port A mailbox select. A high level chooses a mailbox register for a port A read or write operation. When the A0–A35 outputs are active, a high level on MBA selects data from the mail2 register for output, and a low level selects FIFO2 data for output. |
| $\overline{MBF1}$ | O | Mail1 register flag. $\overline{MBF1}$ is set low by the low-to-high transition of CLKA that writes data to the mail1 register. $\overline{MBF1}$ is set back high by a low-to-high transition of CLKB when a port B read is selected and both SIZ1 and SIZ0 are high. $\overline{MBF1}$ is set high when FIFO1 is reset. |
| $\overline{MBF2}$ | O | Mail2 register flag. $\overline{MBF2}$ is set low by the low-to-high transition of CLKB that writes data to the mail2 register. $\overline{MBF2}$ is set back high by a low-to-high transition of CLKA when a port A read is selected and MBA is high. $\overline{MBF2}$ is set high when FIFO2 is reset. |
| ODD/$\overline{EVEN}$ | I | Odd/$\overline{even}$ parity select. Odd parity is checked on each port when ODD/$\overline{EVEN}$ is high, and even parity is checked when ODD/$\overline{EVEN}$ is low. ODD/$\overline{EVEN}$ also selects the type of parity generated for each port if parity generation is enabled for read operations. |

**Terminal Functions (continued)**

| PIN NAME | I/O | DESCRIPTION |
|---|---|---|
| $\overline{PEFA}$ | O | Port A parity error flag. When any byte on A0–A35 fails parity, $\overline{PEFA}$ is forced low. Bytes are organized as A0–A8, A9–A17, A18–A26, and A27–A35, with the most significant bit of each byte serving as the parity bit. The type of parity checked is determined by the level on the ODD/$\overline{EVEN}$ select input. |
| $\overline{PEFB}$ | O | Port B parity error flag. When any valid byte on B0–B35 fails parity, $\overline{PEFB}$ is forced low. Bytes are organized as B0–B8, B9–B17, B18–B26, and B27–B35, with the most significant bit of each byte serving as the parity bit. A byte is valid when it is used in the bus size selection for port B. The type of parity checked is determined by the level on the ODD/$\overline{EVEN}$ select input. |
| PGA | I | Port A parity generation. A high on PGA selects parity to be generated for data read from port A. The level on the ODD/$\overline{EVEN}$ parity select input determines the type of parity generated. |
| PGB | I | Port B parity generation. A high on PGB selects parity to be generated for data read from port B. The level on the ODD/$\overline{EVEN}$ parity select input determines the type of parity generated. |
| $\overline{RESET}$ | I | Reset. To reset the device, four low-to-high transitions of CLKA and four low-to-high transitions of CLKB must occur while $\overline{RESET}$ is low. This sets the $\overline{AFA}$ and $\overline{AFB}$ flags high and the $\overline{EFA}$, $\overline{EFB}$, $\overline{AEA}$, $\overline{AEB}$, $\overline{FFA}$, and $\overline{FFB}$ flags low. The low-to-high transition of $\overline{RESET}$ latches the status of FS1 and FS0 for almost full and almost empty offset selection. |
| SIZ0, SIZ1 | I | Port B bus size selects. A low-to-high transition of CLKB latches the value of SIZ0, SIZ1, and $\overline{BE}$ for a bus size select, and the following low-to-high transition of CLKB implements the latched value as a port B bus size. Port B bus sizes may be selected from long word, word, and byte. A high on both SIZ1 and SIZ0 directs a write or read on port B to a mailbox register. |
| SW0, SW1 | I | Port B byte swap selects. At the beginning of each long word transfer, one of four modes of byte order swapping is selected by SW0 and SW1. The four modes of byte order swapping are no swap, byte swap, word swap, and byte-word swap. Byte order swapping is possible with any bus size selection. |
| W/$\overline{RA}$ | I | Port A write/$\overline{read}$ select. A high selects a write operation and a low selects a read operation on port A for a low-to-high transition of CLKA. The A0–A35 outputs are in the high-impedance state when W/$\overline{RA}$ is high. |
| W/$\overline{RB}$ | I | Port B write/$\overline{read}$ select. A high selects a write operation and a low selects a read operation on port B for a low-to-high transition of CLKB. The B0–B35 outputs are in the high-impedance state when W/$\overline{RB}$ is high. |

## FIFO function

The state of the A0–A35 outputs is controlled by $\overline{CSA}$ and W/$\overline{RA}$. When both $\overline{CSA}$ and W/$\overline{RA}$ are low, the outputs are active. The outputs are in the high-impedance state when either $\overline{CSA}$ or W/$\overline{RA}$ is high. Data is written to FIFO1 from port A on the low-to-high transition of CLKA when $\overline{CSA}$ is low, W/$\overline{RA}$ is high, MBA is low, ENA is high, and the $\overline{FFA}$ flag is high. Data is read from FIFO2 to the A0–A35 outputs on the low-to-high transition of CLKA when $\overline{CSA}$ is low, W/$\overline{RA}$ is low, MBA is low, ENA is high, and the $\overline{EFA}$ flag is high.

The state of the B0–B35 outputs is controlled by $\overline{CSB}$ and W/$\overline{RB}$. When both $\overline{CSB}$ and W/$\overline{RB}$ are low, the outputs are active. The outputs are in the high-impedance state when either $\overline{CSB}$ or W/$\overline{RB}$ is high. Data is written to FIFO2 from port B on the low-to-high transition of CLKB when $\overline{CSB}$ is low, W/$\overline{RB}$ is high, ENB is high, the $\overline{FFB}$ flag is high, and either SIZ0 or SIZ1 is low. Data is read from FIFO1 to the port B outputs on the low-to-high transition of CLKB when $\overline{CSB}$ is low, W/$\overline{RB}$ is low, ENB is high, the $\overline{EFB}$ flag is high, and either SIZ0 or SIZ1 is low.

The setup and hold time constraints to the port clocks for the chip selects ($\overline{CSA}$, $\overline{CSB}$) and write/read selects (W/$\overline{RA}$, W/$\overline{RB}$) are for enabling write and read operations and are not related to high-impedance control of the data outputs. If the master enable signal for a port (ENA or ENB) is set low during a clock cycle, the chip select and write/read select may switch at any time during the cycle to change the state of the data outputs.

Each FIFO flag is two-stage synchronized to a port clock for use as a reliable synchronous control signal. CLKA synchronizes the status of the empty flag ($\overline{EFA}$) and almost empty flag ($\overline{AEA}$) of FIFO2 and the full flag ($\overline{FFA}$) and almost full flag ($\overline{AFA}$) of FIFO1. CLKB synchronizes the status of the empty flag ($\overline{EFB}$) and almost empty flag ($\overline{AEB}$) of FIFO1 and the full flag ($\overline{FFB}$) and almost full flag ($\overline{AFB}$) of FIFO2.

### FIFO function (continued)

When the full flag ($\overline{FFA}$, $\overline{FFB}$) of a port is low, the FIFO receiving input from the port is full, and writes are disabled to its array. When the empty flag ($\overline{EFA}$, $\overline{EFB}$) of a port is low, the FIFO that outputs data to the port is empty, and reads from its memory are disabled.

### mailbox registers

A 36-bit data word may be exchanged between ports and circumvent the normal FIFO path. The mailbox select input (MBA) chooses between a mail register and a FIFO for a port A data transfer operation. Port B accesses a mail register when the bus size select inputs (SIZ0, SIZ1) are both high. A0–A35 data is written to the mail1 register on a low-to-high transition of CLKA when $\overline{CSA}$ is low, W/$\overline{R}$A is high, ENA is high, and MBA is high. B0–B35 data is written to the mail2 register on a low-to-high transition of CLKB when $\overline{CSB}$ is low, W/$\overline{R}$B is high, ENB is high, and both SIZ0 and SIZ1 are high.

When data is written to a mail register, its mailbox flag ($\overline{MBF1}$, $\overline{MBF2}$) is set low. The $\overline{MBF1}$ flag is set high on a low-to-high transition of CLKB when a read is selected for port B and both SIZ0 and SIZ1 are high. The $\overline{MBF2}$ flag is set high on a low-to-high transition of CLKA when a read is selected for port A and the MBA input is high. The data in a mailbox register remains intact after it is read and changes only when new data is written to the register. When the B0–B35 outputs are active, mail1 data is output if both SIZ0 and SIZ1 are high, and FIFO1 data is output if either bus size input is low. The level on MBA selects between FIFO2 and mail2 data for output on A0–A35.

### reset

The SN74ABT7815 is reset by taking the reset input ($\overline{RESET}$) low for at least four CLKA and four CLKB low-to-high transitions. This resets the internal read and write pointers of each FIFO to their initial locations and forces $\overline{AFA}$ and $\overline{AFB}$ flags high and $\overline{EFA}$, $\overline{EFB}$, $\overline{FFA}$, $\overline{FFB}$, $\overline{AEA}$, and $\overline{AEB}$ flags low. The reset input may by asynchronous with respect to either clock. Resetting the device also forces the mailbox flags ($\overline{MBF1}$, $\overline{MBF2}$) high. Data outputs of the FIFO and mailbox register are not reset to any specific logic level. The device must be reset upon power up.

### almost full and almost empty flags

Four preset values are available for the offsets of the almost full and almost empty flags of the SN74ABT7815. The flag select inputs (FS0, FS1) are sampled by the low-to-high transition of the reset input ($\overline{RESET}$), and the offsets for $\overline{AFA}$, $\overline{AEA}$, $\overline{AFB}$, and $\overline{AEB}$ are set according to the flag programming table.

An almost empty flag is low when the number of 36-bit words stored in its FIFO is less than or equal to the flag's offset value. An almost full flag is low when the number of empty locations left in its FIFO is less than or equal to the flag's offset value. Data in the output register of a FIFO has been read from memory, and its previous location is free.

**FLAG PROGRAMMING TABLE**

| FS1 | FS0 | RESET | $\overline{AF}$ AND $\overline{AE}$ OFFSET |
|---|---|---|---|
| H | H | ↑ | 16 |
| H | L | ↑ | 12 |
| L | H | ↑ | 8 |
| L | L | ↑ | 4 |

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### dynamic bus sizing

Port B may be configured in a 36-bit long-word, 18-bit-word, or 9-bit-byte bus size with a choice of big- or little-endian formats to read data from FIFO1 or input data to FIFO2. The bus size can be changed synchronous to CLKB to accommodate peripherals of various bus sizes.

A bus size is selected on the low-to-high transition of CLKB by the levels on the bus size inputs (SIZ0, SIZ1) and the big-endian input ($\overline{BE}$) according to Figure 1. The bus size is implemented on port B by the following low-to-high transition of CLKB. When reading data from FIFO1 and a bus size of word or byte length is implemented for port B, the unused outputs of B0–B35 remain active but static, holding the last data value to decrease power consumption.

The port B almost empty flag ($\overline{AEB}$) and almost full flag ($\overline{AFB}$) always measure the number of 36-bit memory locations in the FIFOs regardless of the bus size. The port B empty flag ($\overline{EFB}$) and full flag ($\overline{FFB}$) are based on the bus size selection.

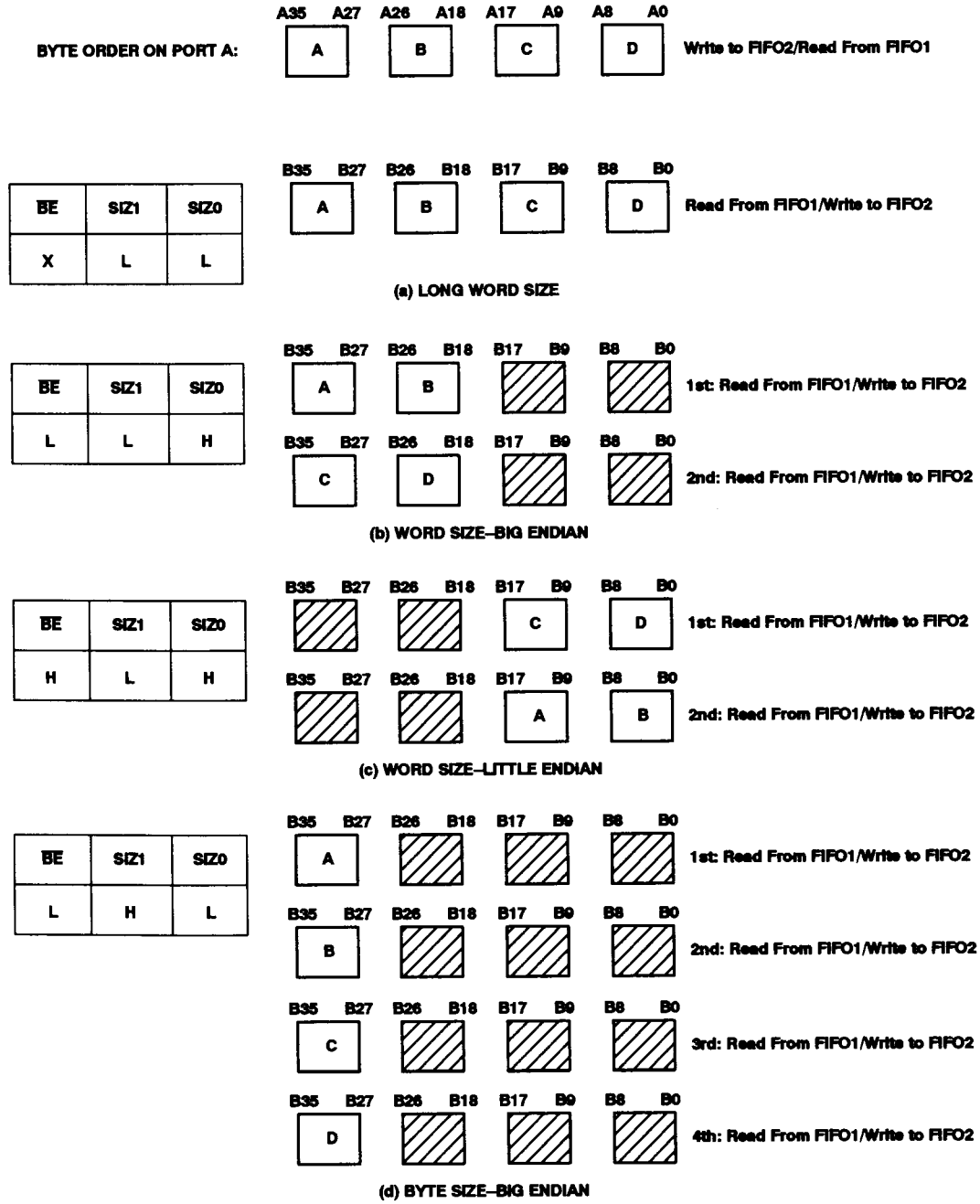


**Figure 1. Dynamic Bus Sizing**

| BE | SIZ1 | SIZ0 |
|---|---|---|
| H | H | L |

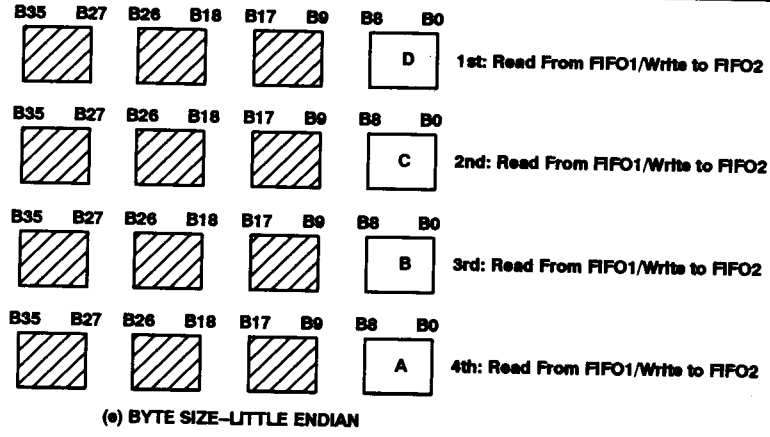


**Figure 1. Dynamic Bus Sizing (continued)**

## byte swapping

The byte order of port B can be changed synchronous to CLKB for FIFO data passing through port B. Four modes of byte order swapping (including no swap) can be done with any data port size selection. The order of the bytes can be rearranged, but the bit order within the bytes remains constant.

When reading data from FIFO1 to port B, the byte arrangement is chosen by the swap inputs (SW0, SW1) on a low-to-high transition of CLKB that reads a new long word from FIFO1. Data is unloaded to the data outputs according to Figure 2.

When writing data from port B to FIFO2, the byte arrangement is chosen by the swap inputs (SW0, SW1) on a low-to-high transition of CLKB that writes a new long word to FIFO2. Data is loaded to memory according to Figure 2. The status of the SW0 and SW1 inputs has no effect when a port B read or write operation accesses a bypass register.

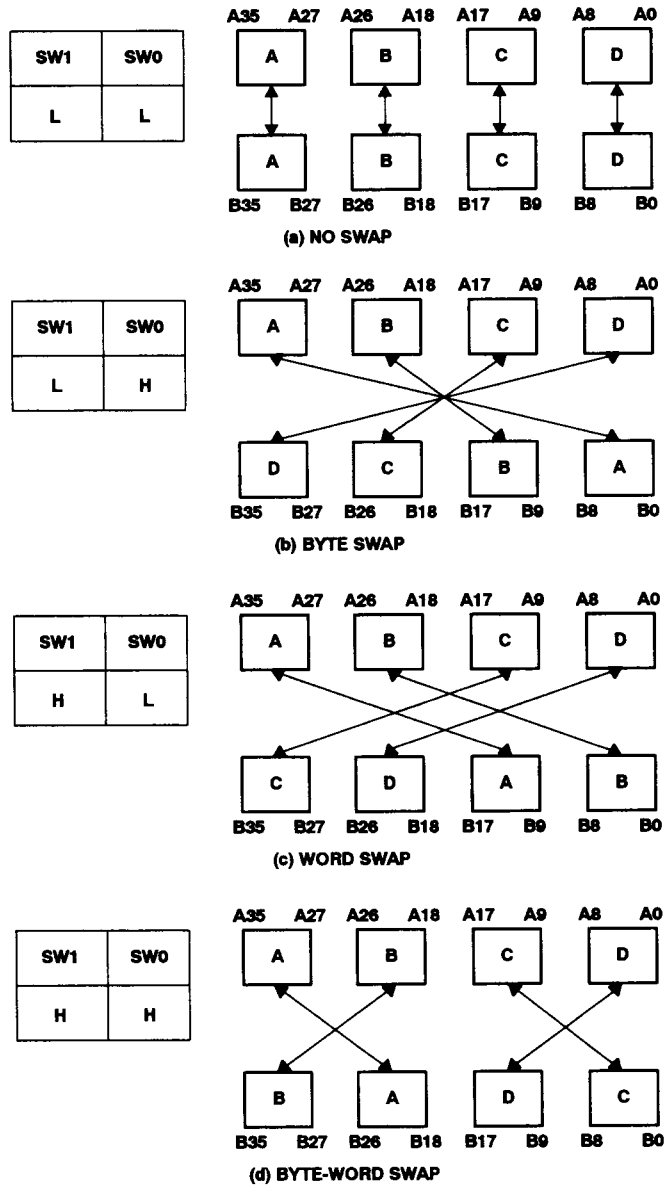


**Figure 2. Byte Swapping (Long Word Size Example)**

### parity checking and parity generation

The parity error flag for port A ($\overline{PEFA}$) is low if any byte on A0–A35 fails a parity check. The bytes are arranged as A0–A8, A9–A17, A18–A26, and A27–A35, with the most significant bit of each byte used as the parity bit. The bytes on port B are also arranged as B0–B8, B9–B17, B18–B26, and B27–B35 with the most signicant bit of each byte used for parity. Only the port B bytes selected by the bus sizing inputs ($\overline{BE}$, SIZ1, SIZ0) are checked for parity, with a parity failure of any of the selected bytes forcing a low on the port B parity error flag ($\overline{PEFB}$). The odd/$\overline{even}$ select input (ODD/$\overline{EVEN}$) chooses the type of parity checked on both port A and port B.

Parity can be generated for data read from a port by asserting the port's parity generation input (PGA, PGB) for the low-to-high transition of the clock that reads the data to the output. When parity generation is selected for a port read, parity is generated for each byte based on the ODD/$\overline{EVEN}$ input selection and stored in the most significant bit of the byte. Parity can be generated for reads from FIFO memory and reads from the mailbox register.

### recommended operating conditions

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | 0.8 | V |
| $I_{OH}$ | High-level output current | | −4 | mA |
| $I_{OL}$ | Low-level output current | | 8 | mA |
| $T_A$ | Operating free-air temperature | 0 | 70 | °C |

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**switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 30 pF (unless otherwise noted)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | 'ACT7815-15 | | 'ACT7815-20 | | 'ACT7815-25 | | 'ACT7815-40 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | CLKA or CLKB | | 67 | | 50 | | 40 | | 25 | | MHz |
| $t_{pd}$ | CLKA↑ | A0–A35 | | 10 | | 12 | | 14 | | 16 | ns |
| | CLKB↑ | B0–B35 | | 10 | | 12 | | 14 | | 16 | |
| | CLKA↑ | $\overline{EFA}$, $\overline{FFA}$, $\overline{AEA}$, $\overline{AFA}$ | | 10 | | 12 | | 14 | | 16 | |
| | CLKB↑ | $\overline{EFB}$, $\overline{FFB}$, $\overline{AEB}$, $\overline{AFB}$ | | 10 | | 12 | | 14 | | 16 | |
| $t_{pd}$ | MBA | A0–A35 | | 11 | | 12 | | 14 | | 16 | |
| | SIZ1, SIZ0† | B0–B35 | | 11 | | 12 | | 14 | | 16 | |
| $t_{pd}$‡ | MBA | A8, A17, A26, A35 | | 14 | | 15 | | 17 | | 19 | ns |
| | SIZ1, SIZ0 | B8, B17, B26, B35 | | 14 | | 15 | | 17 | | 19 | |
| $t_{PHL}$ | CLKA↑ | $\overline{MBF1}$ | | 10 | | 12 | | 14 | | 16 | ns |
| $t_{PLH}$ | CLKB↑ | | | 9 | | 11 | | 13 | | 15 | |
| $t_{PHL}$ | CLKB↑ | $\overline{MBF2}$ | | 10 | | 12 | | 14 | | 16 | ns |
| $t_{PLH}$ | CLKA↑ | | | 9 | | 11 | | 13 | | 15 | |
| $t_{pd}$ | A0–A35 | $\overline{PEFA}$ | | 13 | | 14 | | 16 | | 18 | ns |
| | B0–B35 | $\overline{PEFB}$ | | 13 | | 14 | | 16 | | 18 | |
| $t_{pd}$ | ODD/EVEN | $\overline{PEFA}$ | | 12 | | 13 | | 15 | | 17 | ns |
| | | $\overline{PEFB}$ | | 12 | | 13 | | 15 | | 17 | |
| $t_{PHL}$ | $\overline{RESET}$ | $\overline{AEA}$, $\overline{AEB}$ | | | | | | | | | ns |
| $t_{PLH}$ | $\overline{RESET}$ | $\overline{AFA}$, $\overline{AFB}$ | | | | | | | | | ns |
| | | $\overline{MBF1}$, $\overline{MBF2}$ | | | | | | | | | |
| $t_{en}$ | $\overline{CSA}$, W/$\overline{RA}$ | A0–A35 | | | | | | | | | ns |
| | $\overline{CSB}$, W/$\overline{RB}$ | B0–B35 | | | | | | | | | |
| $t_{dis}$ | $\overline{CSA}$, W/$\overline{RA}$ | A0–A35 | | | | | | | | | ns |
| | $\overline{CSB}$, W/$\overline{RB}$ | B0–B35 | | | | | | | | | |

† Selecting between FIFO1 and mail1 output with SIZ1 and SIZ0
‡ Parity generation is selected when reading a bypass register.

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