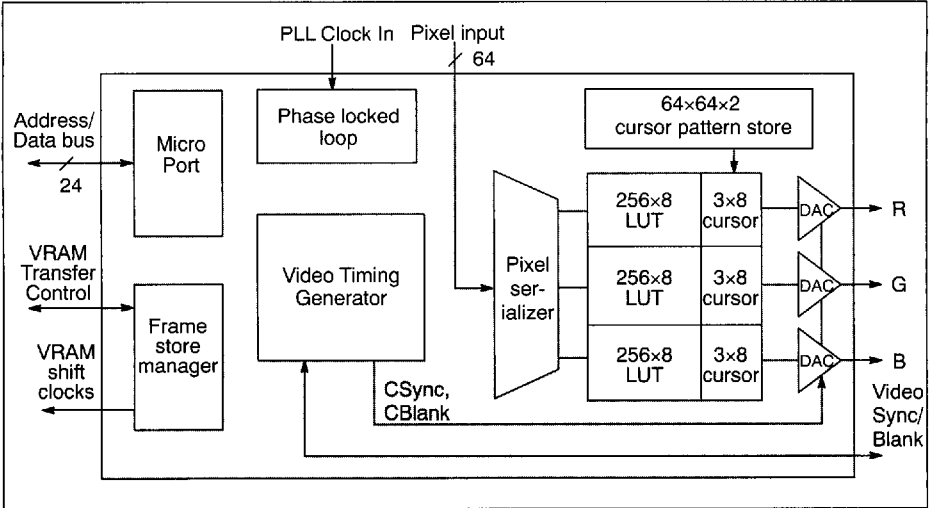# SGS-THOMSON
MICROELECTRONICS

IMS G364

COLOR VIDEO CONTROLLER

PRODUCT OVERVIEW

FEATURES

Video rates up to 110MHz
1, 2, 4 and 8 bit pseudo color pixels
15 or 16 bit true color with gamma correction
24 bit full color with gamma correction
Software configurable video timing generator
Comprehensive video RAM framestore manager
On-chip phase-locked loop pixel clock generator
64×64 pixel ×3 color hardware cursor
Triple 8-bit DACs
Triple 256×8 anti-sparkle lookup RAM

BENEFITS

Reduced component count
Reduced system power consumption
Enhanced system flexibility
Easy upgradeabilty
Broadcast standards compliance
All digital signals below RFI regulated frequency
Software compatible with IMS G332

APPLICATIONS

High resolution graphics and imaging
Broadcast/CC television systems
Multimedia
Graphical user interfaces
X-terminals
Low cost workstations

DESCRIPTION

The IMS G364 is a high performance CMOS device which integrates all the subsystem functions required to control high resolution color graphics displays.

This device has now been superseded by the IMS G365, which offers higher performance and greater ease of design.

The IMS G365 is recommended for all new designs. Full engineering data on the IMS G364 is still available from your local sales office if required.

TABLE OF CONTENTS

14.1   Introduction

The IMS G364 provides all the necessary functions to control real-time operation of a raster scan video display, using dual-ported video RAMs.

The device consists of a 64 bit variable format multiplexed pixel interface, a programmable video timing generator (VTG), a 256 location color lookup table (LUT) with variable addressing modes, triple 8 bit video Digital-to-Analogue Convertors (video DACs), a 64×64×2 bit cursor store and 3 location cursor LUT, a programmable cursor positioning/insertion controller, a video memory control system and phase-locked loop clock generator.

A brief description of each functional block follows, for more detailed information please refer to the relevant section in the full datasheet.
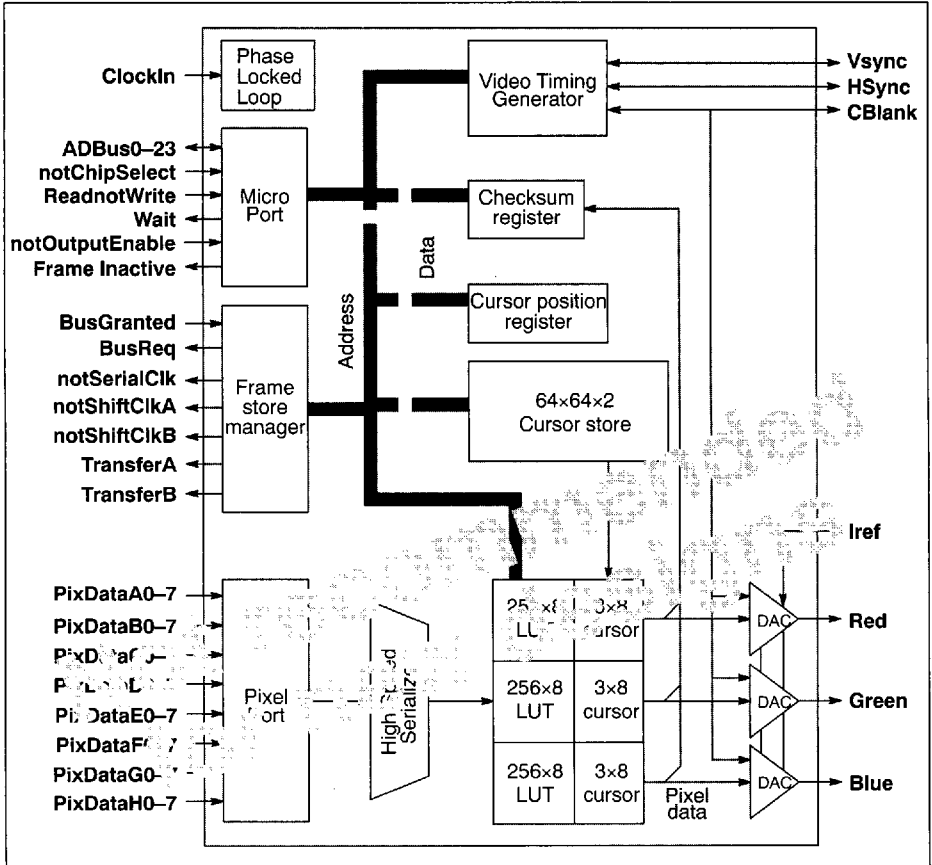

Figure 14.1   IMS G364 Block Diagram

14.1.1 Clocks

An on-chip phase-locked loop clock generator allows the IMS G364 to be driven from a low speed clock in the 5MHz to 10MHz range, which is internally multiplied by a user-specified factor to achieve video data rates. The controller can be clocked by a full rate system clock if desired, although at a reduced frequency compared to that achievable with the PLL.

14.1.2 Micro Port

The entire IMS G364 register space is read/write accessible via the micro port. This is a 24 bit wide synchronous interface, with multiplexed address and data, for single-cycle access to all registers. A wait pin is provided to allow synchronisation between the IMS G364 clock regime and that of the processor or interface bus. This interface is also used to provide the VRAM shift register transfer address.

14.1.3 Video timing generator

The video timing generator is a programmable finite state machine which uses a set of screen description parameters to produce the monitor sync and DAC blanking signals as well as the video RAM shift clock signals. It can be configured to be the system master or, as a slave, to lock onto an external signal which is already synchronous or has been previously genlocked. This may be from another INMOS CVC, giving the potential for multiple, synchronous video systems. The timing generator runs at one quarter of the video dot rate and the screen description parameters therefore have a resolution of four pixel periods.

14.1.4 Framestore manager

All the requirements of supporting a video RAM framestore are met by the IMS G364. The Framestore manager uses two framestore description parameters to maintain a constant supply of pixels to the pixel interface. It supports synchronous reload by supplying the refresh address and the transfer strobes, synchronised to the VRAM SC signals, so that a packed pixel framestore can be implemented regardless of the variations in screen format and framestore architecture. The refresh address generator supports all current VRAM standards together with the NTSC and PAL/SECAM screen formats.

14.1.5 Pixel Port

High pixel rates are achieved by multiplexing the video RAM serial outputs into a 64-bit wide pixel port. The IMS G364 supplies the shift clock signal, automatically adjusting its frequency, along with the multiplex ratio of the port, according to the bits per pixel mode selected. The minimum acceleration ratio is 4:1, achieved in 24 bits per pixel (bpp) mode by the use of an interleaved memory system, for which all the necessary signals are supplied.

14.1.6 Hardware Cursor

The hardware cursor is a complete system. The cursor store and lookup table are memory mapped, its position being modified by a single register access which can occur at any time, becoming valid at the next frame scan. The cursor position is stored in 2's complement relative to the top left pixel on the screen and is independent of monitor specifications.

14.1.7 Anti-sparkle Color Palette

The serialised pixels are used as addresses into a triple 256×8 pipelined RAM. In pseudo color modes one address is applied to all three RAMs giving a maximum of 256 simultaneous colors out of a possible 16·7 million. In true color each RAM is independently addressed for gamma correction of up to 16·7 million simultaneous colors. The palette has an anti-sparkle mechanism which reduces the visible effect of palette updates during display.

14.1.8 Video DACs

The three 8-bit DACs drive RS-170 level signals directly into a 37.5Ω load. They are blanked with programmable setup, internally by the VTG, externally by the **CBlank** pin or by a combination of the two. Composite Sync may be added to all three DACs.

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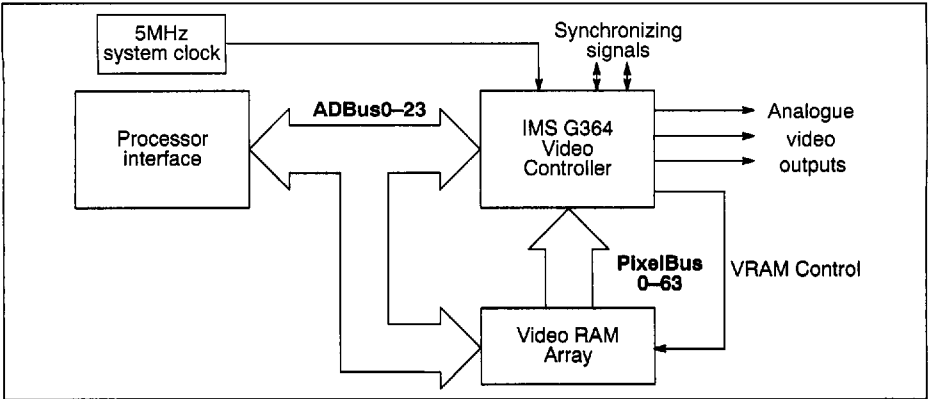
14.1.9 System Operation

Figure 14.2   IMS G364 operating in a simple graphics system

Figure 14.2 shows how the IMS G364 would fit into a typical single-bitmap display system. The clock is typically sourced from a 5MHz crystal, with the video data being streamed to the screen at the full video rate of up to 110MHz. The video RAM array is directly accessed by the processor, with screen management automatically being performed by the IMS G364. All external digital signals and clocks are running at one quarter of the video rate, alleviating problems of high speed system design.

Figure 14.3   IMS G364 operating with an interleaved memory system
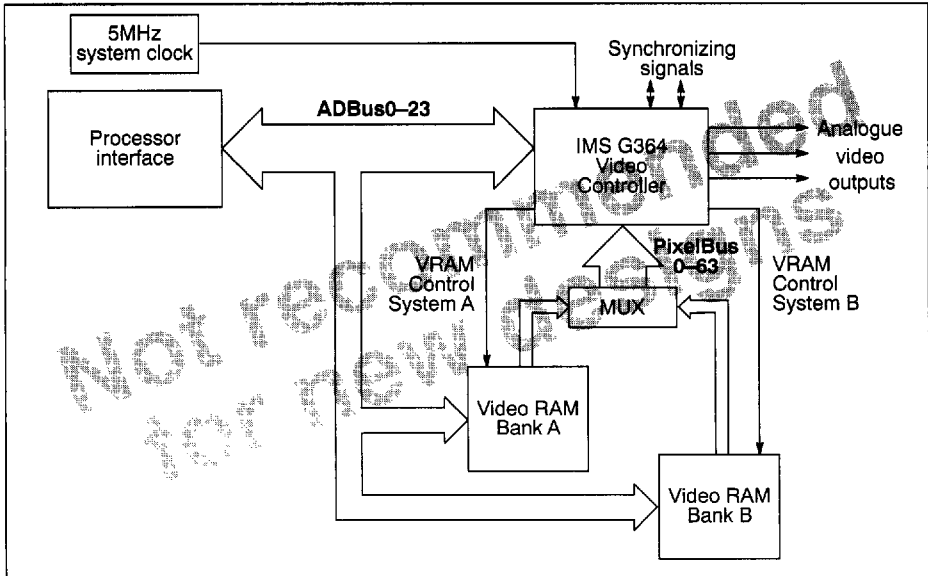
Figure 14.3 shows the organisation of an interleaved framestore. The IMS G364 accepts alternate loads from each bank in turn through an external multiplexor (or if the video rate is low enough - about 85MHz - the VRAM serial output enables can be used instead of external hardware). The IMS G364 supplies all the controls required to implement this architecture.

14.2 Package specifications
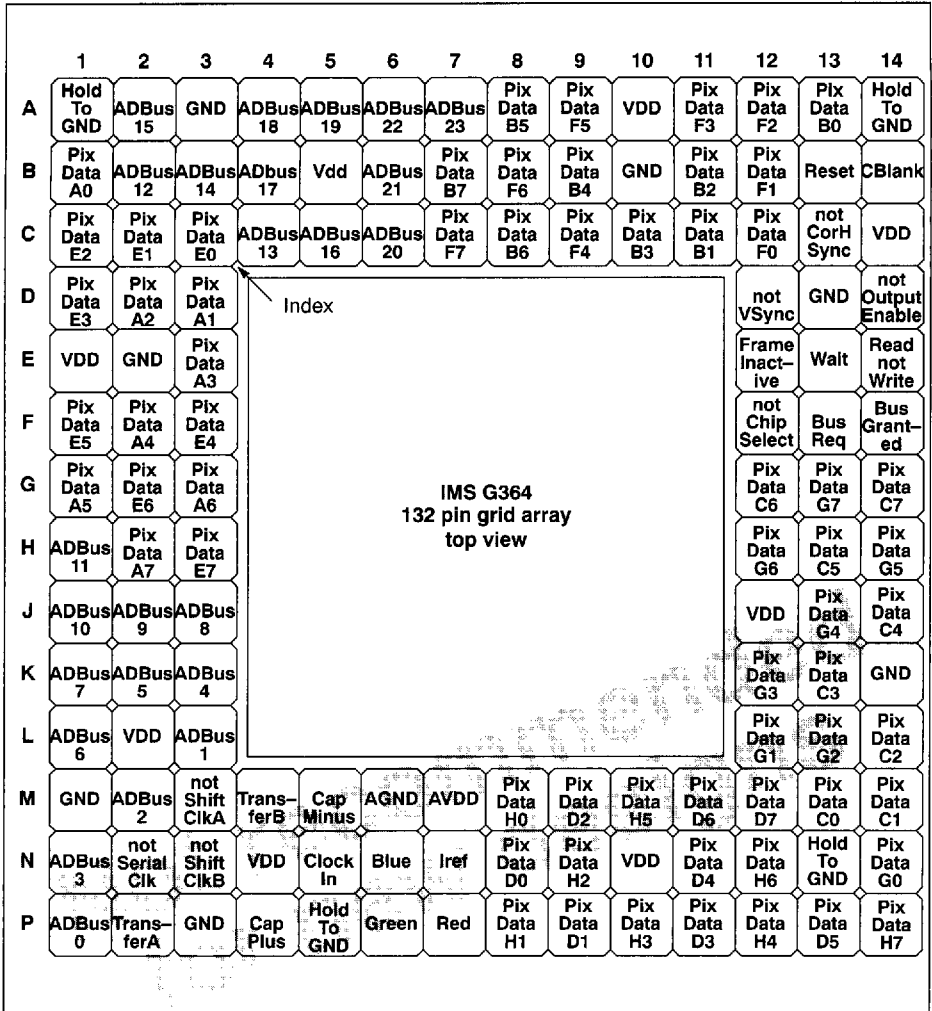
14.2.1 132 pin grid array package

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	Hold To GND	ADBus 15	GND	ADBus 18	ADBus 19	ADBus 22	ADBus 23	Pix Data B5	Pix Data F5	VDD	Pix Data F3	Pix Data F2	Pix Data B0	Hold To GND
B	Pix Data A0	ADBus 12	ADBus 14	ADbus 17	Vdd	ADBus 21	Pix Data B7	Pix Data F6	Pix Data B4	GND	Pix Data B2	Pix Data F1	Reset	CBlank
C	Pix Data E2	Pix Data E1	Pix Data E0	ADBus 13	ADBus 16	ADBus 20	Pix Data F7	Pix Data B6	Pix Data F4	Pix Data B3	Pix Data B1	Pix Data F0	not CorH Sync	VDD
D	Pix Data E3	Pix Data A2	Pix Data A1	Index							not VSync	GND	not Output Enable	
E	VDD	GND	Pix Data A3								Frame Inactive	Wait	Read not Write	
F	Pix Data E5	Pix Data A4	Pix Data E4								not Chip Select	Bus Req	Bus Granted	
G	Pix Data A5	Pix Data E6	Pix Data A6			IMS G364 132 pin grid array top view					Pix Data C6	Pix Data G7	Pix Data C7	
H	ADBus 11	Pix Data A7	Pix Data E7								Pix Data G6	Pix Data C5	Pix Data G5	
J	ADBus 10	ADBus 9	ADBus 8								VDD	Pix Data G4	Pix Data C4	
K	ADBus 7	ADBus 5	ADBus 4								Pix Data G3	Pix Data C3	GND	
L	ADBus 6	VDD	ADBus 1								Pix Data G1	Pix Data G2	Pix Data C2	
M	GND	ADBus 2	not Shift ClkA	Trans-ferB	Cap Minus	AGND	AVDD	Pix Data H0	Pix Data D2	Pix Data H5	Pix Data D6	Pix Data D7	Pix Data C0	Pix Data C1
N	ADBus 3	not Serial Clk	not Shift ClkB	VDD	Clock In	Blue	Iref	Pix Data D0	Pix Data H2	VDD	Pix Data D4	Pix Data H6	Hold To GND	Pix Data G0
P	ADBus 0	Trans-ferA	GND	Cap Plus	Hold To GND	Green	Red	Pix Data H1	Pix Data D1	Pix Data H3	Pix Data D3	Pix Data H4	Pix Data D5	Pix Data H7

Figure 14.4 IMS G364 pin configuration

| DIM	CONTROL DIMENSIONS INCH			ALTERNATIVE DIMENSIONS mm		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.130	0.142	0.155	3.302	3.607	3.937
A1	–	0.050REF	–	–	1.270REF	–
A2	0.080	0.092	0.105	2.032	2.337	2.667
B	0.016	0.018	0.020	0.406	0.457	0.508
B1	–	0.050REF	–	–	1.270REF	–
D	1.385	1.450	1.465	35.179	36.830	37.211
D1	–	1.300REF	–	–	33.020REF	–
e	–	0.100BSC	–	–	2.540BSC	–
E	1.385	1.450	1.465	35.179	36.830	37.211
E1	–	1.300REF	–	–	33.020REF	–
L	0.120	0.130	0.140	3.048	3.302	3.556
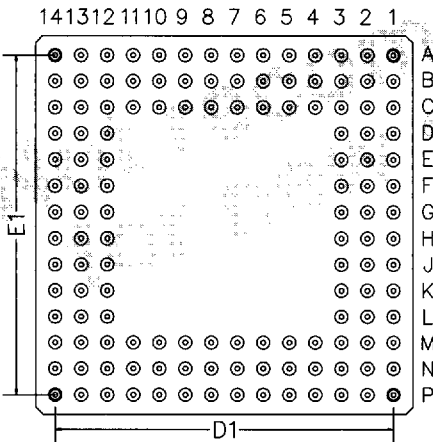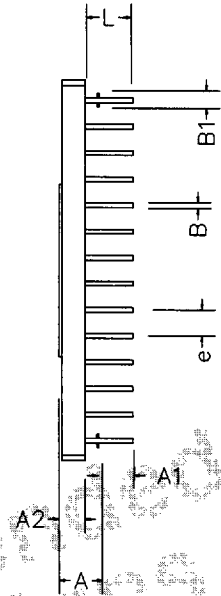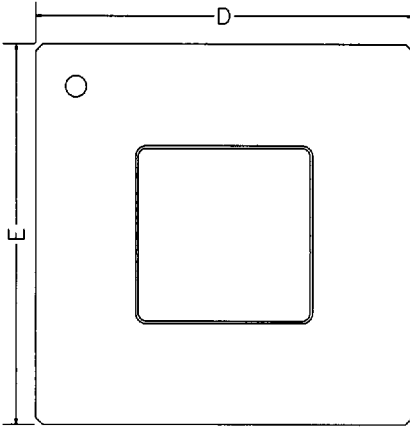
Figure 14.5   132 pin grid array package dimensions

14.3　Ordering information

Device	Clock rate	Package	Part number
IMS G364	85 MHz	132 pin grid array	IMS G364G-85S
IMS G364	100 MHz	132 pin grid array	IMS G364G-10S
IMS G364	110 MHz	132 pin grid array	IMS G364G-11S