

8-DIGIT FLUORESCENT DISPLAY DRIVER FOR MICROCOMPUTOR

DESCRIPTION

The M54844P, a semiconductor integrated circuit fabricated with using IIL technology, is designed for driving an 8-digit, 8-segment fluorescent display.

FEATURES

- Can be used in either an 8-digit or 7-digit plus a decimal point.
- 4-bit data input
- Mode-input controllable display mode
- Internal clock generator
- Wide operating voltage ($V_{CC}=5\sim 12V$)

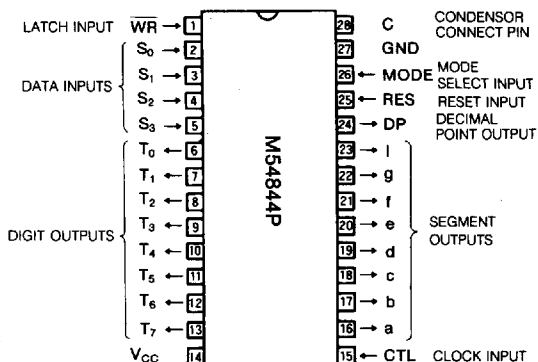
APPLICATION

Micro computer display
 Digital equipment for industrial and consumer use

FUNCTION

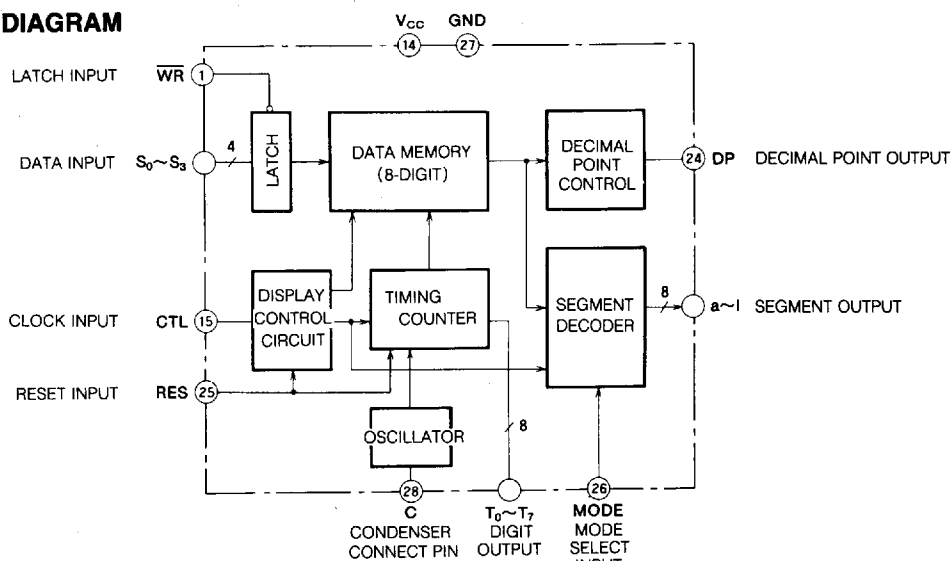
The M54844p, a decoder/driver for fluorescent displays, has a 4-bit $\times$ 8-digit memory. Employing the dynamic lighting method, it can light an 8-segment, 8-digit device. Two indication modes can be selected, by the setting of the MODE input.

PIN CONFIGURATIONS (TOP VIEW)



Outline 28P4

BLOCK DIAGRAM



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DESCRIPTION OF OPERATION

1. Output after reset and during reset.

Outputs during reset (RES=high-state) is shown in the following chart.

Output pin		Output level
Digit output	T_0	H
	$T_1 \sim T_7$	L
Segment output	$a \sim i$	L
	DP	L

After reset, the outputs $T_0 \sim T_7$ are scanned beginning with T_0 . Outputs $S_0 \sim S_1$ and DP remain in low-state until CTL has been input for 8 cycles.

2. Decimal point setting

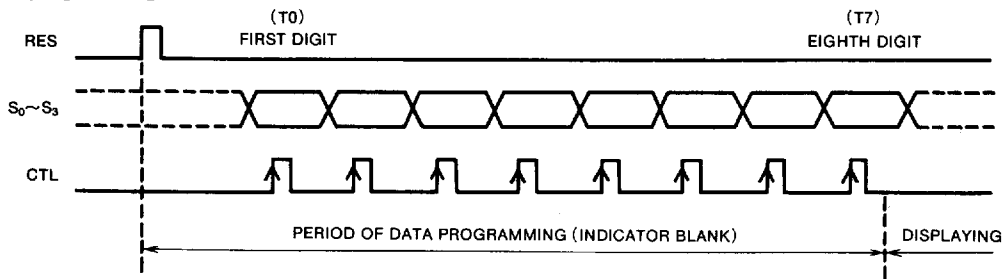
The location of the decimal point depends on the contents of the data memory corresponding to T_0 . When the decimal point is to be displayed, digit T_0 cannot be used.

The display position of the decimal point is as follows.

Content of digit T_0	Display position of decimal point
0 or 8	T_1
1 or 9	T_2
2 or A	T_3
3 or B	T_4
4 or C	T_5
5 or D	T_6
6 or E	T_7
7 or F	T_0

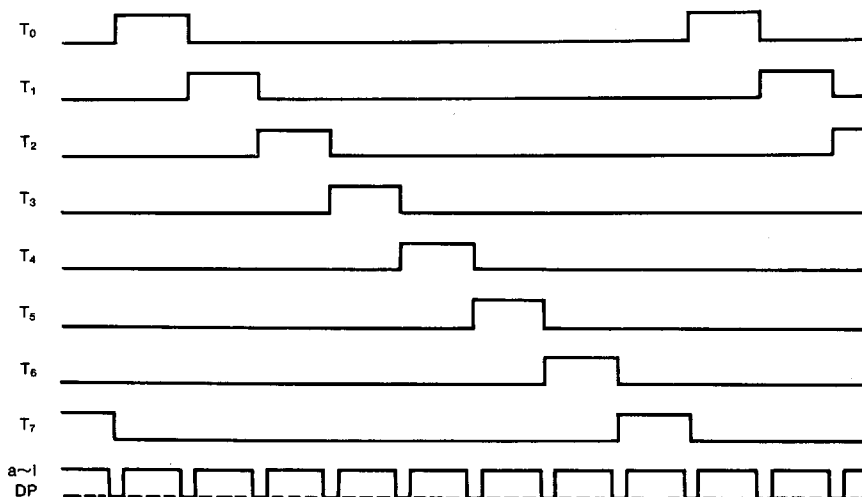
3. Operation timing

(1) Data programming



- Reset input is necessary before data programming input.
- $S_0 \sim S_3$ data is read at the leading edge of the CTL.

(2) Output timing

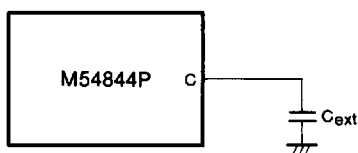
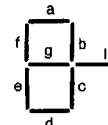


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DISPLAY CHARACTERS

Hexadecimal code Mode	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
I	0	1	2	3	4	5	6	7	8	9	-	E	C	-	0	
II					4						a	b	c	d	e	+

Mode I is displayed when MODE input is low-state.
Mode II is displayed when MODE input is high-state.



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		$-0.3 \sim +15$	V
V_i	Input voltage		$-0.3 \sim V_{CC}$	V
$V_{CC}-V_O$	Voltage between the power supply and output pin	Output off-state	$-0.3 \sim +35$	V
T_{opr}	Operating temperature		$-30 \sim +85$	°C
T_{stg}	Storage temperature		$-55 \sim +125$	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -30 \sim +85^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	10	12	V
$V_{CC}-V_O$	Voltage between the power supply and output pin			33	V

ELECTRICAL CHARACTERISTICS ($T_a = -30 \sim +85^\circ\text{C}$, $V_{CC} = 10\text{V}$, unless otherwise noted)

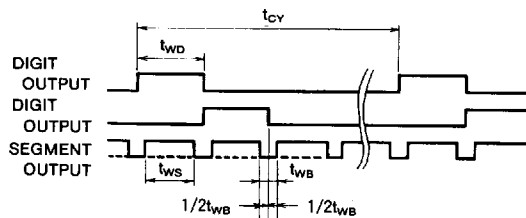
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2		V_{CC}	V
V_{IL}	Low-level input voltage		0		0.7	V
I_{IH}	High-level input current	$V_{IH} = 10\text{V}$			20	μA
I_{IL}	Low-level input current	$V_{IL} = 0.5\text{V}$			-200	μA
V_{OH}	High-level output voltage	$I_{OH} = -10\text{mA}$	8			V
I_{OLK}	Output leak current	$V_O = -20\text{V}$			-30	μA
I_{CC}	Supply current	Display off-state		12	18	mA
t_{ws}	Segment output width	$C_{ext} = 1000\text{pF}$	130	260	520	μs
t_{wb}	Segment blank width	$C_{ext} = 1000\text{pF}$	20	40	80	μs
t_{wD}	Digit output width	$C_{ext} = 1000\text{pF}$	150	300	600	μs
t_{CY}	Digit period	$C_{ext} = 1000\text{pF}$	1.2	2.4	4.8	ms

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TIMING REQUIREMENTS ($T_a = -30 \sim +85^\circ\text{C}$, $V_{cc} = 4.5 \sim 12\text{V}$, unless otherwise noted)

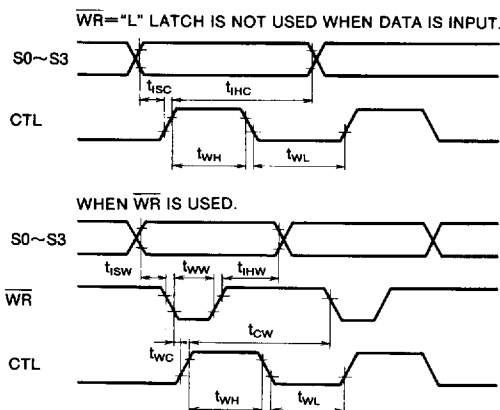
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{ISC}	Input setup time in relation to CLK		5			μs
t_{IHC}	Input hold time in relation to CLK		10			μs
t_{WH}	High-level CTL width		5			μs
t_{WL}	Low-level CTL width		10			μs
t_{ISW}	Input setup time in relation to WR		0			μs
t_{IHW}	Input hold time in relation to WR		5			μs
t_{WW}	WR width		5			μs
t_{WC}	WR $\rightarrow$ CTL		5			μs
t_{CW}	CTL $\rightarrow$ WR		15			μs

OUTPUT TIMING DIAGRAM



DIGIT OUTPUT WIDTH $t_{wd} = 15t_{osc}$
 SEGMENT OUTPUT WIDTH $t_{ws} = 13t_{osc}$
 SEGMENT BLANK WIDTH $t_{wb} = 2t_{osc}$
 (t_{osc} is oscillation period of the oscillator circuit.)

INPUT TIMING DIAGRAM



WR="L" LATCH IS NOT USED WHEN DATA IS INPUT.

WHEN WR IS USED.