

OBJECTIVE SPECIFICATIONS

Features

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 $I_{OL} = 8 \text{ mA @ } V_{OL} = 0.5V$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

74HCTLS: $-40^{\circ}C$ to $+85^{\circ}C$
54HCTLS: $-55^{\circ}C$ to $+125^{\circ}C$

Quad 2-Input NOR Gates

Description

These devices contain four independent 2-input NOR gates that perform the Boolean functions $Y = A + \bar{B}$ or $Y = \bar{A} + B$.

Fabrication using ISI proprietary ICE-MOS process, these devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

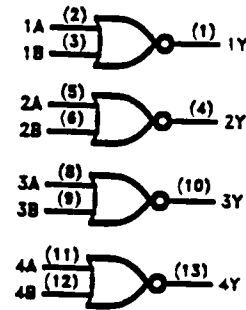
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Function Table

(Each Gate)

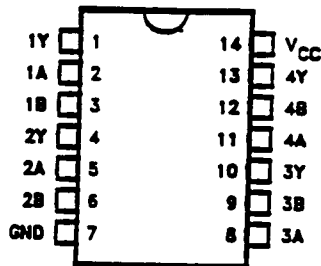
Inputs		Output
A	B	Y
H	H	L
L	X	H
X	L	H

Logic Diagram



0083-2

Pin Configuration



0083-1

Absolute Maximum Ratings*

Supply Voltage Range, V_{CC} -0.5V to 7V
 DC Input Diode Current, I_{IK}
 ($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$)..... ± 20 mA
 DC Output Diode Current, I_{OK}
 ($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$)..... ± 20 mA
 Continuous Output Current Per Pin, I_O
 ($-0.5V < V_O < V_{CC} + 0.5V$)..... ± 35 mA
 Continuous Current Through
 V_{CC} or GND pins..... ± 125 mA
 Storage Temperature Range, T_{STG} -65°C to +150°C
 Power Dissipation Per Package, P_D 500 mW

*Power Dissipation temperature derating:
 Plastic Package (N): -12mW/°C from 65°C to 85°C
 Ceramic Package (J): -12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} 4.5V to 5.5V
 DC Input & Output Voltages*, V_{IN} , V_{OUT} 0V to V_{CC}

Operating Temperature

Range 74HCTLS: -40°C to +85°C
 54HCTLS: -55°C to +125°C

Input Rise & Fall Times, t_r , t_f Max 500 ns

*Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC Electrical Characteristics ($V_{CC} = 5V \pm 10\%$ Unless Otherwise Specified)

Sym	Parameter	Test Conditions	$T_A = 25^\circ C$			74HCTLS	54HCTLS	Unit
			Typ	Guaranteed Limits		$T_A = -40^\circ C$ to $+85^\circ C$	$T_A = -55^\circ C$ to $+125^\circ C$	
V_{IH}	Minimum High-Level Input Voltage			2.0	2.0	2.0	V	
V_{IL}	Maximum Low-Level Input Voltage			0.8	0.8	0.8	V	
V_{OH}	Minimum High-Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $I_O = -20 \mu A$ $I_O = -4 mA$	V_{CC} 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V	
V_{OL}	Maximum Low-Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $I_O = 20 \mu A$ $I_O = 4 mA$ $I_O = 8 mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V	
I_{IN}	Maximum Input Current	$V_{IN} = V_{CC}$ or GND		± 0.1	± 1.0	± 1.0	μA	
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu A$		2.0	20.0	40.0	μA	

AC Electrical Characteristics (Input $t_r, t_f \leq 6$ ns), HCTLS02

Sym	Parameter	Conditions •	$T_A = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		74HCTLS $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V } \pm 10\%$	54HCTLS $T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V } \pm 10\%$	Unit
			Typ	Guaranteed Limits			
t_{PLH}	Maximum Propagation Delay	$C_L = 50$ pF	9	15	18	22	ns
t_{PHL}			10	15	18	22	
C_{IN}	Maximum Input Capacitance		5				pF
C_{PD}	Power Dissipation Capacitance*	(per gate)	15				pF

* C_{PD} determines the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

• For AC switching test circuits and timing waveforms see section 2.