MH88205
HYBRID DTMF RECEIVER SYSTEM

53 ORIG

002984

FEB. 79

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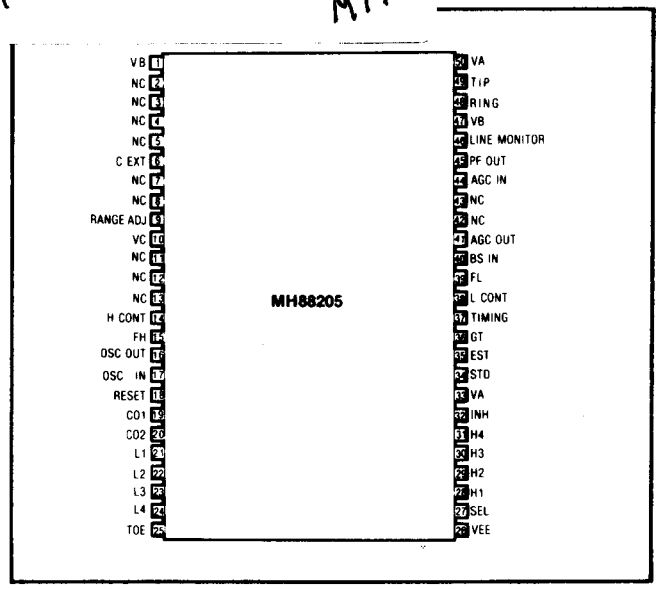
FEATURES:

- UP TO 55dB DYNAMIC RANGE
- AGC FOR PRECISE TWIST DETECTION
- NO EXTERNAL COMPONENTS NEEDED
- DIRECT CONNECTION TO TELEPHONE LINE
- EXCEPTIONAL TALK OFF
- 14dB SIGNAL TO NOISE RATIO
- ACQUISITION TIME ADJUSTABLE DOWN TO 10 ms
- MAJOR PARAMETERS EXTERNALLY ADJUSTABLE



APPLICATIONS:

- END TO END SIGNALING
- CONTROL SYSTEMS
- MOBILE RADIO
- CENTRAL OFFICE
- PABX
- KEY SYSTEMS

DESCRIPTION:

The MITEL MH88205 Hybrid TOUCH-TONE® Receiver is a high performance, high quality unit packaged in a dual in line hybrid measuring only 2.5" x 1.5" x 0.25" and requires no external components for normal operation. The unit features exceptional dynamic range and precise twist performance both adjustable to meet the exacting demands of end to end signaling applications as well as providing a unit of excellent central office quality.

The MH88205 utilizes a digital detection algorithm incorporated in the MITEL CMOS/LSI MT8820 Digital Tone Decoder, which provides the unit with excellent talk-off immunity and signal to noise performance.

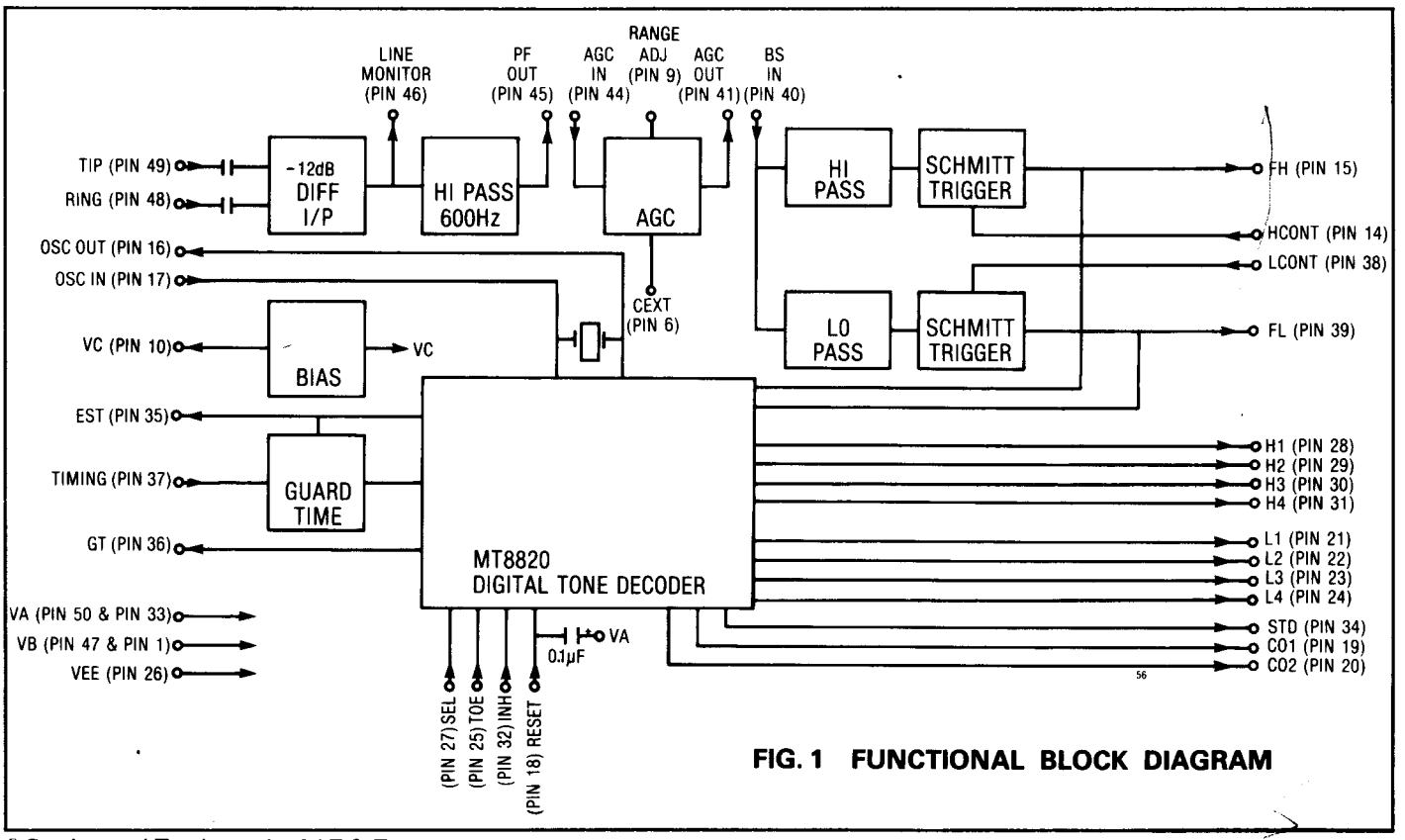


FIG. 1 FUNCTIONAL BLOCK DIAGRAM

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2805m

ABSOLUTE MAXIMUM RATINGS

RATING	SYMBOL	VALUE		UNIT
		MIN	MAX	
Analog Supply Voltage	$V_A - V_B$		22	V
Digital Supply Voltage	$V_A - V_{EE}$	−0.5	16	V
Digital Input Voltage	V_{IN}	V_{EE} − 0.3	V_A+0.3	V
Operating Temperature Range	T_A	−40	+85	°C
Storage Temperature Range	T_{STRG}	−55	+125	°C

DC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS T_A=25°C V_A=12v, V_B=V_{EE}=0V UNLESS OTHERWISE SPECIFIED	
1 Analog Operating Voltage (V_A-V_B)		8		18	V		
2 Digital Operating Supply Voltage (V_A-V_{EE})		4.75		16	V		
3 Operating Supply Current	I_A		15	25	mA		
4 Operating Supply Current	I_{EE}		−0.6	−1	mA		
5 Input Low Level Voltage	V_{IL}			2	V	SEL, TOE, INH, RESET	
6 Input High Level Voltage	V_{IH}	10			V	SEL, TOE, INH, RESET	
7 Input Pull Down Current	I_{IH}	0.1		0.4	mA	SEL,INH	V_{IN}=12V
8 Input Pull Down Current	I_{IH}	0.02		0.1	mA	RESET	V_{IN}=12V
9 Input Pull Up Current	I_{IL}	−0.015		−0.1	mA	TOE	V_{IN}=0V
10 Output Low Level Current	I_{OL}	1			mA	V_O=0.5V	L1-L4,H1-H4
11 Output High Level Current	I_{OH}	−1			mA	V_O=11.5V	CO1, CO2
12 Output Low Level Voltage	V_{OL}			0.4	V	I_{OL}=0.4mA	V_A=+5V V_{EE}=0v
13 Output High Level Voltage	V_{OH}	4.6			V	I_{OH}=−0.4mA	L1-L4, H1-H4 CO1, CO2
14 Output Low Level Voltage	V_{OL}			0.5	V	I_{OL}=20μA	STD NOTE 1 V_A=+5V
15 Output High Level Voltage	V_{OH}	4.5			V	I_{OH}=−10μA	V_B=−5V V_{EE}=0V

Note 1: STD Logic Low Level is internally referenced at (VA-VEE-0.7V) if (VA-VEE) ≤6V; (VA−6V) if (VA-VEE) ≥ 6V.

AC ELECTRICAL AND TIMING CHARACTERISTICS

CHARACTERISTIC	SYMBOL	LIMITS			UNITS	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED. TA=25°C, V_A=12v, V_B=V_{EE}=0V
		MIN	TYP	MAX		
1 Valid Signal Level		−20		+10	dBm600Ω	Dual tone, Range Adj. Open
2 Valid Signal Level (Extended)		−45		+10	dBm600Ω	Dual tone. Max. sensitivity
3 Signal to Noise Ratio		14			dB	Note 1
4 Max Twist Acceptance (Standard)		8	10		(V_L/V_H)dB	Note 2
5 Min Twist Rejection (Standard)			10	14	(V_L/V_H)dB	Note 2
6 Max Twist Acceptance (Reverse)		6	8		(V_H/V_L)dB	Note 2
7 Min Twist Rejection (Reverse)			8	12	(V_H/V_L)dB	Note 2
8 Recognition Bandwidth		±2.0		±2.8	%	
9 Differential Input Impedance		180	200		kΩ	f = lkHz.
10 Common Mode DC				200	V	
11 Common Mode AC				50	V_{PP}	
12 Dial Tone Rejection		−30			dB	f = 500Hz.
13 Tone Recognition Time	t_{REC}	24	28	32	ms	Note 2
14 Inter Digit Pause	t_{IDP}	18			ms	Note 2
15 Intra Digit Drop-out	t_{DO}			14	ms	Note 2
16 Digital Detection Time	t_{DD}	8	12	16	ms	
17 Data Valid to STD Delay	t_{DSTD}	6		10	μs	
18 Guard Time	t_{GT}		15		ms	Note 2

NOTES: 1. Band limited white noise (300Hz–3400Hz).
Tone burst 50ms on – 50ms off.
Error rate 1 in 10,000.
2. Normal mode. No external adjustment.
3. After tone recognition.

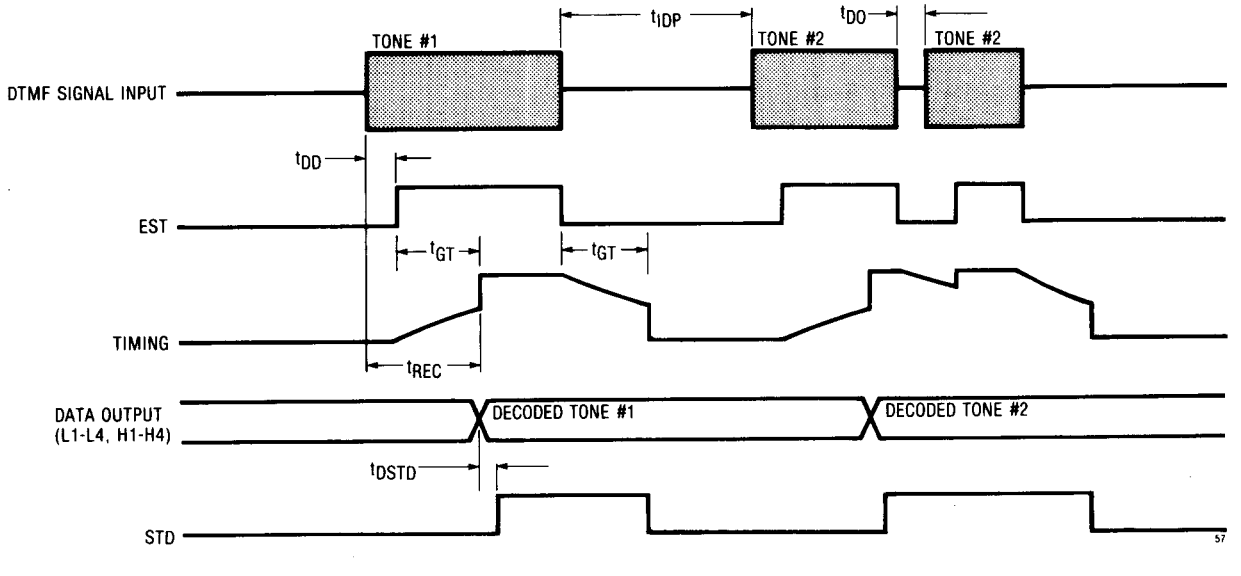


FIG. 2 TIMING WAVEFORM DIAGRAM

PIN DESCRIPTION

PIN	NAME	DESCRIPTION
1	V_B	Negative Analog Power Supply (also Pin 47).
6	CEXT	Monitors AGC relaxation time constant capacitor.
9	RANGE ADJ	Resistor connected between Pin 9 and Vc (Pin 10) increases input sensitivity.
10	V_C	Internally derived analog common rail {5/9(VA-VB)}. Power supply output.
14	HCONT	Resistor connected between Pin 14 and FH (Pin 15) decreases (V_H/V_L) twist ACCEPT/REJECT window.
15	FH	Output of High Group Schmitt trigger.
16	OSC OUT	Output of internal oscillator amplifier. 3.58 MHz.
17	OSC IN	Input of internal oscillator amplifier.
18	RESET	Active HIGH logic input. Resets MT8820 digital tone decoder.
19 20	CO1 CO2	18.2KHz digital clock output. $\phi 1$. Active low, non overlapping 18.2KHz digital clock output. $\phi 2$. Active low, non overlapping
21 22 23 24	L1 L2 L3 L4	Low tone group decoded digital outputs. Active HIGH If SEL (Pin 27) = HIGH, these outputs indicate valid tone, low group component. If SEL=LOW, L1-L4 provide a hexadecimal format.
25	TOE	3 State Output Enable logic input. Active HIGH enables L1-L4, H1-H4 data output. TOE=LOW; L1-L4, H1-H4 are high impedance.
26	V_{EE}	Negative Logic Input/Output Common
27	SEL	Output Code Select logic input. HIGH on this input selects 2 of 8 code on L1-L4, H1-H4. LOW selects L1-L4 hexadecimal code and H1-H4 an alternative 4 BIT code.
28 29 30 31	H1 H2 H3 H4	High tone decoded digital outputs. Active HIGH If SEL (Pin 27) = HIGH, these outputs indicate valid tone, high group component. If SEL=LOW, H1-H4 provide an alternative 4BIT code.
32	INH	Full Decode Inhibit logic input. Active HIGH disables detection of A,B,C,D,*,#.
33	V_A	Positive Analog/Logic Power Supply (also Pin 50)
34	STD	Valid Tone Detect indication, logic output. Active HIGH.
35	EST	Early Steering Digital Output. Active HIGH indicates digital detection of valid tone pair before guard time.
36	GT	Guard Time. Normally connected to Pin 37, TIMING
37	TIMING	Guard Time Adjust. A capacitor connected between Pin 37 and V_A increases guard time. A resistor connected between Pin 37 and EST decreases guard time.
38	LCONT	Resistor connected between Pin 38 and FL (Pin 39) decreases (V_L/V_H) twist ACCEPT/REJECT window.
39	FL	Output of Low Group Schmitt trigger.
40	BS IN	Analog input to the bandsplitting filters. Normally connected to AGC OUT (Pin 41).
41	AGC OUT	Analog output of the AGC circuit. Normally connected to BS IN (Pin 40).
44	AGC IN	Analog input to the AGC circuit. Normally connected to PF OUT (pin 45).
45	PF OUT	Analog output from Dial Tone Reject 600Hz. high pass filter. Normally connected to AGC IN (Pin 44).
46	LINE MONITOR	Single ended monitor of differential line input. Attenuated 12dB referred to line input signal.
47	V_B	Negative Analog Power Supply. (also Pin 1)
48 49	RING TIP	Differential line inputs ac coupled. Direct connection to telephone line.
50	V_A	Positive Analog Power Supply. (also Pin 33)

697 Hz.	770 Hz.	852 Hz.	941 Hz.
1209 Hz.	1336 Hz.	1477 Hz.	1633 Hz.

FUNCTIONAL DESCRIPTION

The MITEL hybrid DTMF tone receiver offers small size (2.5" x 1.5"), exceptional signal detection performance, and high quality through the use of state of the art thick film and CMOS/LSI technology. No external components are needed and the unit can be directly connected to telephone lines. Digital outputs are CMOS and low power SCHOTTKY TTL compatible (2 loads). The unit is particularly suited to applications where high sensitivity, high twist and detection in the presence of noise is required such as end to end signaling and mobile radio. Additionally, it provides a high performance cost effective solution in Central Office, PABX and other applications. For maximum flexibility all major functional blocks of the receiver are externally accessible, and the use of an external resistor provides adjustment of input sensitivity, twist accept/reject limits and guard time decrement while the use of an external capacitor allows an increase of guard time.

The MH88205 is designed to accept the standard TOUCH-TONE frequencies as recommended by CCITT normally generated from a push button TOUCH-TONE telephone set. See Fig. 4.

The input signal is received on the TIP and RING which provide an ac coupled balanced differential input impedance of approximately 200KΩ. The signal is fed into a high pass filter providing at least 30dB dial tone rejection. The use of an AGC circuit provides the unit with up to 55dB dynamic range, while the combination of AGC and Schmitt triggers following the band splitting filters provide precise twist control and adjustment.

The high and low frequency signals are separated by band splitting 5th order elliptic filters, the outputs of which are fed into a Schmitt trigger circuit per tone group. This produces a square wave the frequency of the incoming high and low tones on FH and FL respectively.

The MITEL MT8820 Digital Tone Decoder chip accepts FH and FL and performs a complex proprietary averaging algorithm empirically developed in a practical telecommunications environment. On valid detection of both the high and low tone the early steering output, EST, goes HIGH. (Refer to Fig. 2) This activates a simple analog guard time circuit which operates on tone acquisition and release, preventing multiple digit recognition in the presence of impulse noise, or, tone interruption less than the allowable tone drop-out time t_{DO}. In the event of a tone drop-out or frequency error prior to elapse of the guard time, t_{GT}, EST goes low resetting the analog timer and the digital detection algorithm is repeated.

At the positive transition of TIMING after t_{GT} has elapsed, the output latches (L1-L4, H1-H4) of the MT8820 are updated. Three output formats are selectable via SEL, Pin 27. These formats are 2 of 8 active high, hexadecimal and an alternate 4 BIT code. The truth table is listed in Table I. The data in the output latches will remain stable until the valid recognition of the subsequent tone pair. The end of a tone is not recognized until t_{GT} has timed out on the trailing edge of the detected tone pair. A delayed strobe signal, STD, is available on Pin 34. This signal remains HIGH for the duration of the detected tone pair and goes low after the release guard time has elapsed. Additionally, a 3-state output enable, TOE, Pin 25, is provided to enable bussing of the data outputs . Two non-overlapping, active low clocks are provided on CO1 and CO2 for optional use with digital logic that may be used to process the decoded digital outputs.

The INH pin taken HIGH, allows the user to inhibit the decode of tone pairs corresponding to the keypad designations A,B,C,D,*,#, further reducing susceptibility to "talk-off".

OUTPUT TRUTH TABLE — TABLE I

	SEL=H (2-of-8 Code)								SEL=L L1-L4 Hexadecimal Code. H1-H4 format compatible with GI AY-5-9100 Unit.							
	L1	L2	L3	L4	H1	H2	H3	H4	L1	L2	L3	L4	H1	H2	H3	H4
1	H	L	L	L	H	L	L	L	H	L	L	L	L	L	L	L
2	H	L	L	L	L	H	L	L	L	H	L	L	L	H	L	L
3	H	L	L	L	L	L	H	L	H	H	L	L	L	L	H	L
4	L	H	L	L	H	L	L	L	L	L	H	L	L	L	L	H
5	L	H	L	L	L	H	L	L	H	L	H	L	L	H	L	H
6	L	H	L	L	L	L	H	L	L	H	H	L	L	L	H	H
7	L	L	H	L	H	L	L	L	H	H	H	L	H	L	L	L
8	L	L	H	L	L	H	L	L	L	L	L	H	H	H	L	L
9	L	L	H	L	L	L	H	L	H	L	L	H	H	L	H	L
0	L	L	L	H	L	H	L	L	L	H	L	H	L	H	H	L
*	L	L	L	H	H	L	L	L	H	H	L	H	H	L	H	H
#	L	L	L	H	L	L	H	L	L	L	H	H	H	L	L	H
A	H	L	L	L	L	L	L	H	H	L	H	H	H	H	H	L
B	L	H	L	L	L	L	L	H	L	H	H	H	H	H	L	H
C	L	L	H	L	L	L	L	H	H	H	H	H	L	H	H	H
D	L	L	L	H	L	L	L	H	L	L	L	L	H	H	H	H

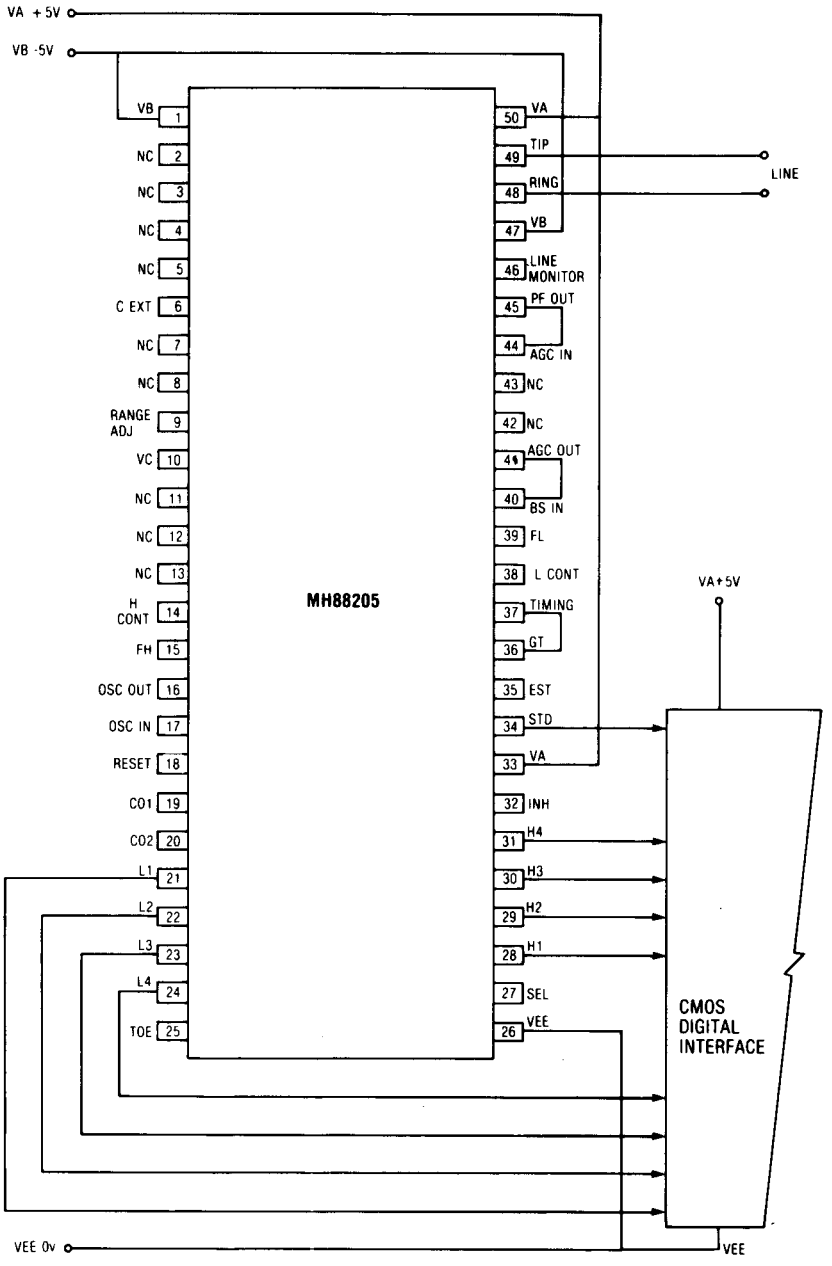


FIG. 3 TYPICAL CONNECTION DIAGRAM

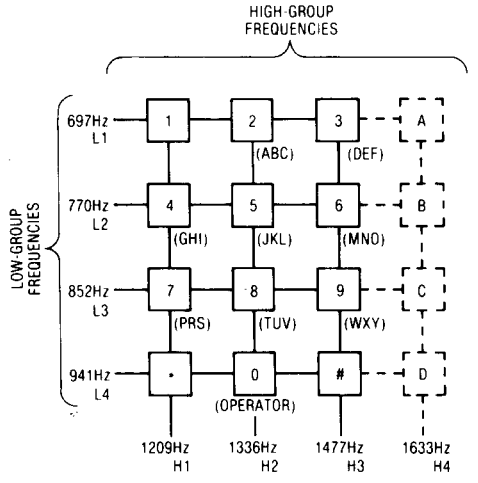
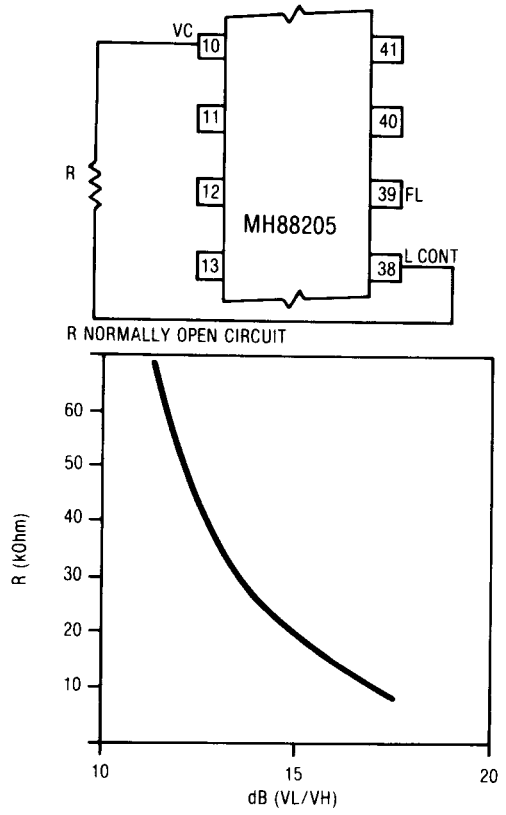


FIG. 4 DTMF KEYPAD

VL/VH TWIST INCREMENT



VL/VH TWIST DECREMENT

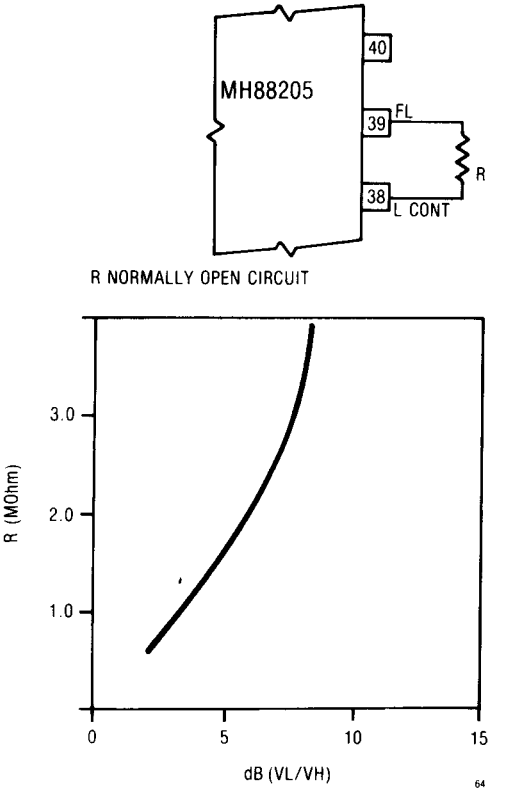
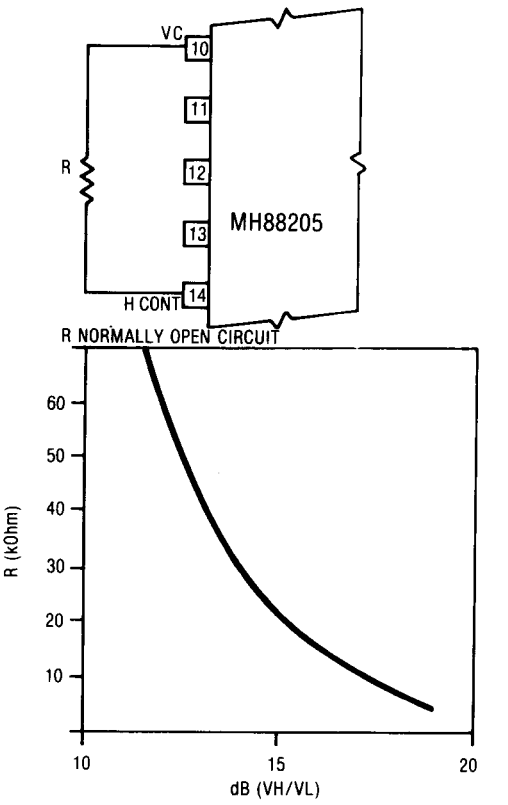


FIG. 9 $V_L > V_H$ TWIST ADJUSTMENT

VH/VL TWIST INCREMENT



VH/VL TWIST DECREMENT

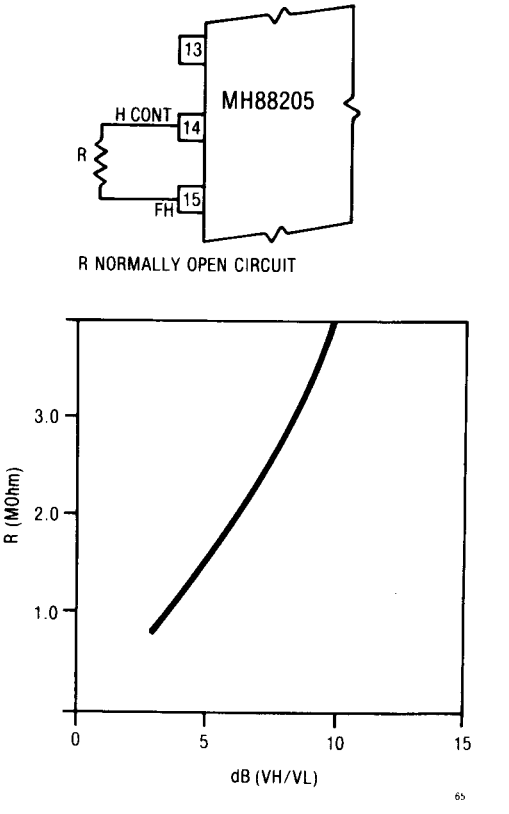
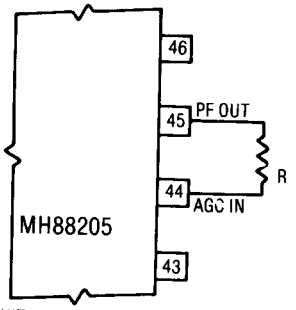
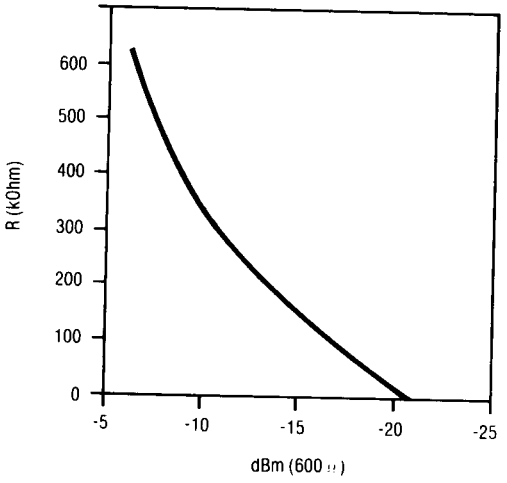


FIG. 10 $V_H > V_L$ TWIST ADJUSTMENT

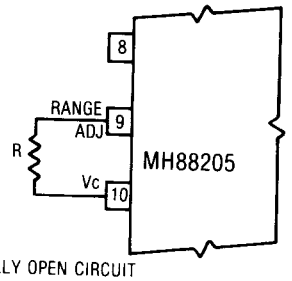
MINIMUM VALID SIGNAL LEVEL INCREMENT



R NORMALLY SHORT CIRCUIT



MINIMUM VALID SIGNAL LEVEL DECREMENT



R NORMALLY OPEN CIRCUIT

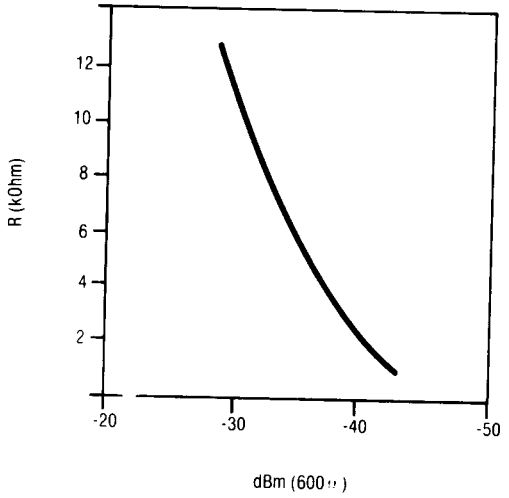


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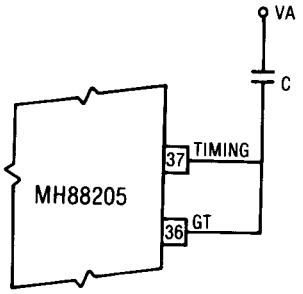
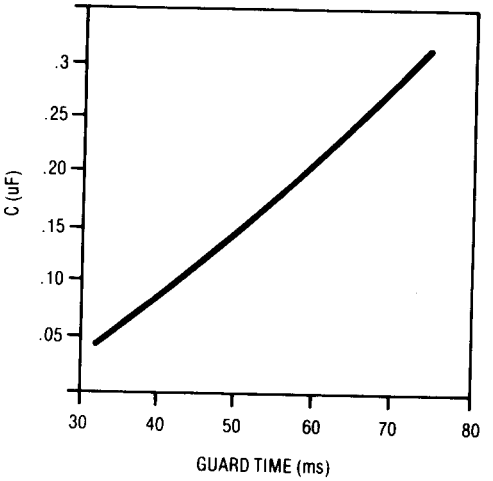
FIG. 7 INPUT SENSITIVITY ADJUSTMENT

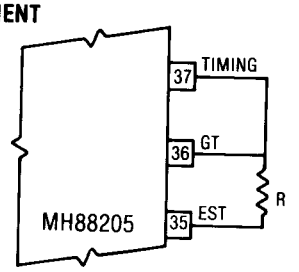
GUARD TIME INCREMENT



C NORMALLY NOT CONNECTED



GUARD TIME DECREMENT



R NORMALLY OPEN CIRCUIT

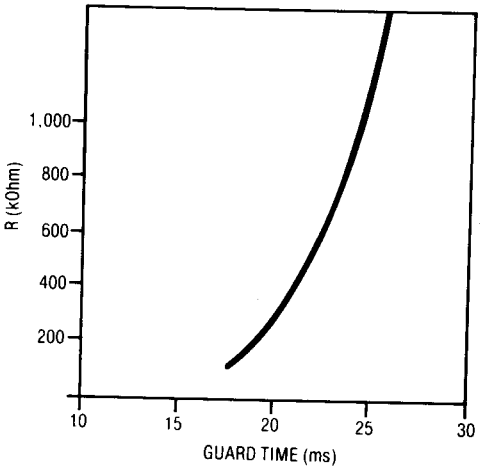


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FIG. 8 GUARD TIME ADJUSTMENT

APPLICATIONS:

The typical connection diagram, Fig. 3, illustrates the ease with which the MH88205 may be applied in a system, requiring no extra external components to perform the tone receiving and decoding function, and providing direct connection to 5V CMOS logic.

The outputs L1-L4, H1-H4, CO1 and CO2 are directly interfaceable to low Power TTL if V_A and V_{EE} are connected to the TTL positive and common rails respectively. However, it is necessary to buffer STD as shown in Fig. 6. Fig. 5 shows how to interface the MH88205 to high voltage CMOS.

A feature of the MH88205 is the flexibility to adjust tone recognition parameters by the use of one external resistor. The following parameters are adjustable:

* input sensitivity
* guard time
* VL>VH standard twist accept/reject limit.
* VH>VL reverse twist accept/reject limit.

The methods of increasing or decreasing each one of these parameters are shown in Figures 7, 8, 9, and 10, respectively.

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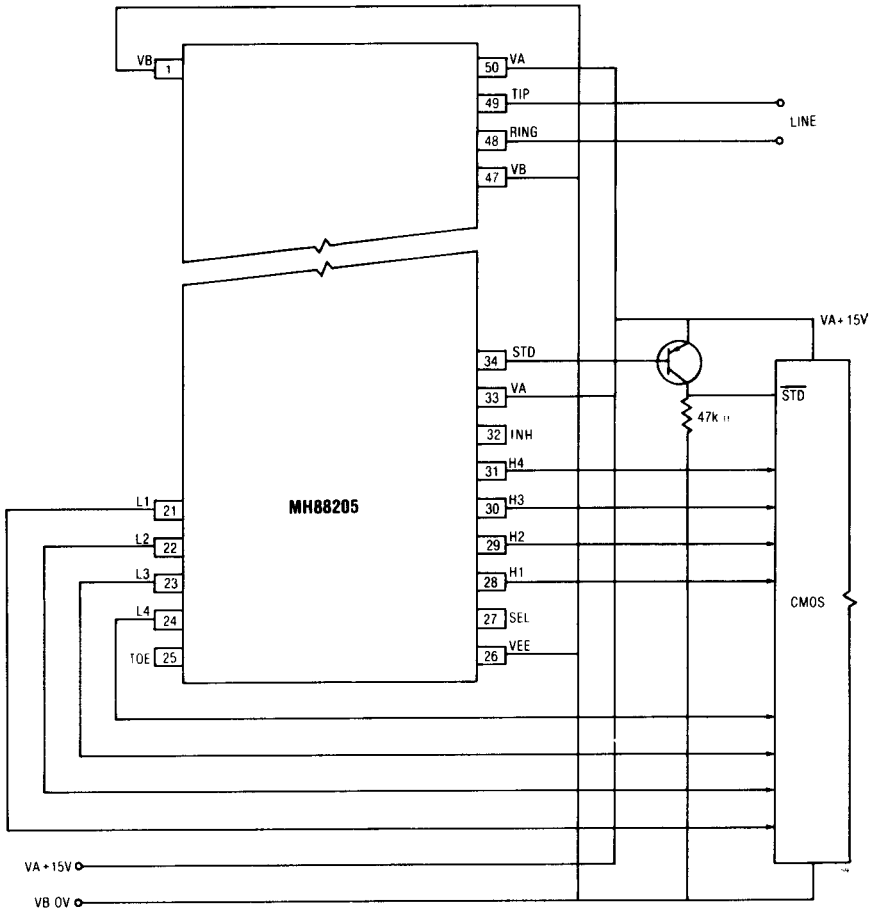

FIG. 5 INTERFACING TO HIGH VOLTAGE CMOS

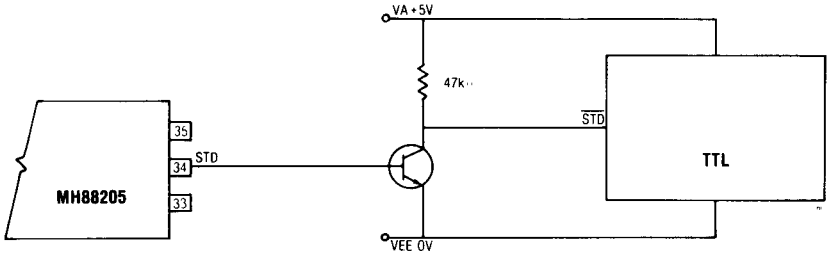

FIG. 6 INTERFACING STD TO TTL.

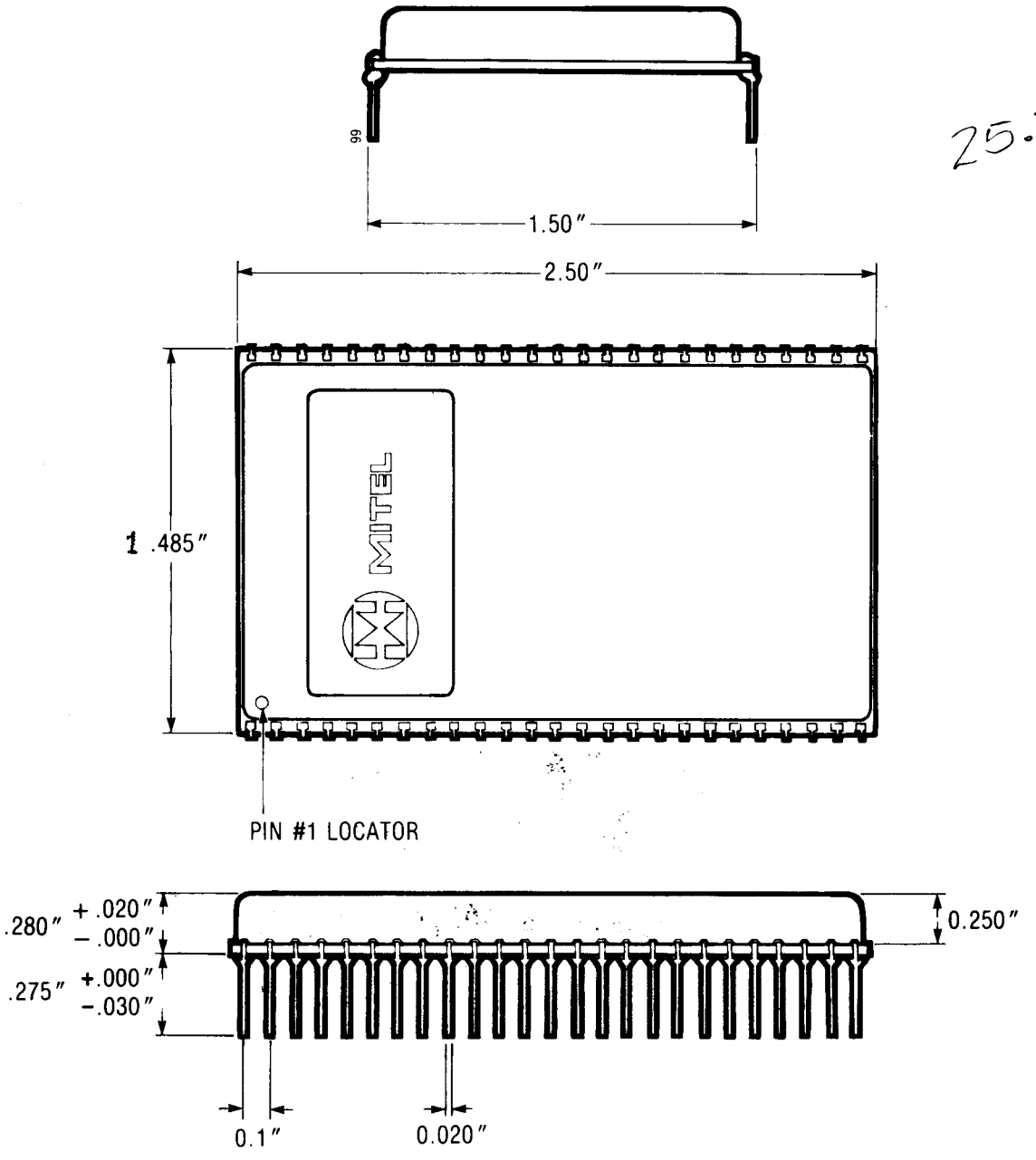

FIG. 11 MECHANICAL DATA

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