
FDDI 1300 nm Transceiver

Technical Data

New **HFBR-5101
HFBR-5102**

Features

- Full Compliance with FDDI PMD Standard
- Multisourced Package Style with:
 - 2 X 11 Pins
 - User Installable Key
- Available with Either Metal or Plastic Media Interface Connector/Receptacle
- Suitable for Use in Equipment Regulated for:
 - VCCI Class 2, CISPR 22B, CENELEC 55022B and FCC Class B
 - Immunity to EM/RFI
 - Immunity to ESD
- Wavesolder and Aqueous Wash Compatible
- Single +5 V Power Supply
- Shifted ECL Logic Interface Directly Compatible with FDDI PHY Circuits
- Compatible with TAXIchip™ * Encode/Decode Circuits

*TAXIchip™ is a trademark of Advanced Micro Devices, Inc.

Applications

- FDDI Single or Dual Attachment Stations
- Local ATM Interfaces at 125 MBd, 140 MBd, 155 MBd
- Fiber Channel Interfaces at 133 MBd
- Proprietary Interfaces

Description

The FDDI transceiver described in this data sheet is a member of a growing family of 1300 nm technology fiber optic products available from Hewlett-Packard. FDDI is an acronym for the Fiber Distributed Data Interface local area network standard. This FDDI transceiver product supplies the performance necessary for the system designer who seeks to develop equipment with fully compliant FDDI interfaces per the FDDI Physical Layer Medium Dependent (PMD) standard. This standard has been approved as an International Standard, ISO/IEC 9314-3, and an American National Standard, ANSI X3.166-1990. The performance of this Hewlett-Packard transceiver is guaranteed over the operating



temperature and power supply voltage ranges found in most commercial equipment. Sufficient margin exists over the FDDI PMD requirements to allow for substantial equipment mission-life and configuration flexibility.

Hewlett-Packard is a vertically integrated supplier. The 1300 nm LED and PIN devices along with the three custom bipolar integrated circuits (ICs) used in these products have been developed and manufactured by Hewlett-Packard. The transceiver assembly and testing is performed in facilities wholly-owned and operated by Hewlett-Packard.

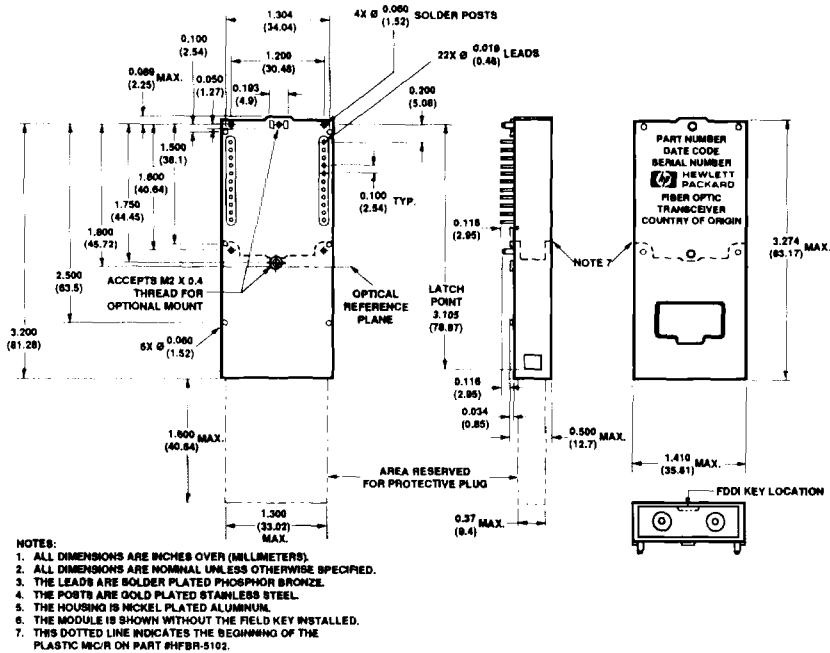


Figure 1. Outline Drawing. HFBR-5101 – Metal MIC/R, HFBR-5102 – Plastic MIC/R

Transmitter Section

The transmitter section of the FDDI transceiver uses a 1300 nm InGaAsP LED and a single custom silicon bipolar LED driver integrated circuit. The LED has an integral etched lens that provides efficient coupling to multimode fibers when combined with the Hewlett-Packard custom optical subassembly. The driver circuit provides temperature compensation for a predictable output optical power over the recommended operating temperature range. It also maintains a steady power supply current due to internal loads which conduct the LED drive current when logic "0"s are being transmitted to minimize creation of high frequency noise on power supply lines. The data input to

the transmitter section is differential, 100K ECL compatible, referenced (shifted) to operate from a +5 volt supply.

Receiver Section

The receiver section of the FDDI transceiver uses a 1300 nm InGaAs PIN photodiode and two custom silicon bipolar integrated circuits. The PIN is a planar top-illuminated device which provides ease of assembly into the Hewlett-Packard custom optical subassembly. The preamplifier IC is mounted in the optical subassembly with the PIN detector to maximize the receiver sensitivity. This sensitivity is guaranteed over a wide time-window in the data output eye-pattern. The second IC, a quantizer, provides the final pulse shaping for the logic

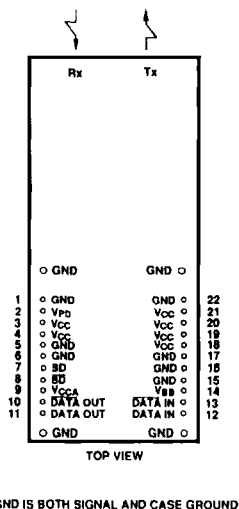


Figure 2. Pin Assignments.

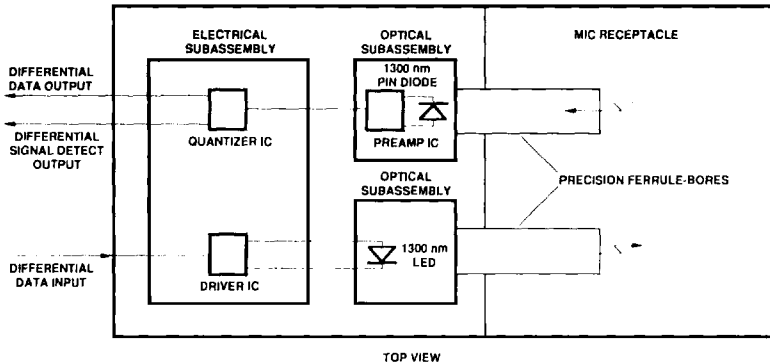


Figure 3. Block Diagram.

output and the Signal Detect function. Both the Data and Signal Detect logic outputs are differential, 100K ECL compatible, referenced (shifted) to a +5 volt power supply.

A strong attribute of the receiver section of this transceiver is the ability to provide excellent sensitivity over a wide output data eye-opening. A wide window time-width (eye-opening) that results in only a small sensitivity change from the center symbol time-position relaxes strict timing requirements on the FDDI PHY clock recovery circuitry. The receiver sensitivity is guaranteed over a wide 4.6 ns window time-width under minimum input jitter conditions. This wide window time-width ensures that under maximum FDDI PMD worst case Active Input Interface peak-to-peak jitter conditions of DCD (1.0 ns), DDJ (1.2 ns), and RJ (0.76 ns), the receiver will maintain a minimum 2.13 ns window time-width for a clock recovery circuit per the example in the FDDI PMD Annex E. Receiver tests using a wider window time-width opening along with corresponding smaller input jitter conditions

are equivalent to testing with the larger worst case FDDI PMD input jitter conditions, and the minimum window time-width of 2.13 ns. Please read Note 17 for a detailed explanation.

When only small sensitivity changes occur over a wide window time-width, the clock recovery circuit can exhibit larger static alignment error (a time offset from true center symbol position) plus more data dependent and random clock jitter and still maintain the FDDI PMD error rate requirements. Figure 9 illustrates the typical tradeoff of available window time-width versus sensitivity penalty. Designers can tradeoff for less clock recovery performance with little loss of sensitivity in this Hewlett-Packard receiver.

Package

The overall package concept for the Hewlett-Packard FDDI transceiver consists of three basic elements; the optical subassemblies, the electrical subassembly, and the housing with integral FDDI Media Interface Connector Receptacle

(MIC/R). The objective of the design is to provide consistent optoelectronic performance in commercial equipment environments over extended equipment mission- lifetimes. The two versions provide design flexibility for different chassis grounding schemes. Two versions of the transceiver are available:

- The HFBR-5102 is constructed with a non-conductive plastic MIC/R mated to an aluminum case for the electrical subassembly. See Figure 1 for the outline drawing. This part is intended for use in equipment designs where separation is desired between the system signal ground and the chassis ground. The plastic MIC/R provides this ground isolation. The low emissions signature of the HFBR-5102 makes it compatible with VCCI Class 2, CISPR 22B, CENELEC 55022B and FCC Class B EMI Regulations.
- The HFBR-5101 is an all aluminum package part including the MIC/R. See Figure 1 for the outline drawing. The HFBR-5101 has

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a low electromagnetic emissions signature but can be used in conjunction with conductive gasketing to the equipment chassis to form an EMI shield. This shield can prevent emissions generated inside the equipment from leaking outside.

The package is mechanically attached to the designer's circuit board by wave-soldered posts that eliminate the need for secondary operations which screw or rivet the device to the board. Two holes are provided in the bottom of the package for those circuit board applications where additional, or alternate, mechanical attachment is desired.

The optical subassemblies contain the 1300 nm LED (transmitter section) and the 1300 nm PIN with preamplifier IC (receiver section). Both transmitter and receiver optical subassemblies are hermetically sealed. These optical subassemblies are actively aligned to optical elements in the ferrule-bores. This active alignment provides optimal optical coupling for both the transmitter and receiver functions.

The electrical subassembly contains the driver and quantizer integrated circuits along with various surface-mounted passive components. This electrical subassembly provides optimum electrical performance with good noise immunity.

The housing for the electrical subassembly is aluminum with nickel plating. Aluminum is used for its excellent thermal conductivity which maintains the junction temperatures of the active semiconductors at low levels for high reliability and long mission-life. The optical subassemblies with their precision connector ferrule-bores are attached to the electrical subassembly and aligned to the MIC/R. Electrical and optical subassembly signal grounds are connected to the aluminum housing for maximum shielding.

The optical ports in the MIC/R are covered with an easily removable, high temperature, protective plug to prevent contamination during wave solder assembly of circuit boards and for shipment to end-user sites.

This package is compatible with normal wave solder and aqueous wash assembly procedures used in the industry today.

The transceiver is delivered in a specially designed shipping container to protect the part from mechanical or ESD damage during shipment or storage.

Product Reliability Data

Various environmental and life tests are performed on these products on an ongoing basis. Contact your local Hewlett-Packard sales representative to obtain copies of the latest test summaries as they become available.

Ordering Information

The Hewlett-Packard FDDI Transceivers are available packaged with key inserts per Table 1. The all metal HFBR-5101 directly replaces the HFBR-5125 transceiver per Table 1, and the HFBR-5102 is identical to the HFBR-5101 except for the plastic MIC/R.

Table 1. Ordering Information

	Transceiver Metal MIC/R	Transceiver Plastic MIC/R
Transceiver with a set of 4 key inserts (A, B, M and S)	HFBR-5101 Option ALL (Replaces HFBR-5125 Option ALL)	HFBR-5102 Option ALL
Transceiver with no key inserts included	HFBR-5101 Option 0FN	HFBR-5102 Option 0FN
Transceiver with A key installed	HFBR-5101 Option 0FA	HFBR-5102 Option 0FA
Transceiver with B key installed	HFBR-5101 Option 0FB	HFBR-5102 Option 0FB
Transceiver with M key installed	HFBR-5101 Option 0FM	HFBR-5102 Option 0FM
Transceiver with S key installed	HFBR-5101 Option 0FS	HFBR-5102 Option 0FS
Bag of 50 bags of 4 key inserts (A, B, M, and S)	HFBR-ABMS	
Bag of 100 A key inserts	HFBR-000A	
Bag of 100 B key inserts	HFBR-000B	
Bag of 100 M key inserts	HFBR-000M	
Bag of 100 S key inserts	HFBR-000S	

Figure 4 shows the key inserts which are black plastic parts with an identifying key letter code molded into the top surface of each key.

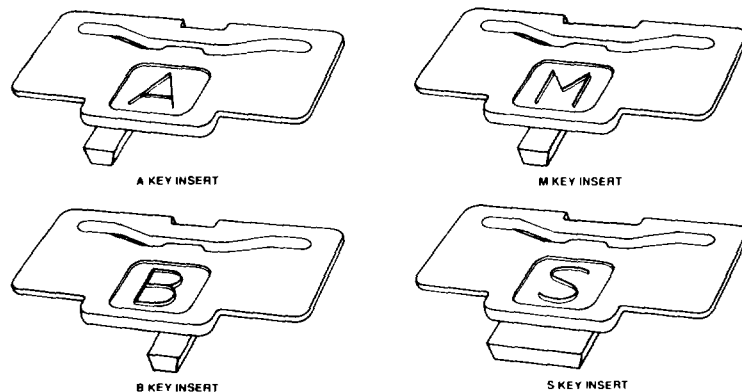


Figure 4. Key Inserts.

- NOTES
1. ALL KEY INSERTS MATE WITH KEYHOLE IN TOP OF TRANSCEIVER SHOWN IN FIGURE 1.
 2. ALL KEY INSERTS ARE BLACK PLASTIC.

FDDI Transceiver

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Storage Temperature	T_S	-40		100	°C	
Operating Temperature-Ambient	T_A	-10		80	°C	Note 1
Lead Soldering Temperature	T_{SOLD}			270	°C	
Lead Soldering Time	t_{SOLD}			4	sec.	
Supply Voltage	V_{CC}	-0.5		7.0	V	Note 2
Data Input Voltage	V_I	-0.5		V_{CC}	V	
Differential Input Voltage	V_D			1.4	V	Note 3
Output Current	I_O			50	mA	Note 4

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by electrostatic discharge (ESD).

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Operating Temperature-Ambient	T_A	0		70	°C	Note 1
Supply Voltage	V_{CC}	4.75		5.25	V	Note 2
Supply Voltage – ECL Driver	V_{CCA}	4.75		5.25	V	Note 2
Supply Voltage – PIN	V_{PD}	4.75		5.25	V	Note 2
Data Input Voltage – Low	$V_{IL} - V_{CC}$	-1.810		-1.475	V	
Data Input Voltage – High	$V_{IH} - V_{CC}$	-1.165		-0.880	V	
Data and Signal Detect Output Load	R_L		50		Ω	Note 5
Signaling Rate	f_s	10		125	MBd	Note 6 Figures 5, 6

Transmitter Section

Transmitter Electrical Characteristics

($T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 4.75\text{ V}$ to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Supply Current	I_{CC}		170	240	mA	Note 7
Power Dissipation	P_{DISS}		0.85	1.2	W	Note 7
Threshold Voltage	$V_{BB} - V_{CC}$	-1.420		-1.240	V	Note 8
Data Input Current – Low	I_{IL}	-350			μA	
Data Input Current – High	I_{IH}			350	μA	

Transmitter Optical Characteristics

($T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 4.75\text{ V}$ to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Output Optical Power 62.5/125 μm , NA = 0.275 Fiber	P_O	-18.5	-16.2	-14	dBm avg	Note 9
Output Optical Power Temperature Coefficient	$\frac{\Delta P_O}{\Delta T}$		-0.015	-0.02	dB/ $^\circ\text{C}$	
Optical Extinction Ratio			0.01 -40	1.0 -20	% dB	Note 10
Center Wavelength	λ_C	1270	1320	1380	nm	Note 11 Figure 7
Spectral Width – FWHM	$\Delta\lambda$		140	170	nm	Note 12 Figure 7
Optical Rise Time	t_r	0.6	1.3	3.0	ns	Note 13 Figures 7, 8
Optical Fall Time	t_f	0.6	2.0	3.0	ns	Note 13 Figures 7, 8
Duty Cycle Distortion Contributed by the Transmitter	DCD		0.13	0.4	ns pk-to-pk	Note 14
Data Dependent Jitter Contributed by the Transmitter	DDJ		0.20	0.6	ns pk-to-pk	Note 15
Random Jitter Contributed by the Transmitter	RJ		0.01	0.69	ns pk-to-pk	Note 16



Receiver Section

Receiver Optical Characteristics

($T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 4.75\text{ V}$ to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Input Optical Power Minimum at Window Edge	$P_{IN\ Min} (W)$		-35.4	-33	dBm avg	Note 17 Figure 9
Input Optical Power Minimum at Center	$P_{IN\ Min} (C)$		-37	-34.5	dBm avg	Note 18 Figure 9
Input Optical Power Maximum	$P_{IN\ Max}$	-14	-12.9		dBm avg	Note 32
Operating Wavelength	λ	1270		1380	nm	
Signal Detect Asserted	P_A	$P_D + 1.5\text{ dB}$	-37.5	-33.5	dBm avg	Note 19, 29 Figure 10
Signal Detect Deasserted	P_D	-45	-39.8		dBm avg	Note 20, 30 Figure 10
Signal Detect Hysteresis	$P_A - P_D$	1.5	2.3		dB	Figure 10

Receiver Electrical Characteristics

($T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 4.75\text{ V}$ to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Supply Current	I_{CC}		70	115	mA	Note 21
Supply Current	I_{CCA}		30	50	mA	Note 21
Supply Current – PIN Diode	I_{PD}		35	500	μA	Note 22
Power Dissipation	P_{DISS}		0.3	0.5	W	Note 23
Data Output Voltage – Low	$V_{OL} - V_{CC}$	-1.840		-1.620	V	Note 24
Data Output Voltage – High	$V_{OH} - V_{CC}$	-1.045		-0.880	V	Note 24
Data Output Rise Time	t_r	0.35	1.2	2.2	ns	Note 25
Data Output Fall Time	t_f	0.35	1.1	2.2	ns	Note 25
Duty Cycle Distortion	DCD		0.04	0.4	ns p-p	Note 26
Data Dependent Jitter	DDJ		0.7	1.0	ns p-p	Note 27
Random Jitter	RJ			2.14	ns p-p	Note 28
Signal Detect Output Voltage – Low	$V_{OL} - V_{CC}$	-1.840		-1.620	V	Note 24
Signal Detect Output Voltage – High	$V_{OH} - V_{CC}$	-1.045		-0.880	V	Note 24
Signal Detect Output Rise Time	t_r	0.35	0.9	2.2	ns	Note 24
Signal Detect Output Fall Time	t_f	0.35	0.7	2.2	ns	Note 25
Signal Detect Assert Time (off to on)	AS_Max	0	58	100	μs	Note 19, 29 Figure 10
Signal Detect Deassert Time (on to off)	ANS_Max	0	130	350	μs	Note 20, 30 Figure 10

Notes:

1. This maximum rating applies to still air environments around the transceiver.
2. When component testing these products all supply voltages should be applied simultaneously to avoid damage to the part.
3. This is the maximum voltage that can be applied across the Differential Transmitter Data Inputs to prevent damage to the input ESD protection circuit.
4. When component testing these products do not short the receiver data or signal detect outputs directly to ground to avoid damage to the part.
5. The outputs are terminated with $50\ \Omega$ connected to $V_{CC} - 2\ V$.
6. The specified signaling rate of 10 MBd to 125 MBd guarantees operation of the transmitter and receiver link to the full conditions listed in the FDDI Physical Layer Medium Dependent standard. Specifically, the link bit error ratio will be equal to or better than 2.5×10^{-10} for any valid FDDI pattern. The transmitter section of the link is capable of dc to 125 MBd. The receiver is internally ac-coupled which limits the lower signaling rate to 10 MBd. For purposes of definition, the symbol rate (Baud), also called signaling rate, f_s , is the reciprocal of the shortest symbol time. Data rate (bits/sec) is the symbol rate divided by the encoding factor used to encode the data (symbols/bit).
7. The power supply current needed to operate the transmitter is provided to differential ECL circuitry. This circuitry maintains a nearly constant current flow from the power supply. Constant current operation helps to prevent unwanted electrical noise from being generated, whether the noise is conducted or emitted, to neighboring receiver or logic circuitry.
8. This value is measured with an output load $R_L = 10\ k\Omega$.
9. These optical power values are measured with the following conditions:
 - At the Beginning Of Life (BOL).
 - Over the specified operating voltage and temperature ranges.

- With HALT Line State, (12.5 MHz square-wave), input signal.
- At the end of one meter of noted optical fiber with cladding modes removed.

The average power value can be converted to a peak power value by adding 3 dB. Higher output optical power transmitters are available on special request.

10. The Extinction Ratio is a measure of the modulation depth of the optical signal. The data "0" output optical power is compared to the data "1" peak output optical power and expressed as a percentage. With the transmitter driven by a HALT Line State (12.5 MHz square-wave) signal the optical signal is detected with a receiver that linearly converts optical power to voltage. The extinction ratio is the ratio of the voltage of the "0" level compared to the voltage at the "1" level expressed as a percentage.
11. This parameter complies with the FDDI PMD requirements for the tradeoffs between center wavelength, spectral width, and rise/fall times shown in Figure 7. The temperature coefficient of the center wavelength is typically $+0.39\ nm/^{\circ}C$.
12. This parameter complies with the FDDI PMD requirements for the tradeoffs between center wavelength, spectral width, and rise/fall times shown in Figure 7. The temperature coefficient of the spectral width is typically $+0.25\ nm/^{\circ}C$.
13. This parameter complies with the FDDI PMD requirements for the tradeoffs between center wavelength, spectral width, and rise/fall times shown in Figure 7. This parameter also complies with the optical pulse envelope shown in Figure 8. The optical rise and fall times are measured from 10% to 90% when the transmitter is driven by the FDDI HALT Line State (12.5 MHz square-wave) input signal.
14. Duty Cycle Distortion is measured at a 50% threshold using an IDLE Line State, 125 MBd (62.5 MHz square-wave), input signal. The maximum value for this parameter

is 0.2 ns better than required by the FDDI PMD standard.

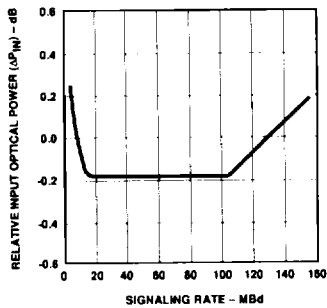
15. Data Dependent Jitter is specified with the FDDI test pattern described in FDDI PMD Annex A.5.
16. Random Jitter is specified with an IDLE Line State, 125 MBd (62.5 MHz square-wave), input signal.
17. This specification is intended to indicate the performance of the receiver section of the transceiver when Input Optical Power signal characteristics are present per the following definitions. The Input Optical Power dynamic range from the minimum level (with a window time-width) to the maximum level is the range over which the receiver is guaranteed to provide output data with a Bit Error Ratio (BER) better than or equal to 2.5×10^{-10} . The BER will be better than or equal to 1×10^{-18} at input optical power levels greater than $P_{IN\ MIN}$ plus approximately 0.8 dB with this Hewlett-Packard receiver. This is 1.2 dB better than required by the FDDI PMD. The measurement conditions are stated below.

- At the Beginning of Life (BOL)
- Over the specified operating temperature and voltage ranges
- Input symbol pattern is the FDDI test pattern defined in FDDI PMD Annex A.5 with 4B/5B NRZI encoded data that contains a duty cycle base-line wander effect of 50 kHz. This sequence causes a near worst case condition for inter-symbol interference.
- Input optical rise and fall times are approximately 1 ns and 2 ns respectively.
- Receiver data window time-width is 2.13 ns or greater and centered at mid-symbol. This worst case window time-width is the minimum allowed eye-opening presented to the FDDI PHY PM_Data.indication input (PHY input) per the example in FDDI PMD Annex E. This minimum window time-width of 2.13 ns is based upon the worst case FDDI PMD Active Input Interface optical conditions for peak-to-peak DCD (1.0 ns), DDJ (1.2 ns) and RJ (0.76 ns) presented to the receiver.

To test a receiver with the worst case FDDI PMD Active Input jitter conditions require exacting control over DCD, DDJ and RJ jitter components that is difficult to implement with production test equipment. The receiver can be equivalently tested to the worst case FDDI PMD input jitter conditions and meet the minimum output data window time-width of 2.13 ns. This is accomplished by using a nearly ideal input optical signal (no DCD, insignificant DDJ and RJ) and measuring for a wider window time-width of 4.6 ns. This is possible due to the accumulative effect of jitter components through their superposition (DCD and DDJ are directly additive and RJ components are rms additive). Specifically, when a nearly ideal input optical test signal is used and the maximum receiver peak-to-peak jitter contributions of DCD (0.4 ns), DDJ (1.0 ns), and RJ (2.14 ns) exist, the minimum window time-width becomes 8.0 ns - 0.4 ns - 1.0 ns - 2.14 ns = 4.46 ns, or conservatively 4.6 ns. This wider window time-width of 4.6 ns guarantees the FDDI PMD Annex E minimum window time-width of 2.13 ns under worst case input jitter conditions to the Hewlett-Packard receiver.

- Transmitter operating with an IDLE Line State pattern, 125 MBd (62.5 MHz square-wave), input signal to simulate any cross-talk present between the transmitter and receiver sections of the transceiver.

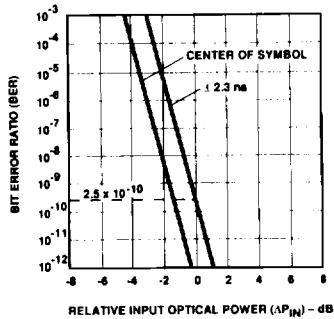
18. All conditions of Note 17 apply except that the measurement is made at the center of the symbol with no window time-width.
19. This value is measured during the transition from low to high levels of input optical power.
20. This value is measured during the transition from high to low levels of input optical power. The minimum value will be either -45 dBm average or when the input optical power yields a BER of 10^{-3} or better, whichever power is higher.
21. These values are measured with the outputs terminated into 50 Ω connected to $V_{CC} - 2 V$.
22. Measured at $P_{IN} = -14$ dBm average.
23. The power dissipation value is the power dissipated in the receiver itself. Power dissipation is calculated as the sum of the products of supply voltage and supply currents, minus the sum of the products of the output voltages and currents.
24. These values are measured with respect to V_{CC} with the output terminated into 50 Ω connected to $V_{CC} - 2 V$. The minimum values are corrected for +5.25 V operation for 100 K ECL values that are usually specified at -4.8 V operation.
25. The output rise and fall times are measured between 20% and 80% levels with the output connected to $V_{CC} - 2 V$ through 50 Ω .
26. Duty Cycle Distortion is measured at 50% threshold using an IDLE Line State, 125 MBd (62.5 MHz square-wave), input signal. The input optical power level is -20 dBm average.
27. Data Dependent Jitter is specified with the FDDI test pattern described in PMD Annex A.5. The input optical power level is -20 dBm average.
28. Random Jitter is specified with an IDLE Line State, 125 MBd (62.5 MHz square-wave), input signal. The input optical power level is at maximum " P_{IN_Max} (W)".
29. The Signal Detect output shall be asserted within 100 μs after a step increase of the Input Optical Power. The step will be from a low Input Optical Power, ≤ -45 dBm, into the range between greater than P_A and -14 dBm. The BER of the receiver output will be 10^{-3} or better during the time, LS_Max (15 μs) after Signal Detect has been asserted. See Figure 10 for more information.
30. Signal detect output shall be de-asserted within 350 μs after a step decrease in the Input Optical Power from a level which is the lower of, -31 dBm or $P_D + 4$ dB (P_D is the power level at which signal detect was deasserted), to a power level of -45 dBm or less. This step decrease will have occurred in less than 8 ns. The receiver output will have a BER of 10^{-3} or better for a period of 12 μs or until signal detect is deasserted. The input data stream is the Quiet Line State. Also, signal detect will be deasserted within a maximum of 350 μs after the BER of the receiver output degrades above 10^{-3} for an input optical data stream that decays with a negative ramp function instead of a step function. See Figure 10 for more information.
31. The transceiver under test was supplied with a 62.5 MHz square wave (125 MBd) optical signal from outside a semi-anechoic chamber to the receiver section located inside this chamber. An input optical power level of -20 dBm average was applied. Electrical output signals from the receiver section were connected directly to the electrical input of the transmitter section of the test transceiver. In turn, the transmitter section returned the optical data to a receiver outside the test chamber to be compared for data integrity. The noise floor of Figure 13 is dictated by the measuring equipment. From DC to one GHz, one set of test instrumentation monitored the emissions. Above 1 GHz, a different instrumentation system measured emissions up to 2 GHz. The difference in the bandwidths of the two systems causes the discontinuity in the noise floor at 1 GHz.
32. Tested at 125 Mb/s and with a data-pattern PRBS 2¹⁷-1. The sampling clock is adjusted to minimum (0.0 ns) delay and incremented in 0.5 ns steps up to a total of 7.5 ns delay. At each clock delay increment, the BER is checked. The total number of delay positions (N) yielding a BER $< 1E-5$ is recorded. The Receiver Saturation level is the highest input optical power at which $N \geq 9$.



CONDITIONS

- 1 P_{IN} NORMALIZED ($\Delta P_{IN} = 0$ dB) TO $P_{IN,MIN}$ (C) AT 125 MBd AT CENTER OF SYMBOL
- 2 $\Delta P_{IN} = P_{IN}$ @ 125 MBd P_{IN} @ 125 MBd
- 3 FDDI PMD APPENDIX A 5 125 MBd TEST PATTERN WITH 50 kHz BASELINE WANDER
- 4 BER = 2.5×10^{-10}
- 5 $T_A = 25^\circ\text{C}$
- 6 $V_{CC} = 5$ Vdc
- 7 INPUT OPTICAL RISE / FALL TIMES : 1.0 ns / 2.1 ns

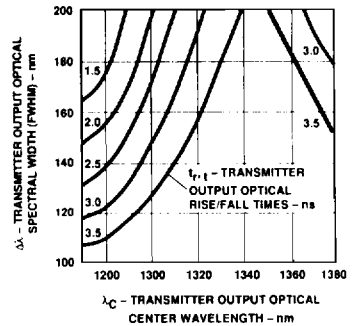
Figure 5. Relative Input Optical Power vs. Signaling Rate.



CONDITIONS

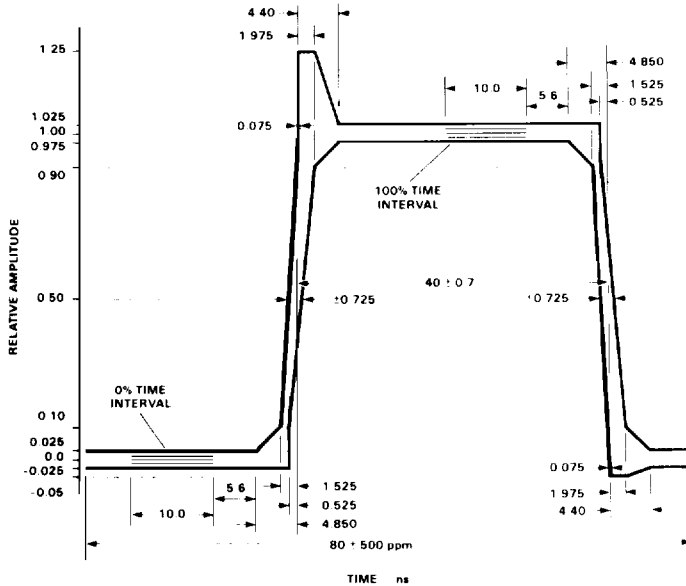
- 1 P_{IN} IS NORMALIZED ($\Delta P_{IN} = 0$ dB) AT $P_{IN,MIN}$ (W) WITH BER = 2.5×10^{-10} AND WINDOW TIME WIDTH OF ± 2.3 ns EITHER SIDE OF SYMBOL CENTER
- 2 $\Delta P_{IN} = P_{IN}$ @ BER = P_{IN} @ 2.5×10^{-10} BER
- 3 FDDI PMD APPENDIX A 5 125 MBd TEST PATTERN WITH 50 kHz BASELINE WANDER
- 4 $T_A = 25^\circ\text{C}$
- 5 $V_{CC} = 5.0$ Vdc
- 6 INPUT OPTICAL RISE / FALL TIMES : 1.0 ns / 2.1 ns

Figure 6. Typical Bit Error Rate vs. Relative Input Optical Power.



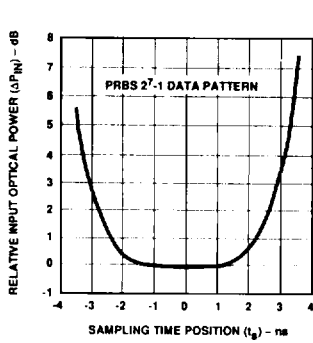
HEWLETT PACKARD FDDI TRANSMITTER TEST RESULTS OF λ_C , $\Delta\lambda$ AND $t_{r,f}$ ARE CORRELATED AND COMPLY WITH THE ALLOWED SPECTRAL WIDTH AS A FUNCTION OF CENTER WAVELENGTH FOR VARIOUS RISE AND FALL TIMES

Figure 7. Transmitter Output Optical Spectral Width (FWHM) vs. Transmitter Output Optical Center Wavelength and Rise/Fall Times.



THE OUTPUT OPTICAL PULSE SHAPE SHALL FIT WITHIN THE BOUNDARIES OF THE PULSE ENVELOPE FOR RISE AND FALL TIME MEASUREMENTS. THE MAXIMUM POSITIVE AND MINIMUM NEGATIVE WAVEFORM EXCURSIONS IN THE ZERO AND 100% TIME INTERVALS SHALL BE CENTERED AROUND THE 0.0 AND 1.00 LEVELS, RESPECTIVELY. A MINIMUM BANDWIDTH RANGE OF 100 KHz TO 750 MHz IS REQUIRED FOR THE MEASUREMENT EQUIPMENT USED TO EVALUATE THE PULSE ENVELOPE

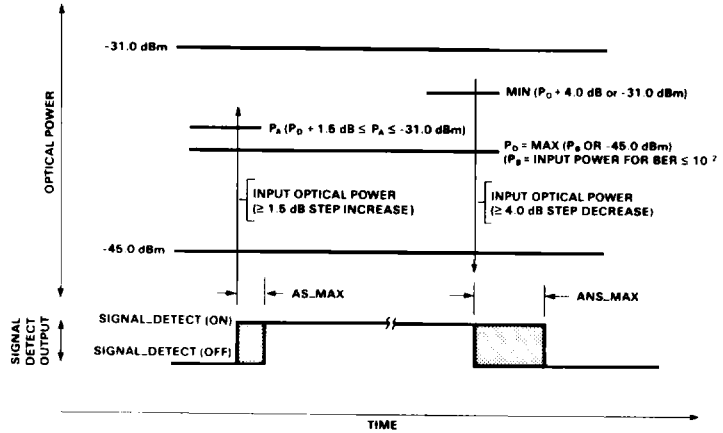
Figure 8. Output Optical Pulse Envelope.



CONDITIONS:

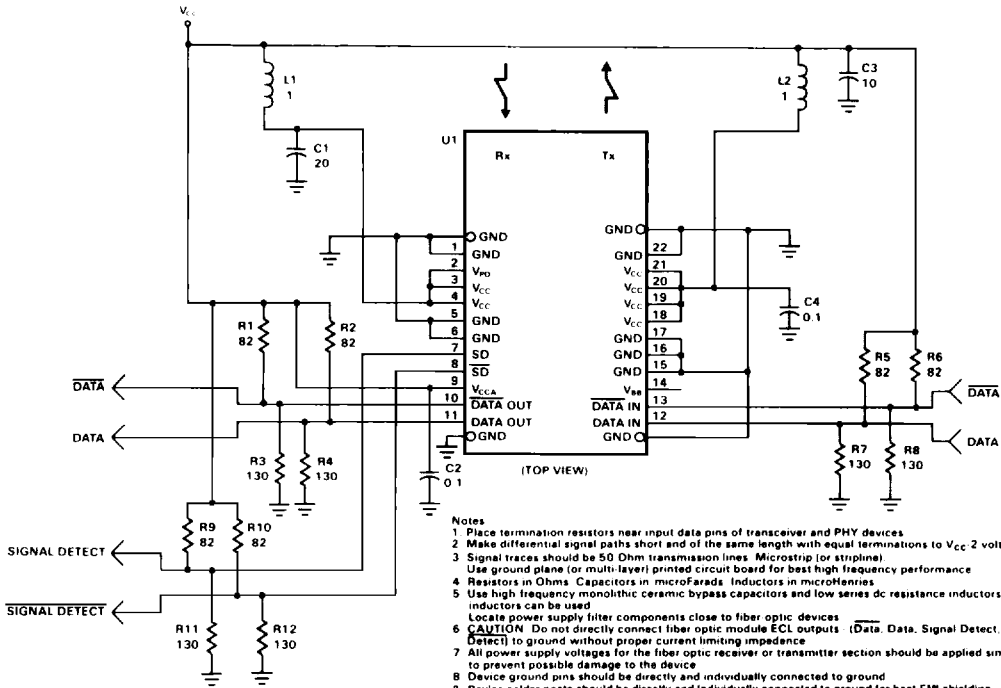
1. PIN IS NORMALIZED TO $P_{IN\ MIN}$ (C) AT CENTER OF SYMBOL.
2. $\Delta P_{IN} = P_{IN} @ t_s - P_{IN} @ t_{CENTER}$
3. PRBS 2^7-1 DATA PATTERN.
4. BER = 2.5×10^{-10}
5. T = 25° C.
6. VCC = 5 Vdc
7. INPUT OPTICAL RISE/FALL TIMES = 1.0 ns/2.1 ns.

Figure 9. Relative Input Optical Power vs. Sampling Time Position.



- AS_MAX**—MAXIMUM ACQUISITION TIME (SIGNAL)
AS_MAX IS THE MAXIMUM SIGNAL_DETECT ASSERTION TIME FOR THE STATION.
AS_MAX SHALL NOT EXCEED 100.0 μ s. THE DEFAULT VALUE OF **AS_MAX** IS 100.0 μ s.
- ANS_MAX**—MAXIMUM ACQUISITION TIME (NO SIGNAL)
ANS_MAX IS THE MAXIMUM SIGNAL_DETECT DEASSERTION TIME FOR A STATION.
ANS_MAX SHALL NOT EXCEED 350 μ s. THE DEFAULT VALUE OF **ANS_MAX** IS 350 μ s.

Figure 10. Signal Detect Thresholds and Timing.



- Notes**
1. Place termination resistors near input data pins of transceiver and PHY devices.
 2. Make differential signal paths short and of the same length with equal terminations to VCC 2 volts.
 3. Signal traces should be 50 Ohm transmission lines. Microstrip (or stripline).
 4. Use ground plane (or multi-layer) printed circuit board for best high frequency performance.
 5. Resistors in Ohms. Capacitors in microfarads. Inductors in microHenries.
 6. Use high frequency monolithic ceramic bypass capacitors and low series dc resistance inductors. Ferrite inductors can be used.
 7. Locate power supply filter components close to fiber optic devices.
 8. **CAUTION:** Do not directly connect fiber optic module ECL outputs (Data, Data, Signal Detect, Signal Detect) to ground without proper current limiting impedance.
 9. All power supply voltages for the fiber optic receiver or transmitter section should be applied simultaneously to prevent possible damage to the device.
 10. Device ground pins should be directly and individually connected to ground.
 11. Device solder posts should be directly and individually connected to ground for best EMI shielding.

Figure 11. Recommended Decoupling Circuit Diagram.

Application Assistance

The Applications Engineering group in the Hewlett-Packard Optical Communication Division is available to assist with the technical understanding and design trade-offs associated with this FDDI transceiver. You can contact them through your local Hewlett-Packard sales representative.

The following information is provided to answer some of the most common application questions that have been asked relative to the use of the HFBR-5101/5102 transceivers.

Board Layout - Decoupling Circuit and Ground Planes

It is important to take care in the layout of your circuit board to achieve optimum performance from the HFBR-5101/5102 transceiver. Figure 11 provides a good example of a schematic for a decoupling circuit that works well with this product. It is further recommended that a contiguous ground plane be provided in the circuit board directly under the transceiver to provide a low inductance ground for signal return current. This recommendation is in keeping with good high frequency board layout practices. Layouts that overlay the multisourced 2X11 footprint with the alternative 1X13 transceiver footprint need to pay special attention to this recommendation for a contiguous ground plane under the transceiver to achieve good performance.

Board Layout - Hole Pattern

Figure 12 shows the recommended board hole pattern to be used for the HFBR-5101/5102 transceivers. This recommenda-

tion complies with the original Multisource FDDI Transceiver definition announced by AT&T, Hewlett-Packard, and Siemens in 1989. This hole size and location recommendation allows for easy insertion of the transceiver into the circuit board during assembly operations.

To interpret Figure 12 it is important to remember to allow

for some positional tolerance beyond the perfect position noted and trade this off for tighter hole size tolerance. For example, if you desire a 0.006 inch tolerance on hole location then the consequent hole size should be held to 0.076 inch minimum instead of 0.070 minimum allowed for the case where the holes would be drilled in the perfect location.

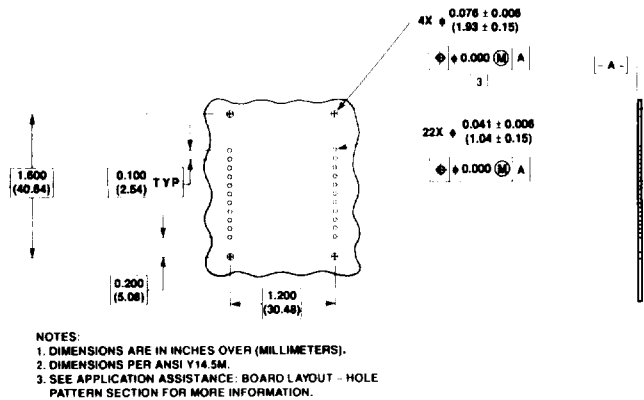


Figure 12. Board Layout - Hole Pattern.

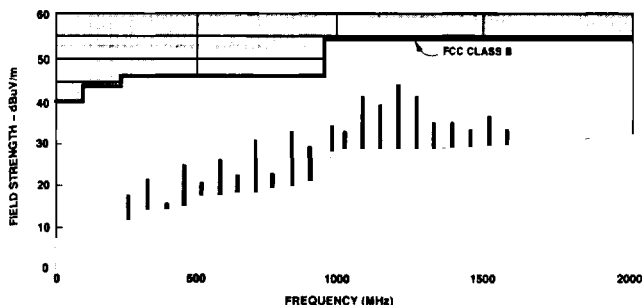


Figure 13. HFBR-5102, Typical Electric Field Strength at 3 m, 125 MBd.

Electromagnetic Emissions

Figure 13 shows typical radiated emissions from a sample of HFBR-5102 transceivers. The units meet FCC Class B far-field emission limits at three metres with the transceiver mounted on a printed circuit board in an open, unshielded environment within an approved semi-anechoic chamber. See note 31 for details on the test method.

Electrostatic Discharge (ESD)

There are two design cases in which immunity to ESD damage is important.

The first case is during handling of the transceiver prior to mounting it on the circuit board. It is important to use normal ESD handling precautions for ESD sensitive devices. These precautions include using grounded wrist straps, work benches, and floor mats in ESD controlled work areas.

The Hewlett-Packard HFBR-5101/5102 has been characterized per MIL-STD-883C Method

3015.4 to tolerate more than 2 kV between pins without damage. This is within the ESD Class 2 specification range of 2000 V to 3999 V.

The second case to consider is static discharges to the exterior of the equipment chassis after the FDDI interface card is installed. In many equipment designs the MIC/R of the FDDI transceiver is exposed outside the exterior of the chassis. With this exposure it is subject to the same ESD test criteria that apply to the entire product in which it is installed. Another specific exposure occurs whenever a Media Interface Connector/Plug is inserted into the transceiver MIC/R.

The Hewlett-Packard HFBR-5101/5102 transceiver has been characterized to withstand up to 25 kV air discharge from a human body source without catastrophic damage. A test procedure similar to IEC 801-2 was used for this characterization test.

When designing equipment the designer should consider the

ESD discharge path to ground. In designs that allow contact between chassis and signal/logic ground this can be accomplished either with a conductive shield or gasket between the chassis and the conductive (aluminum) MIC/R of the HFBR-5101 transceiver, or by connecting the transceiver solder posts and/or ground pins to chassis ground on the circuit board.

In the design case where contact between chassis ground and signal/logic ground is not allowed, the HFBR-5102, which has a non-conductive MIC/R, may be used. To assist an ESD event to transfer to ground, a metal ground plane can be located near the aperture, inside the equipment chassis. This would provide a local, conductive arc-path to ground. Also, this metal can take the form of a guard ring at the peripheral edge of a printed circuit board that is connected to Earth ground. For best EMI/ESD performance, the ground posts should be soldered to the designer's PCB ground.