NEC

MOS INTEGRATED CIRCUIT

μPD44323182, 44323362

32M-BIT CMOS SYNCHRONOUS FAST STATIC RAM
2M-WORD BY 18-BIT / 1M-WORD BY 36-BIT
HSTL INTERFACE / REGISTER-REGISTER / LATE WRITE

Description

The μPD44323182 is a 2,097,152 words by 18 bits, and the μPD44323362 is a 1,048,576 words by 36 bits synchronous static RAM fabricated with advanced CMOS technology using Full-CMOS six-transistor memory cell.

The μPD44323182 and μPD44323362 are suitable for applications which require high-speed, low voltage, high-density memory and wide bit configuration, such as cache and buffer memory.

The μPD44323182 and μPD44323362 are packaged in a 119-pin PLASTIC BGA (Ball Grid Array).

Features

- Fully synchronous operation
- HSTL Input / Output levels
- Fast clock access time: 2.0 ns / 250 MHz, 2.5 ns / 200 MHz
- Asynchronous output enable control: /G
- Byte write control: /SBa (DQa1 to DQa9), /SBb (DQb1 to DQb9), /SBc (DQc1 to DQc9), /SBd (DQd1 to DQd9)
- Common I/O using three-state outputs
- Internally self-timed write cycle
- Late write with 1 dead cycle between Read-Write
- User-configurable outputs: Controlled impedance outputs or push-pull outputs
- Boundary scan (JTAG) IEEE 1149.1 compatible
- 2.5 ± 0.125 V (Chip) / 1.4 to 1.9 V (I/O) supply
- 119 bump BGA package, 1.27 mm pitch, 14 mm × 22 mm
- Sleep mode: ZZ (Enables sleep mode, active high)

Ordering Information

	Part number	Access time	Clock frequency	Package
★	μPD44323182F1-C40-FJ1 Note	2.0 ns	250 MHz	119-pin PLASTIC BGA
★	μPD44323182F1-C50-FJ1 Note	2.5 ns	200 MHz	
	μPD44323362F1-C40-FJ1	2.0 ns	250 MHz	
	μPD44323362F1-C50-FJ1	2.5 ns	200 MHz	

Note Under development

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The mark ★ shows major revised points.

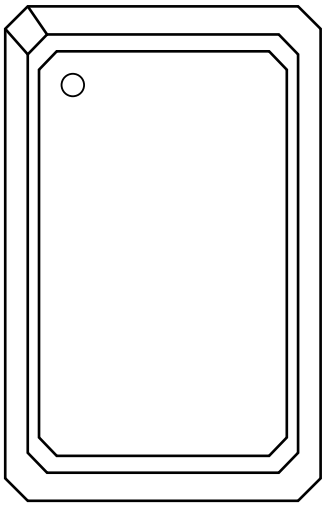
Pin Configurations

/xxx indicates active low signal.

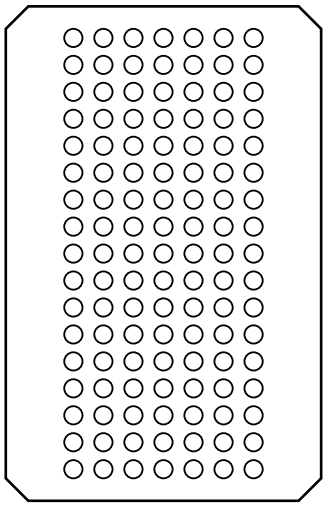
119-pin PLASTIC BGA (2M Words by 18 Bits Pin Assignment)

[μPD44323182F1]

Top View



Bottom View



1 2 3 4 5 6 7

7 6 5 4 3 2 1

1	2	3	4	5	6	7		7	6	5	4	3	2	1
$V_{DD}Q$	SA12	SA9	NC	SA6	SA2	$V_{DD}Q$	A	$V_{DD}Q$	SA2	SA6	NC	SA9	SA12	$V_{DD}Q$
NC	SA19	SA17	SA20	SA16	SA18	NC	B	NC	SA18	SA16	SA20	SA17	SA19	NC
NC	SA13	SA10	V_{DD}	SA7	SA3	NC	C	NC	SA3	SA7	V_{DD}	SA10	SA13	NC
DQb1	NC	V_{SS}	ZQ	V_{SS}	DQa9	NC	D	NC	DQa9	V_{SS}	ZQ	V_{SS}	NC	DQb1
NC	DQb2	V_{SS}	/SS	V_{SS}	NC	DQa8	E	DQa8	NC	V_{SS}	/SS	V_{SS}	DQb2	NC
$V_{DD}Q$	NC	V_{SS}	/G	V_{SS}	DQa7	$V_{DD}Q$	F	$V_{DD}Q$	DQa7	V_{SS}	/G	V_{SS}	NC	$V_{DD}Q$
NC	DQb3	/SBb	NC	NC	NC	DQa6	G	DQa6	NC	NC	NC	/SBb	DQb3	NC
DQb4	NC	V_{SS}	NC	V_{SS}	DQa5	NC	H	NC	DQa5	V_{SS}	NC	V_{SS}	NC	DQb4
$V_{DD}Q$	V_{DD}	V_{REF}	V_{DD}	V_{REF}	V_{DD}	$V_{DD}Q$	J	$V_{DD}Q$	V_{DD}	V_{REF}	V_{DD}	V_{REF}	V_{DD}	$V_{DD}Q$
NC	DQb5	V_{SS}	K	V_{SS}	NC	DQa4	K	DQa4	NC	V_{SS}	K	V_{SS}	DQb5	NC
DQb6	NC	NC	/K	/SBa	DQa3	NC	L	NC	DQa3	/SBa	/K	NC	NC	DQb6
$V_{DD}Q$	DQb7	V_{SS}	/SW	V_{SS}	NC	$V_{DD}Q$	M	$V_{DD}Q$	NC	V_{SS}	/SW	V_{SS}	DQb7	$V_{DD}Q$
DQb8	NC	V_{SS}	SA0	V_{SS}	DQa2	NC	N	NC	DQa2	V_{SS}	SA0	V_{SS}	NC	DQb8
NC	DQb9	V_{SS}	SA1	V_{SS}	NC	DQa1	P	DQa1	NC	V_{SS}	SA1	V_{SS}	DQb9	NC
NC	SA14	M1	V_{DD}	M2	SA4	NC	R	NC	SA4	M2	V_{DD}	M1	SA14	NC
NC	SA15	SA11	NC	SA8	SA5	ZZ	T	ZZ	SA5	SA8	NC	SA11	SA15	NC
$V_{DD}Q$	TMS	TDI	TCK	TDO	NC	$V_{DD}Q$	U	$V_{DD}Q$	NC	TDO	TCK	TDI	TMS	$V_{DD}Q$

Pin Name and Functions [μPD44323182F1]

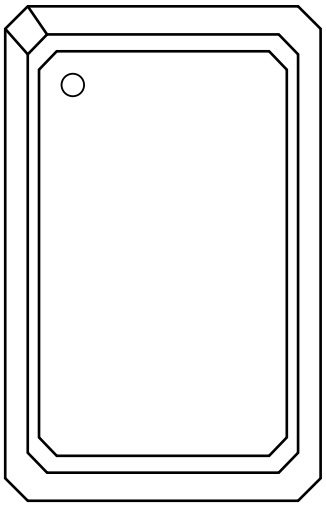
Pin name	Description	Function
V_{DD}	Core Power Supply	Supplies power for RAM core
V_{SS}	Ground	
$V_{DD}Q$	Output Power Supply	Supplies power for output buffers
V_{REF}	Input Reference	
K, /K	Main Clock	
SA0 to SA20	Synchronous Address Input	
DQa1 to DQb9	Synchronous Data Input / Output	
/SS	Synchronous Chip Select	Logically selects SRAM
/SW	Synchronous Byte Write Enable	Write command
/SBa	Synchronous Byte "a" Write Enable	Write DQa1 to DQa9
/SBb	Synchronous Byte "b" Write Enable	Write DQb1 to DQb9
/G	Asynchronous Output Enable	Asynchronous input
ZZ	Asynchronous Sleep Mode	Enables sleep mode, active high
ZQ	Output Impedance Control	
M1, M2	Mode Select	Selects operation mode [Note]
NC	No Connection	
TMS	Test Mode Select (JTAG)	
TDI	Test Data Input (JTAG)	
TCK	Test Clock Input (JTAG)	
TDO	Test Data Output (JTAG)	

Note This device only supports Single Differential Clock, R/R Mode.
(R/R stands for Registered Input / Registered Output.)

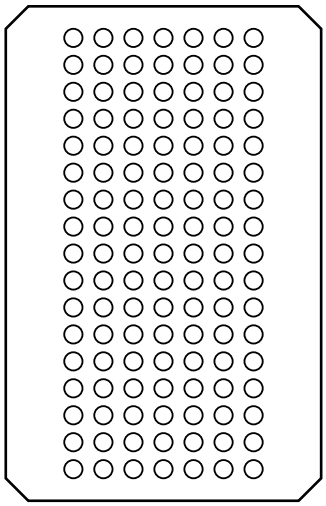
119-pin plastic BGA (1M Words by 36 Bits Pin Assignment)

[μPD44323362F1]

Top View



Bottom View



1	2	3	4	5	6	7	
$V_{DD}Q$	SA12	SA9	NC	SA5	SA2	$V_{DD}Q$	A
NC	SA18	SA16	SA19	SA15	SA17	NC	B
NC	SA13	SA10	V_{DD}	SA6	SA3	NC	C
DQc8	DQc9	V_{SS}	ZQ	V_{SS}	DQb9	DQb8	D
DQc6	DQc7	V_{SS}	/SS	V_{SS}	DQb7	DQb6	E
$V_{DD}Q$	DQc5	V_{SS}	/G	V_{SS}	DQb5	$V_{DD}Q$	F
DQc3	DQc4	/SBc	NC	/SBb	DQb4	DQb3	G
DQc1	DQc2	V_{SS}	NC	V_{SS}	DQb2	DQb1	H
$V_{DD}Q$	V_{DD}	V_{REF}	V_{DD}	V_{REF}	V_{DD}	$V_{DD}Q$	J
DQd1	DQd2	V_{SS}	K	V_{SS}	DQa2	DQa1	K
DQd3	DQd4	/SBd	/K	/SBa	DQa4	DQa3	L
$V_{DD}Q$	DQd5	V_{SS}	/SW	V_{SS}	DQa5	$V_{DD}Q$	M
DQd6	DQd7	V_{SS}	SA0	V_{SS}	DQa7	DQa6	N
DQd8	DQd9	V_{SS}	SA1	V_{SS}	DQa9	DQa8	P
NC	SA14	M1	V_{DD}	M2	SA4	NC	R
NC	NC	SA11	SA8	SA7	NC	ZZ	T
$V_{DD}Q$	TMS	TDI	TCK	TDO	NC	$V_{DD}Q$	U

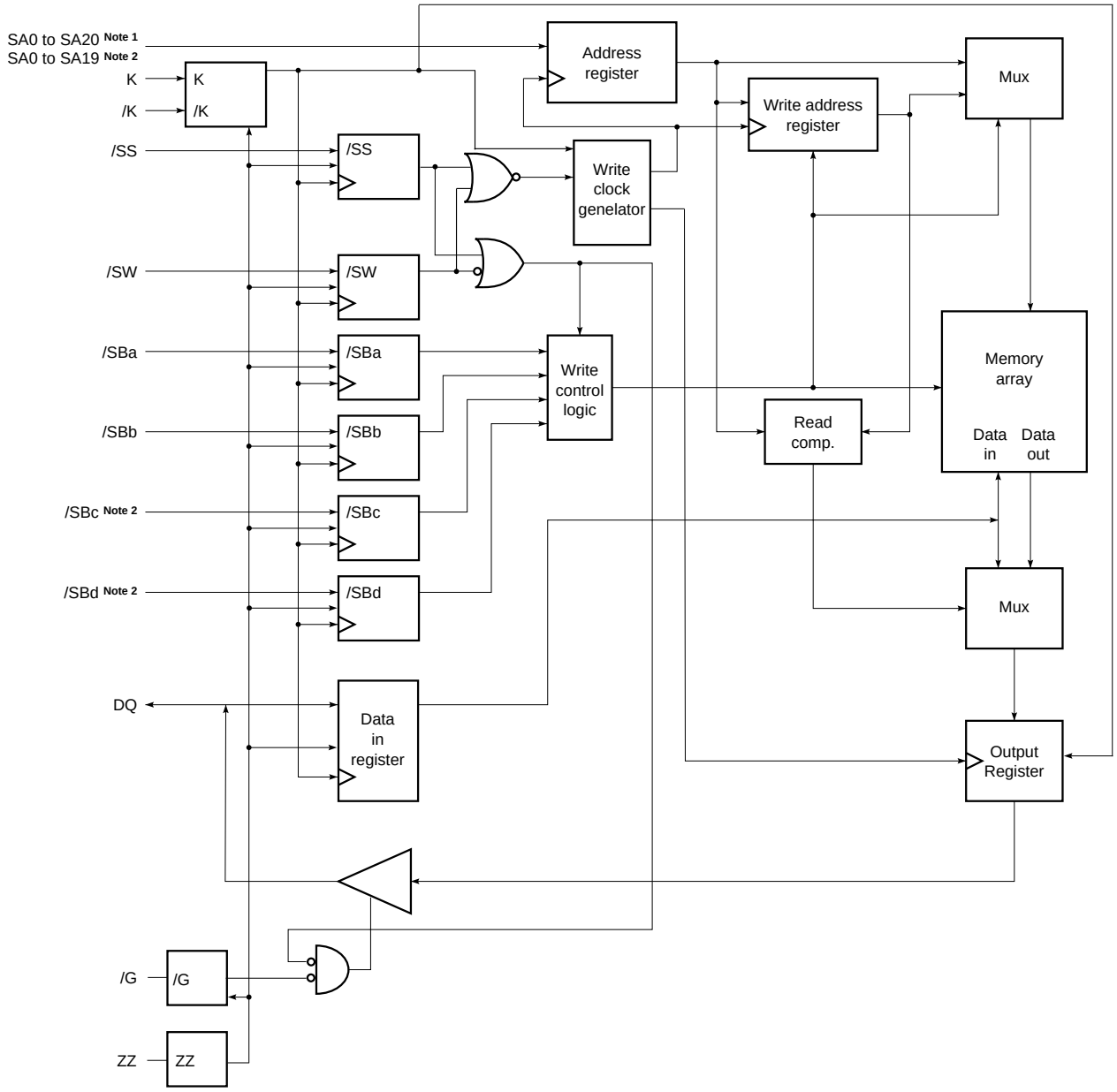
7	6	5	4	3	2	1
$V_{DD}Q$	SA2	SA5	NC	SA9	SA12	$V_{DD}Q$
NC	SA17	SA15	SA19	SA16	SA18	NC
NC	SA3	SA6	V_{DD}	SA10	SA13	NC
DQb8	DQb9	V_{SS}	ZQ	V_{SS}	DQc9	DQc8
DQb6	DQb7	V_{SS}	/SS	V_{SS}	DQc7	DQc6
$V_{DD}Q$	DQb5	V_{SS}	/G	V_{SS}	DQc5	$V_{DD}Q$
DQb3	DQb4	/SBb	NC	/SBc	DQc4	DQc3
DQb1	DQb2	V_{SS}	NC	V_{SS}	DQc2	DQc1
$V_{DD}Q$	V_{DD}	V_{REF}	V_{DD}	V_{REF}	V_{DD}	$V_{DD}Q$
DQa1	DQa2	V_{SS}	K	V_{SS}	DQd2	DQd1
DQa3	DQa4	/SBa	/K	/SBd	DQd4	DQd3
$V_{DD}Q$	DQa5	V_{SS}	/SW	V_{SS}	DQd5	$V_{DD}Q$
DQa6	DQa7	V_{SS}	SA0	V_{SS}	DQd7	DQd6
DQa8	DQa9	V_{SS}	SA1	V_{SS}	DQd9	DQd8
NC	SA4	M2	V_{DD}	M1	SA14	NC
ZZ	NC	SA7	SA8	SA11	NC	NC
$V_{DD}Q$	NC	TDO	TCK	TDI	TMS	$V_{DD}Q$

Pin Name and Functions [μPD44323362F1]

Pin name	Description	Function
V_{DD}	Core Power Supply	Supplies power for RAM core
V_{SS}	Ground	
$V_{DD}Q$	Output Power Supply	Supplies power for output buffers
V_{REF}	Input Reference	
K, /K	Main Clock	
SA0 to SA19	Synchronous Address Input	
DQa1 to DQd9	Synchronous Data Input / Output	
/SS	Synchronous Chip Select	Logically selects SRAM
/SW	Synchronous Byte Write Enable	Write command
/SBa	Synchronous Byte "a" Write Enable	Write DQa1 to DQa9
/SBb	Synchronous Byte "b" Write Enable	Write DQb1 to DQb9
/SBc	Synchronous Byte "c" Write Enable	Write DQc1 to DQc9
/SBd	Synchronous Byte "d" Write Enable	Write DQd1 to DQd9
/G	Asynchronous Output Enable	Asynchronous input
ZZ	Asynchronous Sleep Mode	Enables sleep mode, active high
ZQ	Output Impedance Control	
M1, M2	Mode Select	Selects operation mode [Note]
NC	No Connection	
TMS	Test Mode Select (JTAG)	
TDI	Test Data Input (JTAG)	
TCK	Test Clock Input (JTAG)	
TDO	Test Data Output (JTAG)	

Note This device only supports Single Differential Clock, R/R Mode.
(R/R stands for Registered Input / Registered Output.)

Late Write Block Diagram



Notes **1.** SA0 to SA20 are used in the μPD44323182.

2. SA0 to SA19, /SBc and /SBd are used in the μPD44323362.

Programmable Impedance / Power Up Requirements

An external resistor, RQ, must be connected between the ZQ pin on the SRAM and V_{SS} to allow for the SRAM to adjust its output driver impedance. The value of RQ must be 5X the value of the intended line impedance driven by the SRAM. The allowable range of RQ to guarantee impedance matching with a tolerance of 15% is between 175 ohm and 350 ohm. Periodic readjustment of the output driver impedance is necessary as the impedance is greatly affected by drifts in supply voltage and temperature. The impedance update of the output driver occurs only when the SRAM is in high impedance. Write and Deselect operations will synchronously switch the SRAM into and out of high impedance, therefore, triggering an update. Power up requirements for the SRAM are that V_{DD} must be powered before or simultaneously with $V_{DD}Q$ followed by V_{REF}; inputs should be powered last. The limitation on $V_{DD}Q$ is that it must not exceed V_{DD} during power up. In order to guarantee the optimum internally regulated supply voltage, the SRAM requires 4096 clock cycles of power-up time after V_{DD} reaches its operating range. And CID impedance is not updated during the clock stopped.

Sleep Mode

Sleep Mode is enabled by switching asynchronous signal ZZ High. When the SRAM is in Sleep Mode, the output will go to a high impedance state and the SRAM will draw standby current. SRAM data will be preserved and a recovery time (t_{ZZR}) is required before the SRAM resumes normal operation. And CID impedance is not updated during the sleep mode.

Synchronous Truth Table

ZZ	/SS	/SW	/SBa	/SBb	/SBc	/SBd	Mode	DQa1 to DQa9	DQb1 to DQb9	DQc1 to DQc9	DQd1 to DQd9	Power
L	H	×	×	×	×	×	Not selected	High-Z	High-Z	High-Z	High-Z	Active
L	L	H	×	×	×	×	Read	Dout	Dout	Dout	Dout	Active
L	L	L	L	L	L	L	Write	Din	Din	Din	Din	Active
L	L	L	L	H	H	H	Write	Din	High-Z	High-Z	High-Z	Active
L	L	L	H	L	L	L	Write	High-Z	Din	Din	Din	Active
H	×	×	×	×	×	×	Sleep Mode	High-Z	High-Z	High-Z	High-Z	Standby

Remark × : Don't care

Output Enable Truth Table

Mode	/G	DQ
Read	L	Dout
Read	H	High-Z
Sleep (ZZ = H)	×	High-Z
Write (/SW = L)	×	High-Z
Deselect (/SS = H)	×	High-Z

Mode Select (I/O) [Note 1]

M1	M2	Mode
V_{SS}	V_{DD}	Single Differential Clock (K, /K), R/R Mode [Note 2]

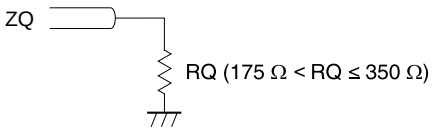
Notes **1.** This device only supports Single Differential Clock, R/R Mode. Mode Select Pins (M1, M2) are to be tied to either V_{DD} or V_{SS}.

2. R/R: Registered Input / Registered Output

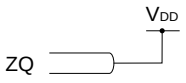
Mode Select (Output Buffer)

ZQ	Mode	Note
IZQ × RQ	Controlled impedance push-pull output buffer mode	1
V_{DD}	Push-pull output buffer mode	2

Notes **1.** See figure.



2. See figure.



Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit	Note
Supply voltage	V_{DD}		–0.5		+3.0	V	1
Output supply voltage	V_{DDQ}		–0.5		+3.0	V	1
Input voltage	V_{IN}		–0.5		V_{DD} + 0.3 (3.0 V MAX)	V	1
Input / Output voltage	$V_{I/O}$		–0.5		V_{DD} + 0.3 (3.0 V MAX)	V	1
Operating temperature	T_j		5		110	°C	2
Storage temperature	T_{stg}		–55		+125	°C	

Notes 1. –1.0 V MIN. (Pulse width 10% Tcyc)

2. T_j = Junction temperature

Caution Exposing the device to stress above those listed in Absolute Maximum Rating could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions (T_j = 5 to 110 °C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Core supply voltage	V_{DD}		2.375	2.5	2.625	V
Output buffer supply voltage	V_{DDQ}		1.4		1.9	V
Input reference voltage	V_{REF}		0.68		0.95	V
Low level input voltage	V_{IL}		–0.3 Note		V_{REF} – 0.1	V
High level input voltage	V_{IH}		V_{REF} + 0.1		V_{DDQ} + 0.3	V

Note –1.0 V MIN. (Pulse width 10% Tcyc)

Recommended AC Operating Conditions (T_j = 5 to 110 °C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input reference voltage	$V_{REF (RMS)}$		–5%		+5%	V
Low level input voltage	V_{IL}		–0.3		V_{REF} – 0.2	V
High level input voltage	V_{IH}		V_{REF} + 0.2		V_{DDQ} + 0.3	V

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter Note	Symbol	Test conditions	MAX.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V	6	pF
Input / Output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V	7	pF
★ Clock input capacitance	C_{clk}	V_{clk} = 0 V	7	pF

Note These parameters are sampled and not 100% tested.

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
	Input leakage current	I_{LI}	V_{IN} = 0 to V_{DD}	–5		+5	μA
	DQ leakage current	I_{LO}	$V_{I/O}$ = 0 to $V_{DD}Q$, /SS = V_{IH} or /G = V_{IH}	–5		+5	μA
	Operating supply current	I_{CC}	V_{IN} = V_{IH} or V_{IL}, /SS = V_{IL}, ZZ = V_{IL}, cycle = 250 MHz, IDQ = 0 mA			550	mA
★	Quiescent active power supply current	I_{CC2}	V_{IN} = V_{IH} or V_{IL}, /SS = V_{IL}, ZZ = V_{IL}, Cycle = 4 MHz, IDQ = 0 mA			250	mA
	Sleep mode power supply current	I_{SBZZ}	ZZ = V_{IH}, All other inputs = V_{IH} or V_{IL}, Cycle = DC, IDQ = 0 mA			150	mA
★	Power supply standby current	I_{SBSS}	V_{IN} = V_{IH} or V_{IL}, /SS = V_{IH}, ZZ = V_{IL}, Cycle = 250 MHz, IDQ = 0 mA			300	mA

Output Voltage on Controlled Impedance Push-Pull Output Buffer Mode (VZQ = IZQ × RQ)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Low level output voltage	V_{OL}	I_{OL} = ($V_{DD}Q$/2) / (RQ/5) ± 15% @V_{OL} = $V_{DD}Q$ / 2 (175 Ω < RQ < 350 Ω)	V_{SS}		$V_{DD}Q$/2	V
High level output voltage	V_{OH}	I_{OH} = ($V_{DD}Q$/2) / (RQ/5) ± 15% @V_{OH} = $V_{DD}Q$ / 2 (175 Ω < RQ < 350 Ω)	$V_{DD}Q$/2		$V_{DD}Q$	V

Output Voltage on Push-Pull Output Buffer Mode (VZQ = V_{DD})

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Low level output voltage	V_{OL}	I_{OL} = +4 mA	–		0.3	V
High level output voltage	V_{OH}	I_{OH} = –4 mA	$V_{DD}Q$ – 0.3		–	V

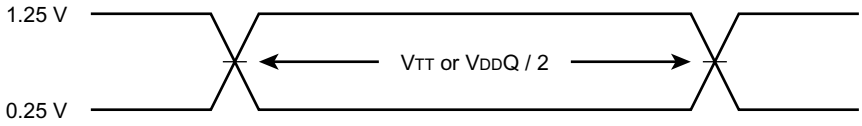
AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

AC Characteristics Test Conditions (T_A = 0 to 70 °C, V_{DD} = 2.375 to 2.625 V, $V_{DD}Q$ = 1.5 V)

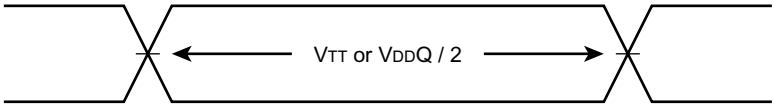
Parameter	Symbol	Conditions	Unit
High level input voltage	V_{IH}	1.25	V
Low level input voltage	V_{IL}	0.25	V
Input reference voltage	V_{REF}	0.75	V
Input rise time	T_R	0.5	ns
Input fall time	T_F	0.5	ns
Input and output timing reference level		Cross point	

Remark Parameter tested with RQ = 250 Ω and $V_{DD}Q$ = 1.5 V.

Input waveform (rise and fall time = 0.5 ns (20 to 80%))



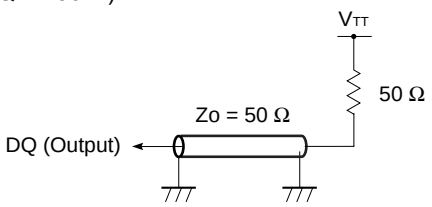
Output waveform



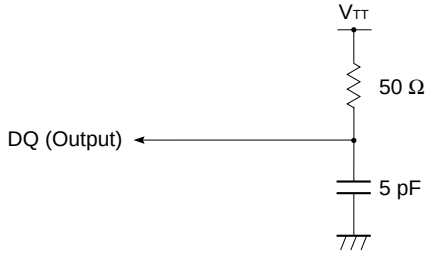
Read and Write Cycle

Parameter		Symbol	-C40 (250 MHz)		-C50 (200 MHz)		Unit	Note
			MIN.	MAX.	MIN.	MAX.		
Clock cycle time		t_{KHKH}	4.0	–	5.0	–	ns	
Clock phase time		t_{KHKL} / t_{KLKH}	1.5	–	1.5	–	ns	
Setup times	Address	t_{AVKH}	0.5	–	0.5	–	ns	
	Write data	t_{DVKH}						
	Write enable	t_{WVKH}						
	Chip select	t_{SVKH}						
Hold times	Address	t_{KHAX}	0.5	–	1.0	–	ns	
	Write data	t_{KHDX}						
	Write enable	t_{KHWX}						
	Chip select	t_{KHSX}						
Clock access time		t_{KHQV}	–	2.0	–	2.5	ns	1
K high to Q change		t_{KHQX}	0.5	–	0.5	–	ns	2
/G low to Q valid		t_{GLQV}	–	2.0	–	2.5	ns	1
/G low to Q change		t_{GLQX}	0.5	–	0.5	–	ns	2
/G high to Q High-Z		t_{GHQZ}	1.0	2.0	1.0	2.5	ns	2
K high to Q High-Z (/SW)		t_{KHQZ}	1.0	2.5	1.0	3.0	ns	2
K high to Q High-Z (/SS)		t_{KHQZ2}	1.0	2.5	1.0	3.0	ns	2
K high to Q Low-Z		t_{KHQX2}	0.7	–	0.7	–	ns	
/G high Pulse width		t_{GHGL}	4.0	–	5.0	–	ns	3
/G high to K high		t_{GHKH}	1.0	–	1.0	–	ns	3
K high to /G low		t_{KHGL}	2.5	–	2.5	–	ns	3
Sleep mode recovery		t_{ZZR}	2	–	2	–	Cycle	4
Sleep mode enable		t_{ZZE}	–	2	–	2	Cycle	4

Notes 1. See figure. (V_{TT} = 0.75 V, RQ = 250 Ω)



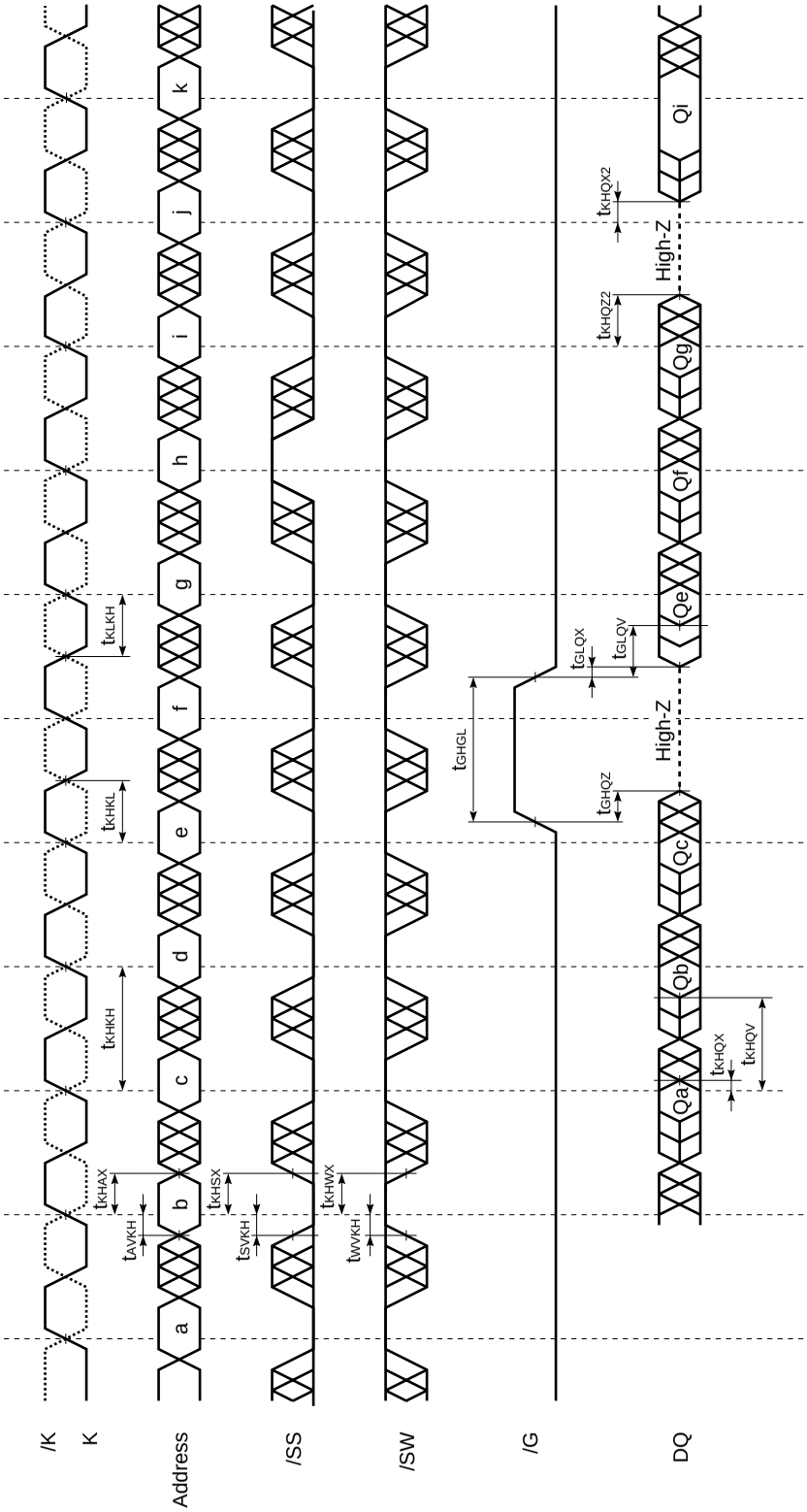
2. See figure. (V_{TT} = 0.75 V, RQ = 250 Ω)



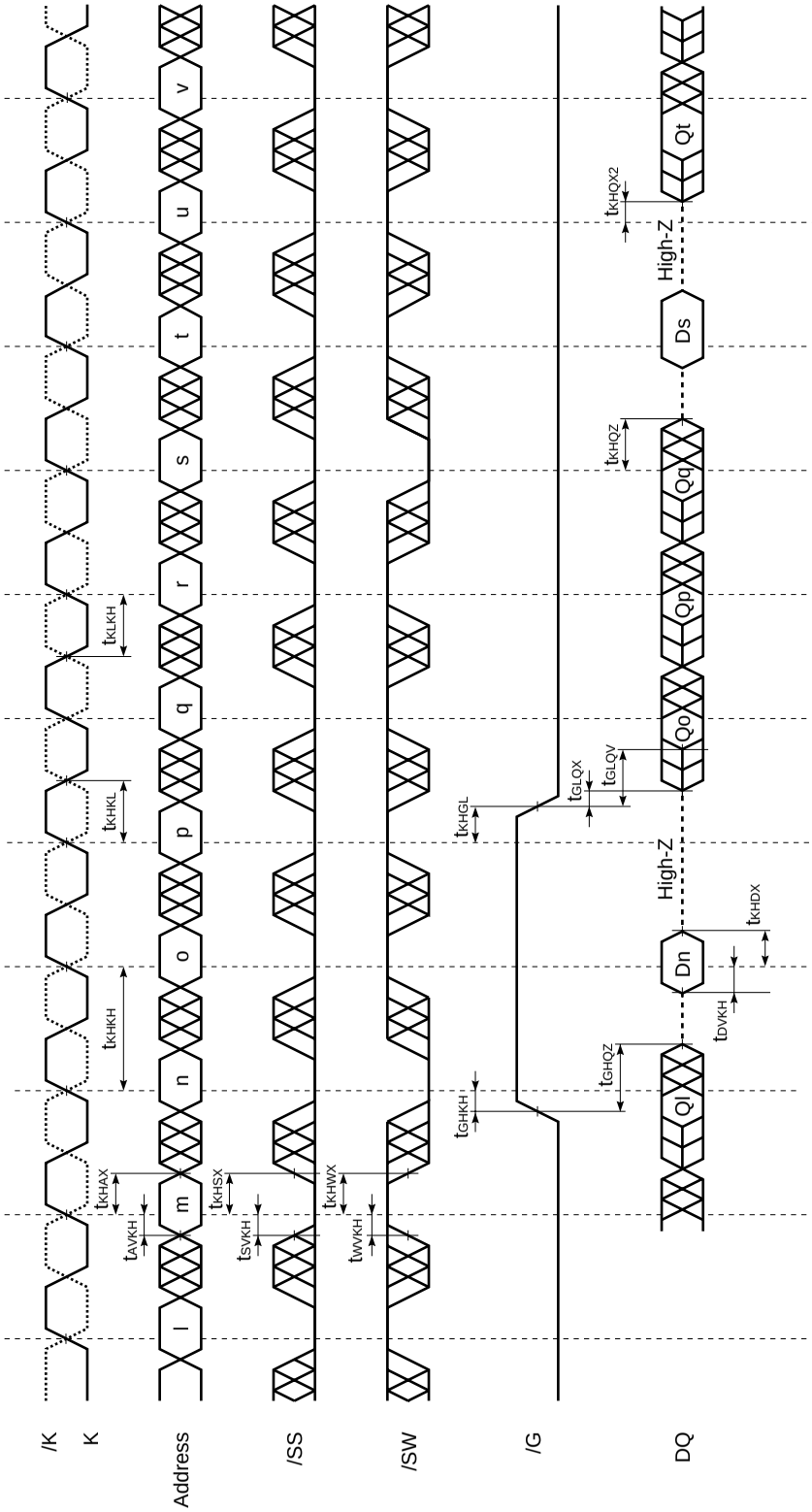
3. Controlled impedance push-pull output buffer mode only.

4. /SS must be 'high' before sleep mode entry.

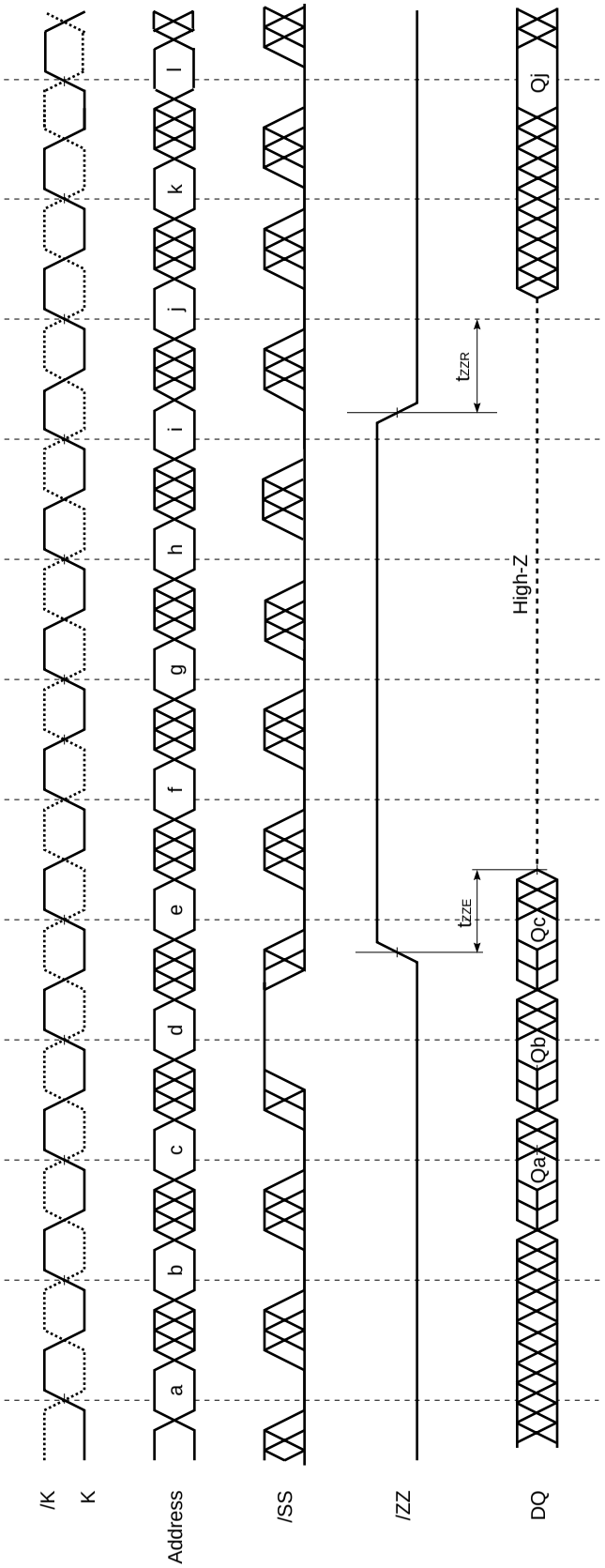
Read Operation



Write Operation



Sleep Mode



JTAG Specifications

The μPD44323182 and μPD44323362 support a limited set of JTAG functions as in IEEE standard 1149.1.

Test Access Port (TAP) Pins

Pin name	Pin assignments	Description
TCK	4 U	Test Clock Input. All input are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.
TMS	2 U	Test Mode Select. This is the command input for the TAP controller state machine.
TDI	3 U	Test Data Input. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction.
TDO	5 U	Test Data Output. Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

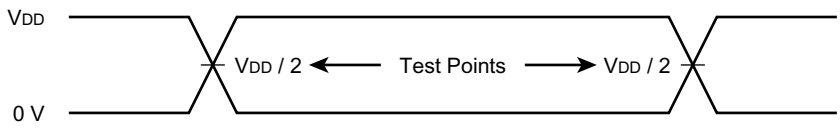
Remark The device does not have TRST (TAP reset). The Test-Logic Reset state is entered while TMS is held high for five rising edges of TCK. The TAP controller state is also reset on the SRAM POWER-UP.

JTAG DC Characteristics (T_j = 5 to 110 °C)

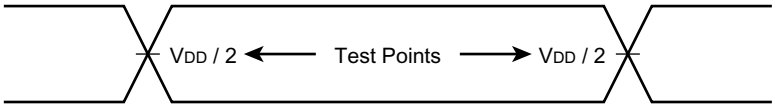
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
JTAG input high voltage	V_{IH}		2.2		V_{DD} + 0.3 (3.0 V MAX)	V	
JTAG input low voltage	V_{IL}		–0.3		+0.5	V	
JTAG output high voltage	V_{OH}	I_{OH} = –8 mA	2.4		–	V	
JTAG output low voltage	V_{OL}	I_{OL} = 8 mA	–		0.4	V	

JTAG AC Test Conditions (T_j = 5 to 110 °C)

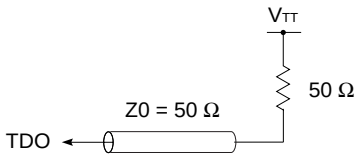
Input waveform (rise / fall time = 1 ns (20 to 80%))



Output waveform



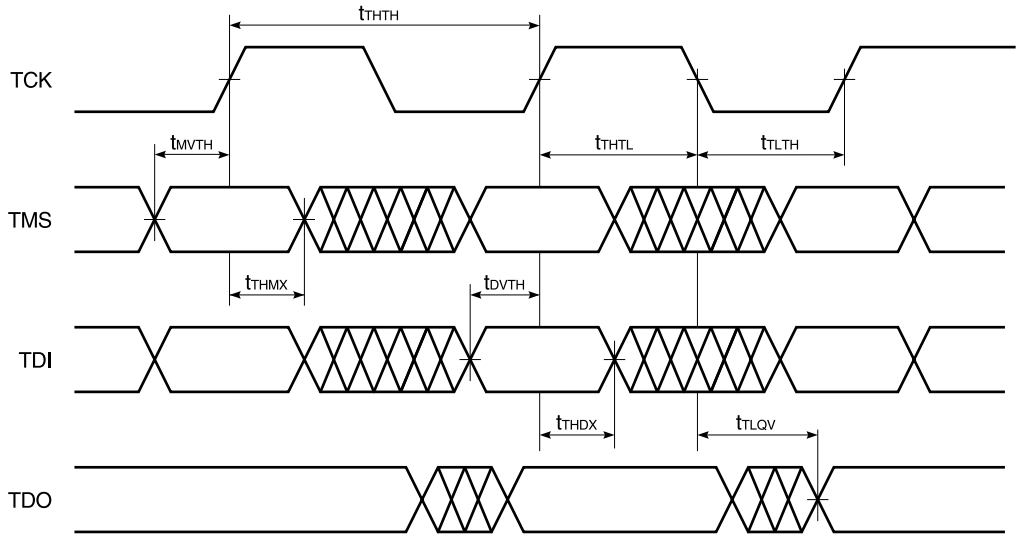
Output load (V_{TT} = 1.5 V)



JTAG AC Characteristics (T_j = 5 to 110 °C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Clock cycle time (TCK)	t_{THTH}		100		–	ns	
Clock phase time (TCK)	t_{THTL} / t_{TLTH}		40		–	ns	
Setup time (TMS / TDI)	t_{MVTH} / t_{DVTH}		10		–	ns	
Hold time (TMS / TDI)	t_{THMX} / t_{THDX}		10		–	ns	
TCK low to TDO valid (TDO)	t_{TLQV}		–		20	ns	

JTAG Timing Diagram



Scan Register Definition (1)

Register name	Description
Instruction register	The instruction register holds the instructions that are executed by the TAP controller when it is moved into the run-test/idle or the various data register state. The register can be loaded when it is placed between the TDI and TDO pins. The instruction register is automatically preloaded with the IDCODE instruction at power-up whenever the controller is placed in test-logic-reset state.
Bypass register	The bypass register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAMs TAP to another device in the scan chain with as little delay as possible.
ID register	The ID Register is a 32 bit register that is loaded with a device and vendor specific 32 bit code when the controller is put in capture-DR state with the IDCODE command loaded in the instruction register. The register is then placed between the TDI and TDO pins when the controller is moved into shift-DR state.
Boundary register	The boundary register, under the control of the TAP controller, is loaded with the contents of the RAMs I/O ring when the controller is in capture-DR state and then is placed between the TDI and TDO pins when the controller is moved to shift-DR state. Several TAP instructions can be used to activate the boundary register. The Scan Exit Order tables describe which device bump connects to each boundary register location. The first column defines the bit's position in the boundary register. The shift register bit nearest TDO (i.e., first to be shifted out) is defined as bit 1. The second column is the name of the input or I/O at the bump and the third column is the bump number

Scan Register Definition (2)

Register name	μPD44323182	μPD44323362	Unit
Instruction register	3	3	bit
Bypass register	1	1	bit
ID register	32	32	bit
Boundary register	51	70	bit

★ **ID Register Definition**

Part number	Organization	ID [31:28] vendor revision no.	ID [27:12] part no.	ID [11:1] vendor ID no.	ID [0] fix bit
μPD44323182	2M × 18	XXXX	0000 0000 0011 1011	00000010000	1
μPD44323362	1M × 36	XXXX	0000 0000 0011 1100	00000010000	1

SCAN Exit Order

[μPD44323182 (2M words by 18 bits)]

Bit no.	Signal name	Bump ID
1	M2	5R
2	SA5	6T
3	SA1	4P
4	SA4	6R
5	SA8	5T
6	ZZ	7T
7	DQa1	7P
8	DQa2	6N
9	DQa3	6L
10	DQa4	7K
11	/SBa	5L
12	/K	4L
13	K	4K
14	/G	4F
15	DQa5	6H
16	DQa6	7G
17	DQa7	6F
18	DQa8	7E
19	DQa9	6D
20	SA2	6A
21	SA3	6C
22	SA7	5C
23	SA6	5A
24	SA18	6B
25	SA16	5B

Bit no.	Signal name	Bump ID
26	SA17	3B
27	SA19	2B
28	SA9	3A
29	SA10	3C
30	SA13	2C
31	SA12	2A
32	DQb1	1D
33	DQb2	2E
34	DQb3	2G
35	DQb4	1H
36	/SBb	3G
37	ZQ	4D
38	/SS	4E
39	SA20	4B
40	NC	4H
41	/SW	4M
42	DQb5	2K
43	DQb6	1L
44	DQb7	2M
45	DQb8	1N
46	DQb9	2P
47	SA11	3T
48	SA14	2R
49	SA0	4N
50	SA15	2T
51	M1	3R

[μPD44323362 (1M words by 36 bits)]

Bit no.	Signal name	Bump ID
1	M2	5R
2	SA1	4P
3	SA8	4T
4	SA4	6R
5	SA7	5T
6	ZZ	7T
7	DQa9	6P
8	DQa8	7P
9	DQa7	6N
10	DQa6	7N
11	DQa5	6M
12	DQa4	6L
13	DQa3	7L
14	DQa2	6K
15	DQa1	7K
16	/SBa	5L
17	/K	4L
18	K	4K
19	/G	4F
20	/SBb	5G
21	DQb1	7H
22	DQb2	6H
23	DQb3	7G
24	DQb4	6G
25	DQb5	6F
26	DQb6	7E
27	DQb7	6E
28	DQb8	7D
29	DQb9	6D
30	SA2	6A
31	SA3	6C
32	SA6	5C
33	SA5	5A
34	SA17	6B
35	SA15	5B

Bit no.	Signal name	Bump ID
36	SA16	3B
37	SA18	2B
38	SA9	3A
39	SA10	3C
40	SA13	2C
41	SA12	2A
42	DQc9	2D
43	DQc8	1D
44	DQc7	2E
45	DQc6	1E
46	DQc5	2F
47	DQc4	2G
48	DQc3	1G
49	DQc2	2H
50	DQc1	1H
51	/SBc	3G
52	ZQ	4D
53	/SS	4E
54	SA19	4B
55	NC	4H
56	/SW	4M
57	/SBd	3L
58	DQd1	1K
59	DQd2	2K
60	DQd3	1L
61	DQd4	2L
62	DQd5	2M
63	DQd6	1N
64	DQd7	2N
65	DQd8	1P
66	DQd9	2P
67	SA11	3T
68	SA14	2R
69	SA0	4N
70	M1	3R

JTAG Instructions

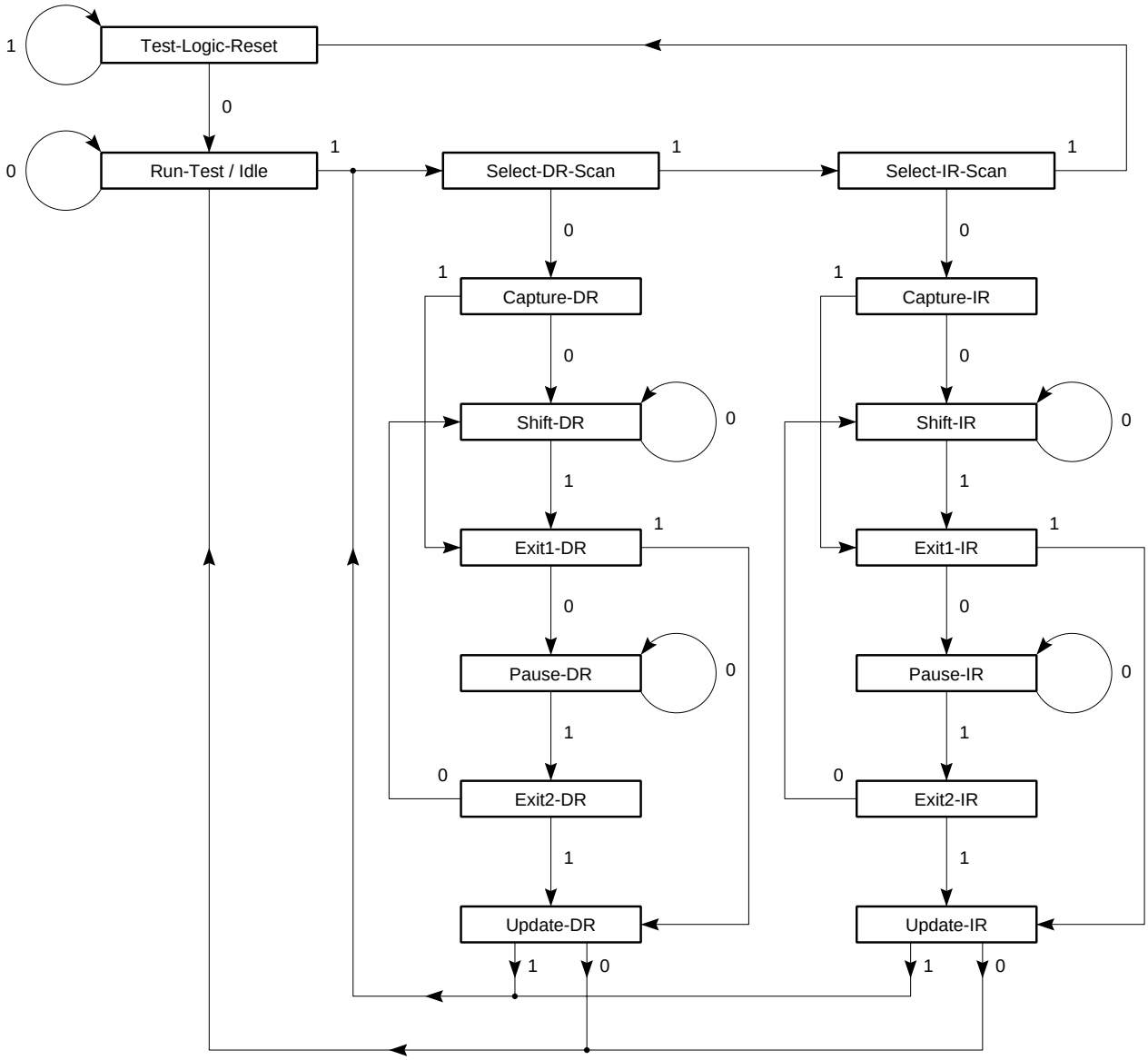
Instructions	Description
EXTEST	EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register, whatever length it may be in the device, is loaded with all logic 0s. EXTEST is not implemented in this device. Therefore this device is not 1149.1 compliant. Nevertheless, this RAMs TAP does respond to an all zeros instruction, as follows. With the EXTEST (000) instruction loaded in the instruction register the RAM responds just as it does in response to the SAMPLE instruction, except the RAM output are forced to high impedance any time the instruction is loaded.
IDCODE	The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in capture-DR mode and places the ID register between the TDI and TDO pins in shift-DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the test-logic-reset state.
BYPASS	The BYPASS instruction is loaded in the instruction register when the bypass register is placed between TDI and TDO. This occurs when the TAP controller is moved to the shift-DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.
SAMPLE	Sample is a Standard 1149.1 mandatory public instruction. When the sample instruction is loaded in the instruction register, moving the TAP controller into the capture-DR state loads the data in the RAMs input and I/O buffers into the boundary scan register. Because the RAM clock(s) are independent from the TAP clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e., in a metastable state). Although allowing the TAP to sample metastable input will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture setup plus hold time (t_{CS} plus t_{CH}). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the boundary scan register. Moving the controller to shift-DR state then places the boundary scan register between the TDI and TDO pins. This functionality is not Standard 1149.1 compliant.
SAMPLE-Z	If the SAMPLE-Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (high impedance) and the boundary register is connected between TDI and TDO when the TAP controller is moved to the shift-DR state.

JTAG Instruction Cording

IR2	IR1	IR0	Instruction	Note
0	0	0	EXTEST	1
0	0	1	IDCODE	
0	1	0	SAMPLE-Z	1
0	1	1	BYPASS	
1	0	0	SAMPLE	
1	0	1	BYPASS	
1	1	0	BYPASS	
1	1	1	BYPASS	

Note 1. TRISTATE all data drivers and CAPTURE the pad values into a SERIAL SCAN LATCH.

TAP Controller State Diagram



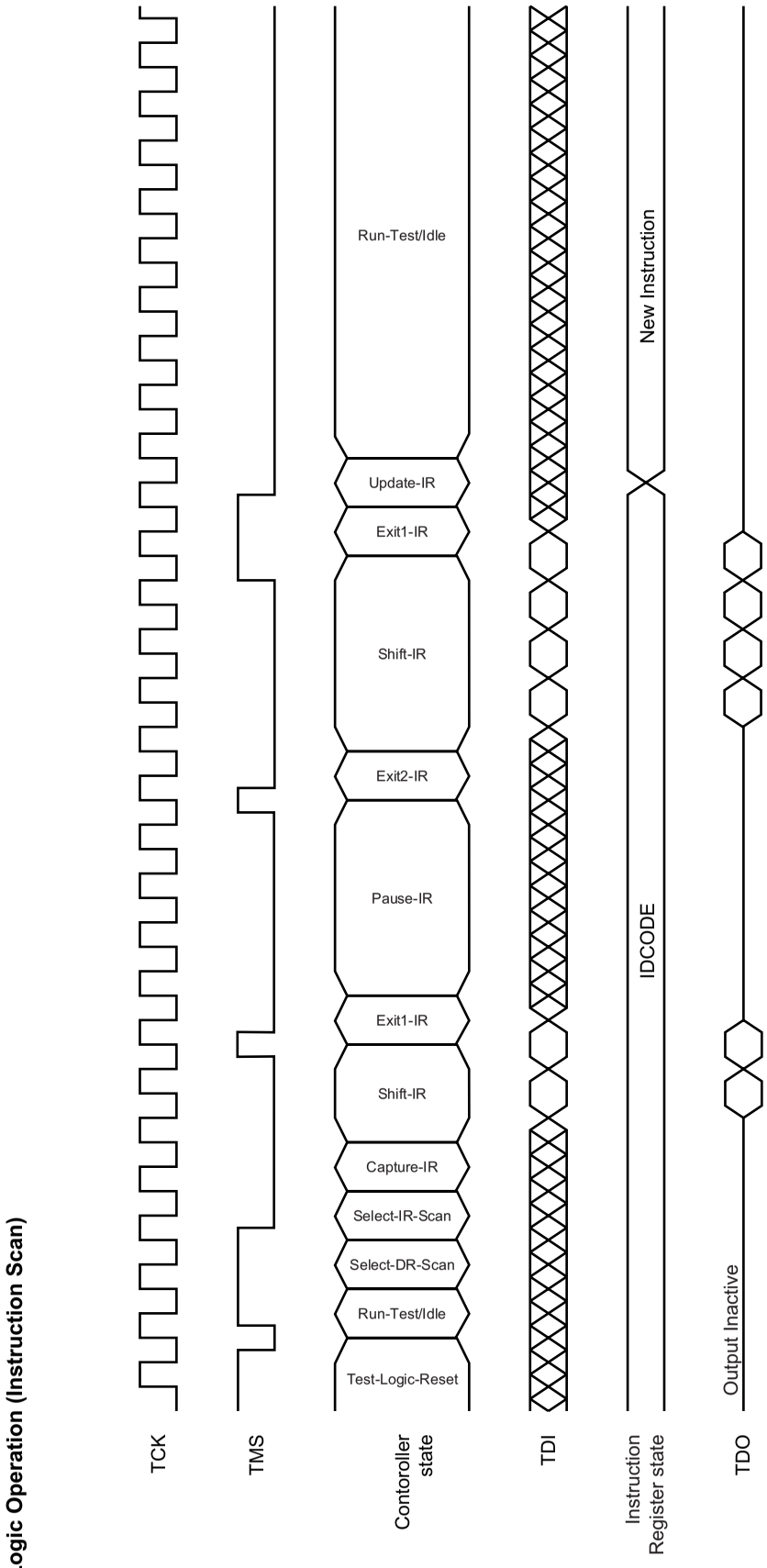
Disabling The Test Access Port

It is possible to use this device without utilizing the TAP. To disable the TAP Controller without interfering with normal operation of the device, TCK must be tied to V_{SS} to preclude mid level inputs.

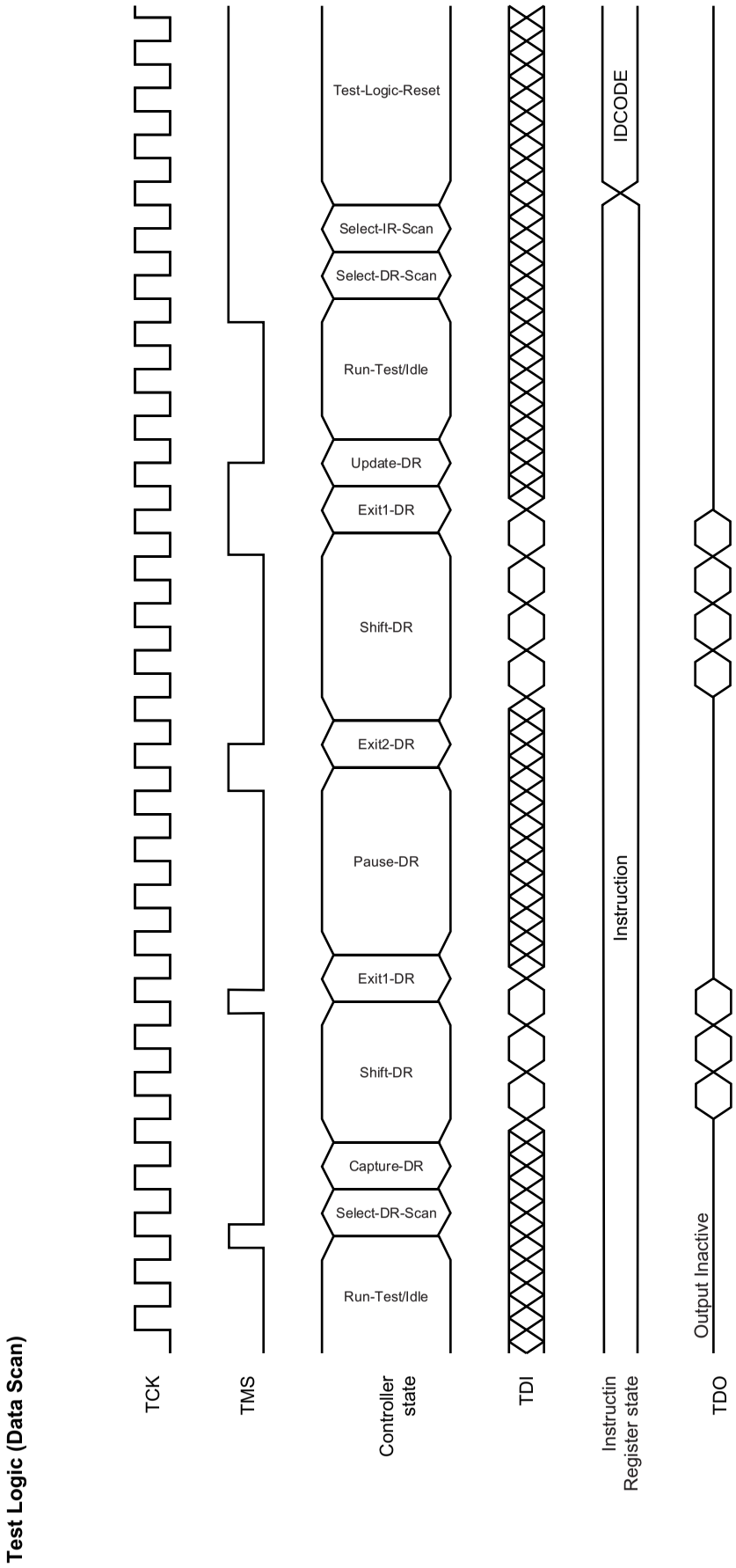
TDI and TMS are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to V_{DD} through a 1k Ω resistor.

TDO should be left unconnected.

Test Logic Operation (Instruction Scan)

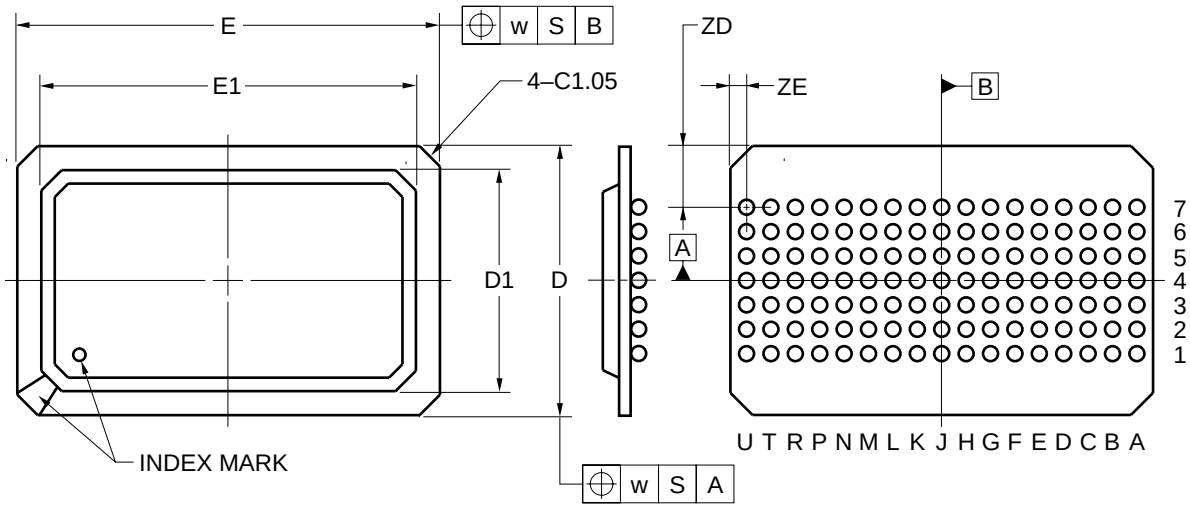


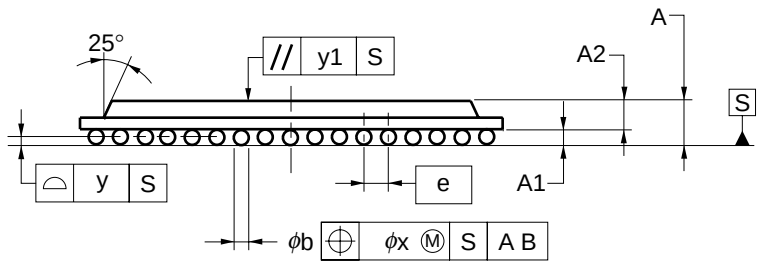
Test Logic (Data Scan)



★ **Package Drawing**

119-PIN PLASTIC BGA (14x22)





(UNIT:mm)

ITEM	DIMENSIONS
D	14.00±0.20
E	22.00±0.20
D1	12.00
E1	19.50
w	0.30
e	1.27
A	2.06±0.30
A1	0.60±0.10
A2	1.46
b	0.75±0.15
x	0.15
y	0.15
y1	0.35
ZD	3.19
ZE	0.84

P119F1-127-FJ1

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD44323182 and μPD44323362.

Types of Surface Mount Device

μPD44323182F1-FJ1: 119-pin plastic BGA

μPD44323362F1-FJ1: 119-pin plastic BGA

Revision History

Edition/ Date	Page		Type of revision	Location	Description (Previous edition → This edition)
	This edition	Previous edition			
3rd edition/ Nov. 2003	p.1	p.1	Addition	Ordering Number	"Note Under development" has been added to μPD44323182.
	p.9	p.9	Addition	Capacitance	C_{clk} has been added.
	p.10	p.10	Addition	DC Characteristics	I_{CC2} and I_{SBSS} have been determined. I_{CC2}: 250 mA I_{SBSS}: 300 mA
	p.19	p.19	Addition	ID Register Definition	ID [27:12] part no. has been determined. x18: 0000 0000 0011 1011 x36: 0000 0000 0011 1100
	p.25	p.25	Modification	Package Drawing	Preliminary version → Standardize version

[MEMO]

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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