

# AN5733

## TV Volume Control Circuit

### ■ Description

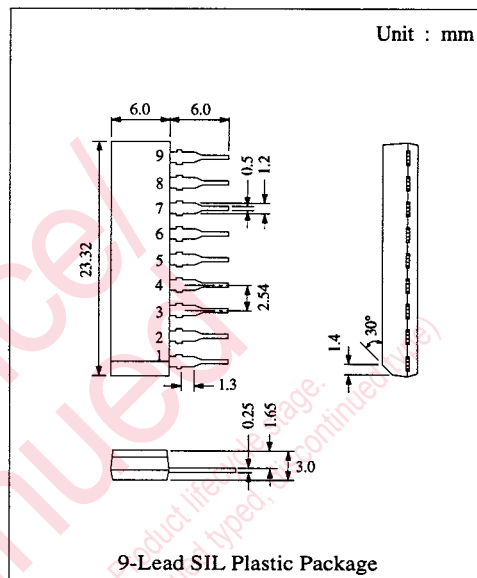
The AN5733 is an integrated circuit designed for TV volume control circuit.

### ■ Features

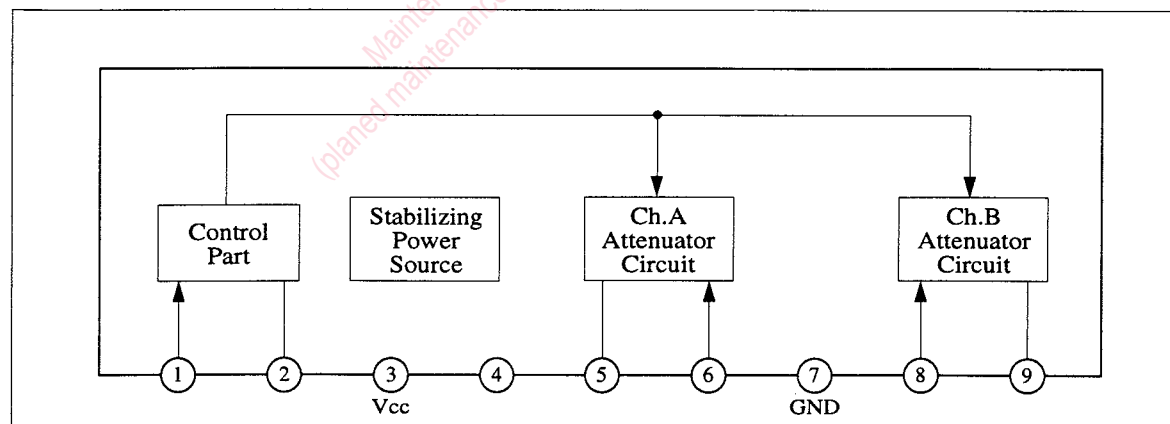
- Dual attenuator
- 9-lead SIL plastic package

### ■ Pin Descriptions

Pin No.	Pin Name
1	Control Voltage Input
2	Control Reference Voltage Output
3	Power Source (Vcc)
4	Decoupling
5	Ch.A Output Signal
6	Ch.A Input Signal
7	GND
8	Ch.B Input Signal
9	Ch.B Output Signal



### ■ Block Diagram



### ■ Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V <sub>CC</sub>	14.4	V
Supply Current	I <sub>3</sub>	13.7	mA
Power Dissipation (Ta = 70°C)	P <sub>D</sub>	197	mW
Operating Ambient Temperature	T <sub>opr</sub>	-40 ~ +150	°C
Storage Temperature	T <sub>stg</sub>	-20 ~ +70	°C

### ■ Electrical Characteristics (Ta=25°C)

Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Supply Voltage	I <sub>3</sub>		Table 1 (V <sub>CC</sub> =12V)	9.5	11.3	13.5	mA
Terminal Voltage	V <sub>2-7</sub>		Table 1 (V <sub>CC</sub> =12V)	3.8	4.1	4.45	V
Terminal Voltage	V <sub>4-7</sub>		Table 1 (V <sub>CC</sub> =12V)	2.9	3.2	3.5	V
Terminal Voltage	V <sub>6-7, 8-7</sub>		Table 1 (V <sub>CC</sub> =12V)	2.0	2.4	2.8	V
Terminal Voltage	V <sub>5-7, 9-7</sub>		Table 1 (V <sub>CC</sub> =12V)	2.9	3.4	3.9	V
Circuit Gain (1) (VR=10kΩ)	G <sub>v⑤-1</sub>	1	f=1kHz, V <sub>L</sub> =500mVrms	4	6	7.6	dB
Circuit Gain (1) Ch. Relative Gain	ΔG <sub>-1</sub>	1	f=1kHz, V <sub>L</sub> =500mVrms	-1.5		1.5	dB
Circuit Gain (1) O/P Dist. Factor	THD	1	f=1kHz, V <sub>L</sub> =500mVrms		0.2		%
Circuit Gain (2) (VR=5kΩ)	G <sub>v⑤-2</sub>	1	f=1kHz, V <sub>L</sub> =500mVrms	-2	0	2.2	dB
Circuit Gain (2) Ch. Relative Gain	ΔG <sub>-2</sub>	1	f=1kHz, V <sub>L</sub> =500mVrms	-2		2	dB
Circuit Gain (2) O/P Dist. Factor	THD	1	f=1kHz, V <sub>L</sub> =500mVrms		0.2		%
Circuit Gain (3) (VR=1kΩ)	G <sub>v⑤-3</sub>	1	f=1kHz, V <sub>L</sub> =500mVrms	-20	-16	-12	dB
Circuit Gain (3) Ch. Relative Gain	ΔG <sub>-3</sub>	1	f=1kHz, V <sub>L</sub> =500mVrms	-2.5		2.5	dB
Maximum Attenuation (VR=0)	Att	1	f=1kHz, V <sub>L</sub> =500mVrms	75			dB
Channel Separation	Sep	2	f=1kHz, V <sub>L</sub> =500mVrms	70			dB
Input Impedance	R <sub>in</sub>	3	f=1kHz		25		kΩ
Output Impedance	R <sub>out</sub>	4	f=1kHz		1.7		kΩ
Hum Rejection	Hr		Table 1	34			dB
Noise Output Voltage	NO	1				180	μVrms
DC Output Voltage Fluctuation	ΔV <sub>5-7, 9-7</sub>		Table 1 (V <sub>CC</sub> =12V)	-0.2		0.3	V

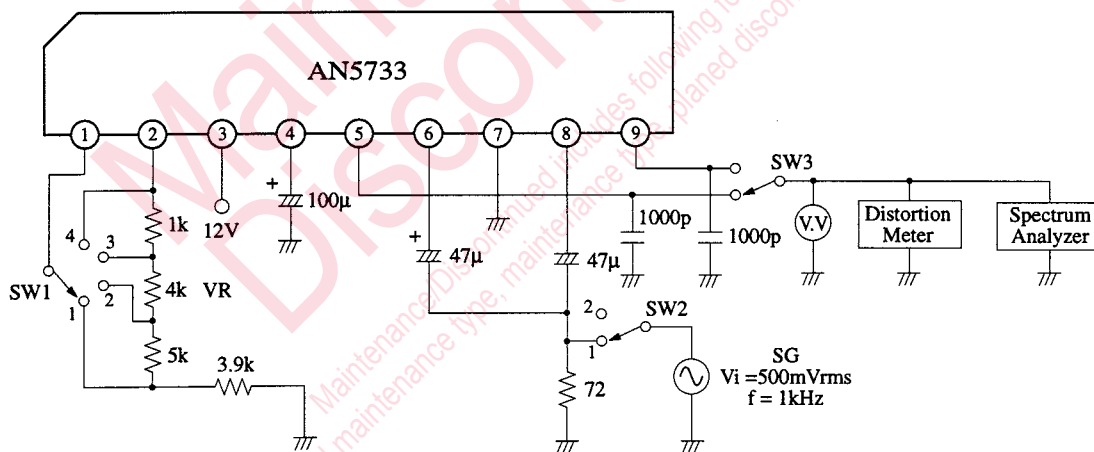
Table 1

Item	Symbol	Measuring Pin No.	Pin No.							Note				
			1	2	3	4	5	6	7		8	9		
Supply Voltage	$I_3$	3	8.9k $\Omega$ 0V	5k $\Omega$ CON①	12V					0V				
Terminal Voltage	$V_{2-7}$	2	8.9k $\Omega$ 0V	5k $\Omega$ CON①	12V					0V				
Terminal Voltage	$V_{4-7}$	4	8.9k $\Omega$ 0V	5k $\Omega$ CON①	12V					0V				
Terminal Voltage	$V_{6-7}$	6	8.9k $\Omega$ 0V	5k $\Omega$ CON①	12V					0V				
Terminal Voltage	$V_{8-7}$	8	8.9k $\Omega$ 0V	5k $\Omega$ CON①	12V					0V				
Terminal Voltage	$V_{5-7}$	5	8.9k $\Omega$ 0V	5k $\Omega$ CON①	12V					0V				
Terminal Voltage	$V_{9-7}$	9	8.9k $\Omega$ 0V	5k $\Omega$ CON①	12V					0V				
Hum Rejection	$Hr_5$	5	8.9k $\Omega$ 0V	5k $\Omega$ CON①	14V					0V				1
Hum Rejection	$\Delta Hr_5$	5	8.9k $\Omega$ 0V	5k $\Omega$ CON①	10V					0V				1
Hum Rejection	$Hr_9$	9	8.9k $\Omega$ 0V	5k $\Omega$ CON①	14V					0V				2
Hum Rejection	$\Delta Hr_9$	9	8.9k $\Omega$ 0V	5k $\Omega$ CON①	10V					0V				2
DC Output Voltage	$V_{5-7, 9-7}$	5, 9	3.9k $\Omega$ 0V	10k $\Omega$ CON①	12V					0V				3,4
DC Output Voltage Fluctuation	$\Delta V_{5-7, 9-7}$	5, 9	CON②	13.9k $\Omega$ 0V	12V					0V				3,4

Obtain  $Hr$  of Pin No.5 by taking ratio of difference between changes of DC voltage of pin No. 5, i.e.  $Hr_5$  and  $\Delta Hr_5$  against change in supply voltage (4V). Similarly, obtain  $Hr$  of Pin No.9.

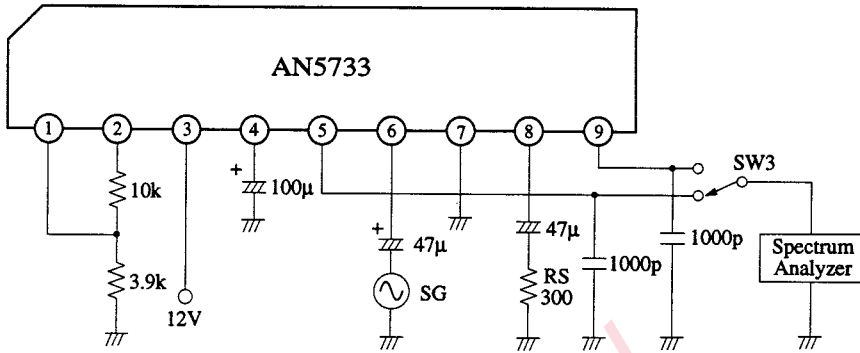
Note) 1. (18-2) - (18-1) :  $H_5$     3. (20 upper) - (5 upper) :  $V_{5-7}$   
 2. (18-4) - (18-3) :  $H_9$     4. (20 below) - (5 below) :  $V_{9-7}$

## Test Circuit 1



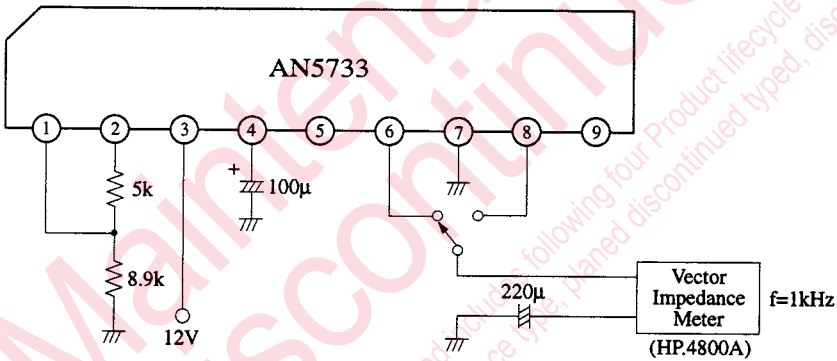
Item	Symbol	SW1	SW2
Circuit Gain (1) Ch. Relative Gain	$\Delta G_{-1}$	1	1
Circuit Gain (1) O/P Dist. Factor	THD	1	1
Circuit Gain (2) (VR=5k $\Omega$ )	$G_{V②-2}$	1	1
Circuit Gain (2) Ch. Relative Gain	$\Delta G_{-2}$	2	1
Circuit Gain (2) O/P Dist. Factor	THD	2	1
Circuit Gain (3) (VR=1k $\Omega$ )	$G_{V③-3}$	2	1
Circuit Gain (3) Ch. Relative Gain	$\Delta G_{-3}$	3	1
Maximum Attenuation (VR=0)	Att	3	1
Channel Separation	Sep	4	1
Input Impedance	$R_{in}$	2	2

Test Circuit 2

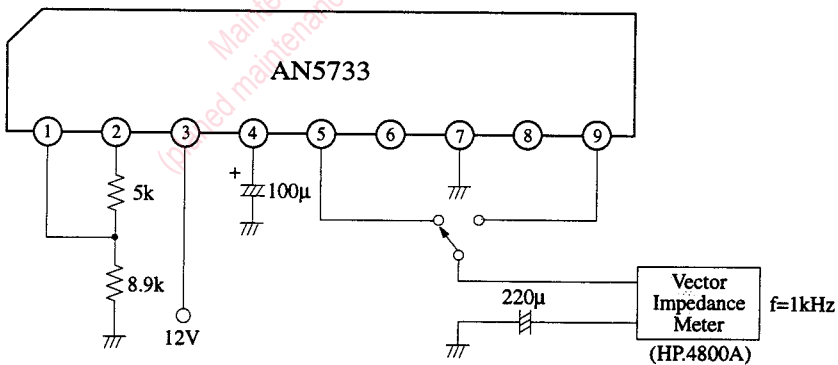


Note) Read level difference between Pin No.5 and Pin No.9 on the Spectrum Analyzer.  
 Read level difference of Pin No.5 and Pin No.9, similarly after changing SG and RS.

Test Circuit 3



Test Circuit 4



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