National Semiconductor

F100128
ECL/TTL Bi-Directional Translator

General Description

The F100128 is an octal latched bi-directional translator designed to convert TTL logic levels to 100K ECL logic levels and vice versa. The direction of this translation is determined by the DIR input. A LOW on the output enable input (OE) holds the ECL outputs in a cut-off state and the TTL outputs at a high impedance level. A HIGH on the latch enable input (LE) latches the data at both inputs even though only one output is enabled at the time. A LOW on LE makes the F100128 transparent.

The cut-off state is designed to be more negative than a normal ECL LOW level. This allows the output emitter-followers to turn off when the termination supply is −2.0V, presenting a high impedance to the data bus. This high impedance reduces termination power and prevents loss of low state noise margin when several loads share the bus.

The F100128 is designed with FAST® TTL output buffers, featuring optimal DC drive and capable of quickly charging and discharging highly capacitive loads. All inputs have 50 kΩ pull-down resistors.

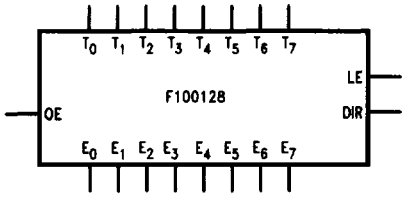
Features

- Bi-directional translation
- ECL high impedance outputs
- Latched outputs
- FAST® TTL outputs
- TRI-STATE® outputs

Refer to the F100328 datasheet for:
PCC Packaging
Lower Power
Military Versions
Extended voltage specs (−4.2V to −5.7V)

Ordering Code: See Section 8

Logic Symbol



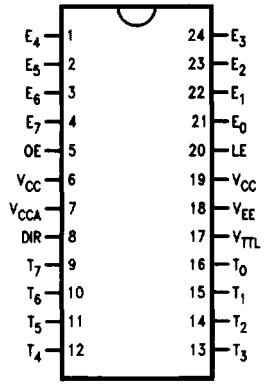
TL/F/9851-3

Pin Names	Description
E_0–E_7	ECL Data I/O
T_0–T_7	TTL Data I/O
OE	Output Enable Input
LE	Latch Enable Input
DIR	Direction Control Input

All pins function at 100K ECL levels except for T_0–T_7.

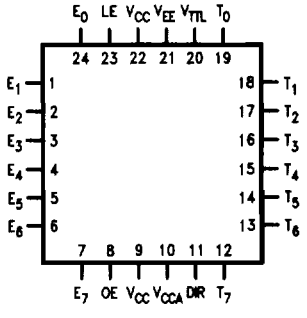
Connection Diagrams

24-Pin DIP



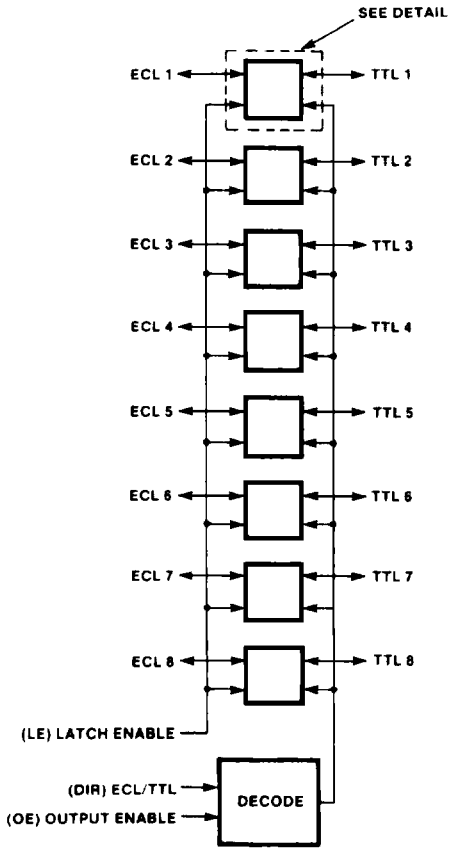
TL/F/9851-1

24-Pin Quad Cerpak



TL/F/9851-2

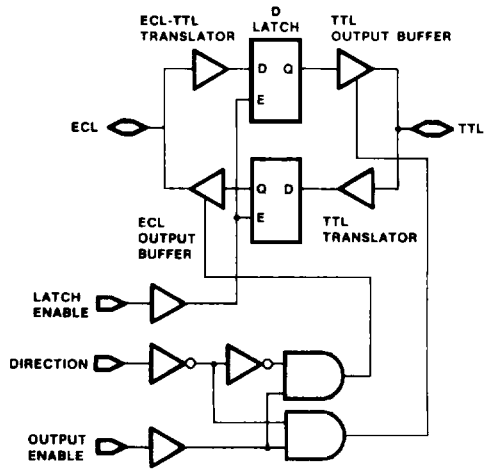
Functional Diagram



TL/F/9851–4

Note: LE, DIR and OE use ECL logic levels

Detail



TL/F/9851–5

Truth Table

OE	DIR	LE	ECL Port	TTL Port	Notes
L	X	L	LOW (Cut-Off)	Z	
L	L	H	Input	Z	1, 3
L	H	H	LOW (Cut-Off)	Input	2, 3
H	L	L	L	L	1, 4
H	L	L	H	H	1, 4
H	L	H	X	Latched	1, 3
H	H	L	L	L	2, 4
H	H	L	H	H	2, 4
H	H	H	Latched	X	2, 3

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance

Note 1: ECL input to TTL output mode.

Note 2: TTL input to ECL output mode.

Note 3: Retains data present before LE set HIGH.

Note 4: Latch is transparent.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature	+150°C
Case Temperature under Bias	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
V_{TTL} Pin Potential to Ground Pin	+6.0V to −0.5V
ECL Input Voltage (DC)	V_{EE} to +0.5V
ECL Output Current (DC Output HIGH)	−50 mA
TTL Input Voltage (Note 2)	−0.5V to +7.0V
TTL Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State TRI-STATE Output	−0.5V to +5.5V
Current Applied to TTL Output in LOW State (Max)	Twice the Rated I_{OL} (mA)

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Case Temperature	0°C to +85°C
Supply Voltage (Note 1)	
V_{EE}	−5.7V to −4.2V
V_{TTL}	+4.5V to +5.5V

Note 1: Parametric values specified at V_{EE} = −4.2V to −4.8V.

TTL-to-ECL DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OH}	Output High Voltage	−1020		−870	mV	V_{EE} = −4.2V, 50Ω to −2V
		−1025	−955	−880	mV	V_{EE} = −4.5V, 50Ω to −2V
		−1035		−880	mV	V_{EE} = −4.8V, 50Ω to −2V
V_{OL}	Output Low Voltage	−1810		−1605	mV	V_{EE} = −4.2V, 50Ω to −2V
		−1810	−1705	−1620	mV	V_{EE} = −4.5V, 50Ω to −2V
		−1830		−1620	mV	V_{EE} = −4.8V, 50Ω to −2V
	Cutoff Voltage					OE or DIR Low,
			−2000	−1930	mV	V_{EE} = −4.2V, 50Ω to −2V
			−2000	−1950	mV	V_{EE} = −4.5V, 50Ω to −2V
			−2000	−1950	mV	V_{EE} = −4.8V, 50Ω to −2V
V_{OHC}	Output High Voltage Corner Point High	−1030			mV	V_{EE} = −4.2V, 50Ω to −2V
		−1035			mV	V_{EE} = −4.5V, 50Ω to −2V
		−1045			mV	V_{EE} = −4.8V, 50Ω to −2V
V_{OLC}	Output Low Voltage Corner Point Low			−1595	mV	V_{EE} = −4.2V, 50Ω to −2V
				−1610	mV	V_{EE} = −4.5V, 50Ω to −2V
				−1610	mV	V_{EE} = −4.8V, 50Ω to −2V
V_{IH}	Input High Voltage	2.0			V	Over V_{TTL}, V_{EE}, T_C Range
V_{IL}	Input Low Voltage			0.8	V	Over V_{TTL}, V_{EE}, T_C Range
I_{IH}	Input High Current			70	μA	V_{IN} = +2.7V
	Breakdown Test			1.0	mA	V_{IN} = +5.5V
I_{IL}	Input Low Current			−1.0	mA	V_{IN} = +0.5V
V_{FCD}	Input Clamp Diode Voltage			−1.2	V	I_{IN} = −18 mA
I_{EE}	V_{EE} Supply Current	−250	−175	−125	mA	LE Low, OE and DIR High

ECL-to-TTL DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C, C_L = 50 pF, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OH}	Output High Voltage	2.7 2.4	3.1 2.9		V V	I_{OH} = −3 mA, V_{TTL} = 4.75V I_{OH} = −3 mA, V_{TTL} = 4.50V
V_{OL}	Output Low Voltage		0.3	0.5	V	I_{OL} = 24 mA, V_{TTL} = 4.50V
V_{IH}	Input High Voltage	−1150 −1165 −1165		−870 −880 −880	mV mV mV	V_{EE} = −4.2V V_{EE} = −4.5V V_{EE} = −4.8V
V_{IL}	Input Low Voltage	−1810 −1810 −1810		−1475 −1475 −1490	mV mV mV	V_{EE} = −4.2V V_{EE} = −4.5V V_{EE} = −4.8V
I_{IH}	Input High Current			200	μA	V_{IN} = V_{IH} (Max)
I_{IL}	Input Low Current	0.50			μA	V_{IN} = V_{IL} (Min)
I_{OZHT}	TRI-STATE Current Output High			70	μA	V_{OUT} = +2.7V
I_{OZLT}	TRI-STATE Current Output Low			−1.0	mA	V_{OUT} = +0.5V
I_{OS}	Output Short-Circuit Current	−60		−225	mA	V_{OUT} = 0.0V, V_{TTL} = +5.5V
I_{TTL}	V_{TTL} Supply Current		155 90 120	200 120 160	mA mA mA	TTL Outputs Low TTL Outputs High TTL Outputs in TRI-STATE

Cerpak TTL-to-ECL AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	T_C = 0°C		T_C = 25°C		T_C = 85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	T_n to E_n (Transparent)	1.0 1.1	3.3 3.7	1.0 1.1	3.3 3.7	1.0 1.4	3.3 4.3	ns ns	*Figures 1 & 2*
t_{PLH} t_{PHL}	LE to E_n	2.2 2.0	4.6 4.3	2.2 2.0	4.6 4.3	2.7 2.4	5.4 5.0	ns ns	*Figures 1 & 2*
t_{PZH}	OE to E_n (Cutoff to High)	1.4	4.5	1.4	4.5	1.5	5.0	ns	*Figures 1 & 2*
t_{PHZ}	DIR to E_n (High to Cutoff)	1.0	4.0	1.0	4.0	1.0	4.0	ns	*Figures 1 & 2*
t_{PHZ}	OE to E_n (High to Cutoff)	1.0	3.5	1.0	3.5	1.0	4.0	ns	*Figures 1 & 2*
t_{set}	T_n to LE	1.0		1.0		1.0		ns	*Figures 1 & 2*
t_{hold}	T_n to LE	2.0		2.0		2.0		ns	*Figures 1 & 2*
tpw(H)	Pulse Width High, LE	2.0		2.0		2.0		ns	*Figures 1 & 2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.6	1.6	0.6	1.6	0.6	1.6	ns	*Figures 1 & 2*

Cerpak ECL-to-TTL AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{TTL} = +4.5V to +5.5V, C_L = 50 pF

Symbol	Parameter	T_C = 0°C		T_C = 25°C		T_C = 85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	E_n to T_n (Transparent)	2.5 2.0	6.5 5.5	2.5 2.0	6.5 5.5	3.0 2.0	8.0 6.0	ns	*Figures 3 & 4*
t_{PLH} t_{PHL}	LE to T_n	3.0 2.5	7.5 6.5	3.0 2.5	7.5 6.5	3.5 3.0	9.5 7.0	ns	*Figures 3 & 4*
t_{PZH} t_{PZL}	OE to T_n (Enable Time)	3.0 4.0	7.5 9.5	3.0 4.0	7.5 9.5	3.5 4.5	8.5 10.0	ns	*Figures 3 & 5*
t_{PHZ} t_{PLZ}	OE to T_n (Disable Time)	3.0 2.5	9.5 8.0	3.0 2.5	9.5 8.0	3.5 3.5	11.0 10.0	ns	*Figures 3 & 5*
t_{PHZ} t_{PLZ}	DIR to T_n (Disable Time)	2.5 2.5	10.0 8.5	2.5 2.5	10.0 8.5	3.0 3.5	10.0 10.0	ns	*Figures 3 & 6*
t_{set}	E_n to LE	1.5		1.5		1.5		ns	*Figures 3 & 4*
t_{hold}	E_n to LE	3.5		3.5		3.5		ns	*Figures 3 & 4*
tpw(H)	Pulse Width High, LE	2.0		2.0		2.0		ns	*Figures 3 & 4*

Ceramic Dual-In-Line Package TTL-to-ECL AC Electrical Characteristics

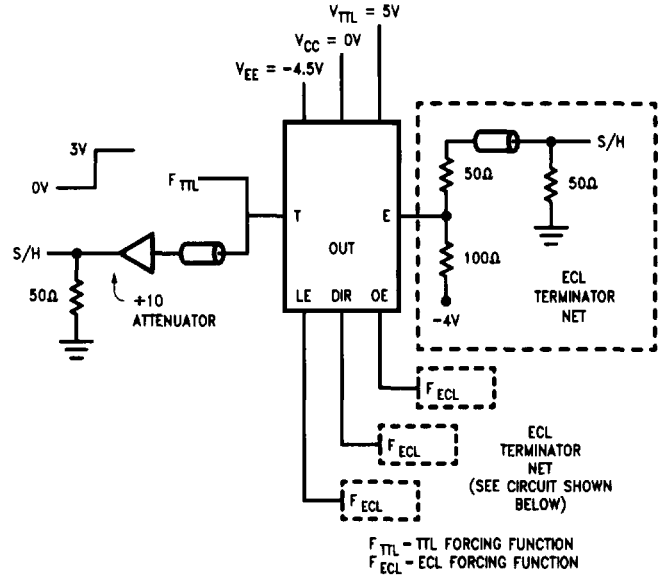
V_{EE} = −4.2V to −4.8V, V_{TTL} = +4.5V to +5.5V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = 25°C		T_C = 85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	T_N to E_n (Transparent)	1.0 1.1	3.3 3.7	1.0 1.1	3.3 3.7	1.0 1.4	3.3 4.3	ns ns	*Figures 1 & 2*
t_{PLH} t_{PHL}	LE to E_n	2.2 2.0	4.6 4.3	2.2 2.0	4.6 4.3	2.7 2.4	5.4 5.0	ns ns	*Figures 1 & 2*
t_{PZH}	OE to E_n (Cutoff to High)	1.4	4.5	1.4	4.5	1.5	5.0	ns	*Figures 1 & 2*
t_{PHZ}	DIR to E_n (High to Cutoff)	1.0	4.0	1.0	4.0	1.0	4.0	ns	*Figures 1 & 2*
t_{PHZ}	OE to E_n (High to Cutoff)	1.0	3.5	1.0	3.5	1.0	4.0	ns	*Figures 1 & 2*
t_{set}	T_n to LE	1.0		1.0		1.0		ns	*Figures 1 & 2*
t_{hold}	T_n to LE	2.0		2.0		2.0		ns	*Figures 1 & 2*
tpw(H)	Pulse Width High, LE	2.0		2.0		2.0		ns	*Figures 1 & 2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.6		1.0		1.6		ns	*Figures 1 & 2*

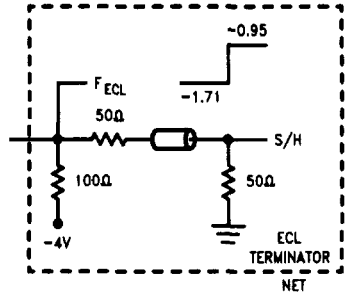
Ceramic Dual-In-Line Package ECL-to-TTL AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{TTL} = +4.5V to +5.5V, V_{CC} = V_{CCA} = GND, C_L = 50 pF

Symbol	Parameter	T_C = 0°C		T_C = 25°C		T_C = 85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	E_n to T_n (Transparent)	2.5 2.0	6.5 5.5	2.5 2.0	6.5 5.5	3.0 2.0	8.0 6.0	ns	*Figures 3 & 4*
t_{PLH} t_{PHL}	LE to T_n	3.0 2.5	7.5 6.5	3.0 2.5	7.5 6.5	3.5 3.0	9.5 7.0	ns	*Figures 3 & 4*
t_{PZH} t_{PZL}	OE to T_n (Enable Time)	3.0 4.0	7.5 9.5	3.0 4.0	7.5 9.5	3.5 4.5	8.5 10.0	ns	*Figures 3 & 5*
t_{PHZ} t_{PLZ}	OE to T_n (Disable Time)	3.0 2.5	9.5 8.0	3.0 2.5	9.5 8.0	3.5 3.5	11.0 10.0	ns	*Figures 3 & 5*
t_{PHZ} t_{PLZ}	DIR to T_n (Disable Time)	2.5 2.5	10.0 8.5	2.5 2.5	10.0 8.5	3.0 3.5	10.0 10.0	ns	*Figures 3 & 6*
t_{set}	E_n to LE	1.5		1.5		1.5		ns	*Figures 3 & 4*
t_{hold}	E_n to LE	3.5		3.5		3.5		ns	*Figures 3 & 4*
tpw(H)	Pulse Width High, LE	2.0		2.0		2.0		ns	*Figures 3 & 4*

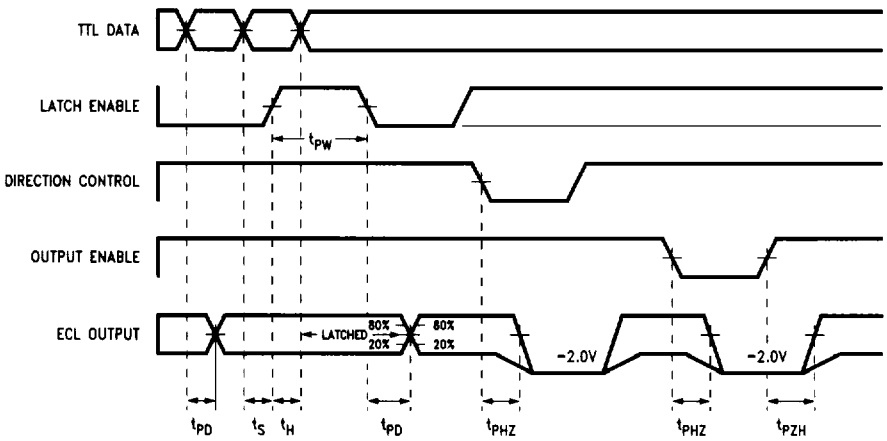


TL/F/9851–6



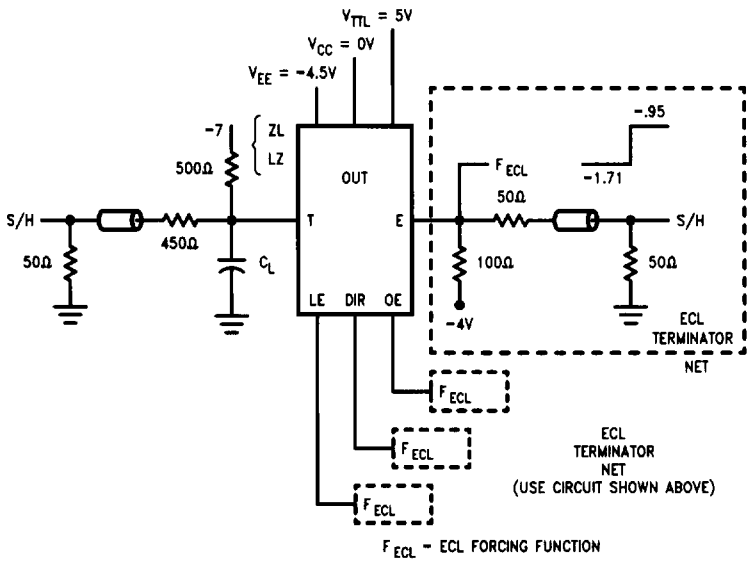
TL/F/9851–12

FIGURE 1. TTL to ECL AC Test Circuit



TL/F/9851–7

FIGURE 2. TTL to ECL Transition—Propagation Delay and Transition Times

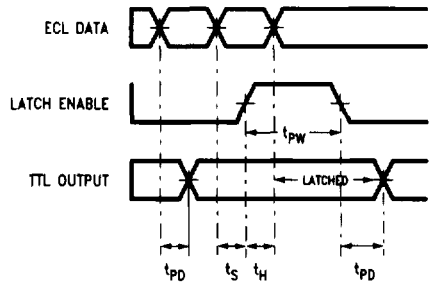


TL/F/9851–8

C_L = 50 pF including stray and jig capacitance.

Note: 50Ω to ground termination **must be included** on ECL I/O pins **not** monitored by a 50Ω scope to prevent oscillatory feedback.

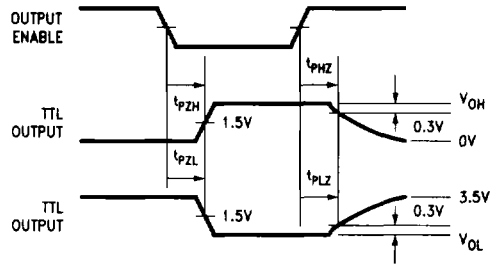
FIGURE 3. ECL-to-TTL AC Test Circuit



TL/F/9851–9

Note: DIR is LOW, OE is HIGH

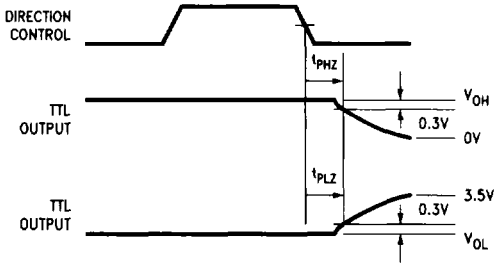
FIGURE 4. ECL-to-TTL Transition—Propagation Delay and Transition Times



TL/F/9851–13

Note: DIR is LOW, LE is HIGH

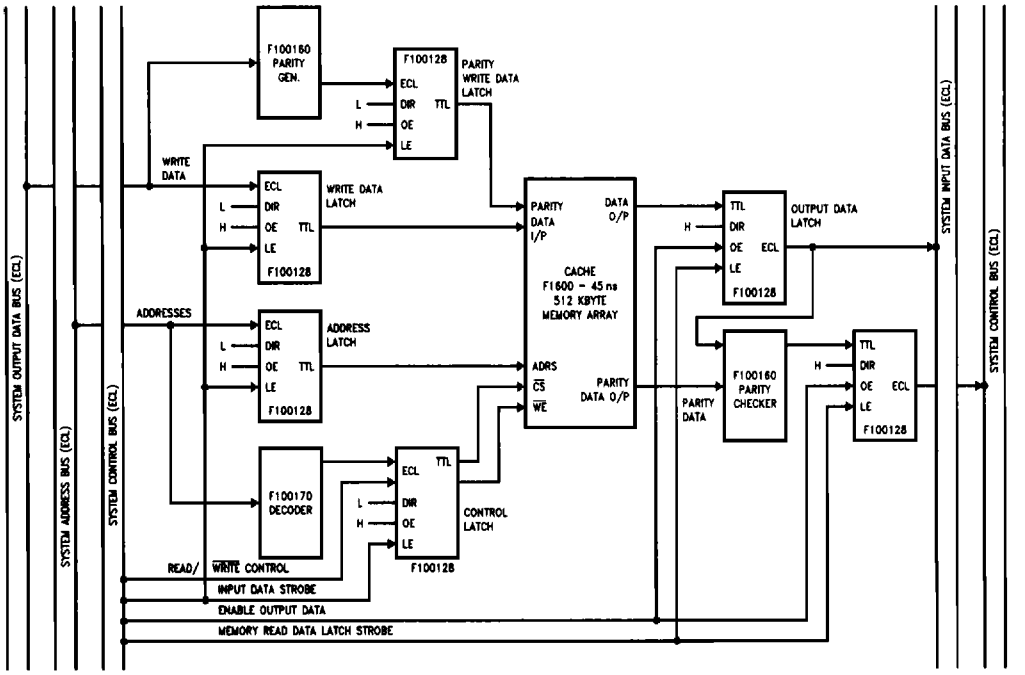
FIGURE 5. ECL-to-TTL Transition; OE to TTL Output, Enable and Disable Times



TL/F/9851–14

Note: OE and LE are HIGH

FIGURE 6. ECL-to-TTL Transition; DIR to TTL Output, Disable Time



TL/F/9851-10

FIGURE 5. Applications Diagram—MOS/TTL SRAM Interface Using F100128 ECL–TTL Latched Translator