Chapter 7
Electrical Characteristics

DC Characteristics

Table 7-1: Absolute Maximum Stress Ratings

Symbol	Parameter	Min	Max	Unit	Test Conditions
T_{STG}	Storage temperature	-55	150	°C	-
V_{DD}	Supply voltage	-0.5	7.0	V	-
V_{IN}	Input Voltage	V_{SS} - 0.5	V_{DD} + 0.5	V	-
I_{LP}*	Latch-up current	± 150	-	mA	-
ESD**	Electrostatic discharge	-	2K	V	MIL-STD 883C, Method 3015.7

Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those indicated in the Operating Conditions section of the manual is not implied.

* $-2V < V_{PIN} < 8V$

** *SCSI pins only*

Table 7-2: Operating Conditions

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{DD}	Supply voltage	4.75	5.25	V	-
I_{DD}	Supply current (dynamic)	-	130	mA	-
	Supply current (static)	-	1	mA	-
T_A	Operating free air	0	70	°C	-
O_{JA}	Thermal resistance (junction to ambient air)	-	67	°C/W	-

Conditions that exceed the operating limits may cause the device to function incorrectly

Table 7-3: SCSI Signals - SD(15-0)/, SDP(1-0)/, SREQ/ SACK/

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	2.0	V_{DD} + 0.5	V	-
V_{IL}	Input low voltage	V_{SS} - 0.5	0.8	V	-
V_{OH}*	Output high voltage	2.5	3.5	V	2.5 mA
V_{OL}	Output low voltage	V_{SS}	0.5	V	48 mA
I_{OZ}	Tristate leakage	-10	10	µA	-

**TolerANT active negation enabled*

Table 7-4: SCSI Signals - SMSG, SI_O/, SC_D/, SATN/, SBSY/, SSEL/, SRST/

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	2.0	V_{DD} + 0.5	V	-
V_{IL}	Input low voltage	V_{SS} - 0.5	0.8	V	-
V_{OL}	Output low voltage	V_{SS}	0.5	V	48 mA
I_{OZ}	Tristate leakage (SRST/ only)	-10 -500	10 -50	µA	-

Table 7-5: Input Signals - CLK, SCLK, GNT/, IDSEL, RST/, TESTIN, DIFFSENS, BIG_LIT/

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	2.0	V_{DD} + 0.5	V	-
V_{IL}	Input low voltage	V_{SS} - 0.5	0.8	V	-
I_{IN}	Input leakage	-10	10	µA	-

Note: CLK, SCLK, GNT/, BIG_LIT/, and IDSEL have 100 µA pull-ups that are enabled when TESTIN is low. TESTIN has a 100 µA pull-up that is always enabled.

Table 7-6: Capacitance

Symbol	Parameter	Min	Max	Unit	Test Conditions
C_I	Input capacitance of input pads	-	7	pF	-
C_{IO}	Input capacitance of I/O pads	-	10	pF	-

Table 7-7: Output Signal - MAC/_TESTOUT, REQ/

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{OH}	Output high voltage	2.4	V_{DD}	V	-16 mA
V_{OL}	Output low voltage	V_{SS}	0.4	V	16 mA
I_{OZ}	Tristate leakage	-10	10	µA	-

Note: REQ/ has a 100 µA pull-up that is enabled when TESTIN is low

Table 7-8: Output Signals - IRQ/, SDIR(15-0), SDIRP0, SDIRP1, BSYDIR, SELDIR, RSTDIR, TGS, IGS, MAS/(1-0), MCE/, MOE/, MWE/

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{OH}	Output high voltage	2.4	V_{DD}	V	-4 mA*
V_{OL}	Output low voltage	V_{SS}	0.4	V	4 mA*
I_{OZ}	Tristate leakage	-10	10	µA	-

Note: IRQ/, MAS/(1-0), MCE/, MOE/, and MWE/ have a 100 µA pull-up that is enabled when TESTIN is low. IRQ/ can be enabled with a register bit as an open drain output with an internal 100 µA pull-up.

**for IRQ/, Test Conditions are ± 8mA*

Table 7-9: Output Signal - SERR/

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{OL}	Output low voltage	V_{SS}	0.4	V	16 mA
I_{OZ}	Tristate leakage	-10	10	µA	-

Table 7-10: Bidirectional Signals - AD(31-0), C_BE/(3-0), FRAME/, IRDY/, TRDY/, DEVSEL/, STOP/, PERR/, PAR,

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	2.0	V_{DD} + 0.5	V	-
V_{IL}	Input low voltage	V_{SS} - 0.5	0.8	V	-
V_{OH}	Output high voltage	2.4	V_{DD}	V	16 mA
V_{OL}	Output low voltage	V_{SS}	0.4	V	16 mA
I_{OZ}	Tristate leakage	-10	10	µA	-

Note: All the signals in this table have 100 µA pull-ups that are enabled when TESTIN is low

Table 7-11: Bidirectional Signals - GPIO0_FETCH/, GPIO1_MASTER/, GPIO2_MAS2/, GPIO3, GPIO4

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	2.0	V_{DD} + 0.5	V	-
V_{IL}	Input low voltage	V_{SS} - 0.5	0.8	V	-
V_{OH}	Output high voltage	2.4	V_{DD}	V	-16 mA
V_{OL}	Output low voltage	V_{SS}	0.4	V	16 mA
I_{OZ}	Tristate leakage	-10	10	µA	-

Note: All the signals in this table have 100 µA pull-ups that are enabled when TESTIN is low

Table 7-12: Bidirectional Signals - MAD(7-0)

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	2.0	V_{DD} + 0.5	V	-
V_{IH}	Input high voltage - external memory pull-downs	3.85	V_{DD} + 0.5	V	-
V_{IL}	Input low voltage	V_{SS} - 0.5	0.8	V	-
V_{IL}	Input low voltage - external memory pull-downs	V_{SS} - 0.5	1.35	V	-
V_{OH}	Output high voltage	2.4	V_{DD}	V	-4 mA
V_{OL}	Output low voltage	V_{SS}	0.4	V	4 mA
I_{OZ}	Tristate leakage	-10	10	µA	-

Note: All the signals in this table have 100 µA pull-ups that are enabled when TESTIN is low

Table 7-13: Input Signals —TDI, TMS, TCK (53C825AJonly)

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	3.85	V_{DD} + 0.5	V	-
V_{IL}	Input low voltage	V_{SS} - 0.5	1.35	V	-
I_{IN}	Input leakage	-800	-200	µA	-

Table 7-14: Output Signal —TDO (53C825AJ only)

Symbol	Parameters	Min	Max	Units	Test Conditions
V_{OH}	Output high voltage	V_{DD} - 0.5	V_{DD}	V	-4 mA
V_{OL}	Output low voltage	V_{SS}	0.5	V	4 mA
I_{OZ}	Tristate leakage	-10	10	µA	-

53C825A TolerANT Technology Electrical Characteristics

Table 7-15: TolerANT Technology Electrical Characteristics

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{OH}[1]	Output high voltage	2.5	3.5	V	I_{OH} = 2.5 mA
V_{OL}	Output low voltage	0.1	0.5	V	I_{OL} = 48 mA
V_{IH}	Input high voltage	2.0	7.0	V	-
V_{IL}	Input low voltage	-0.5	0.8	V	Referenced to V_{SS}
V_{IK}	Input clamp voltage	-0.66	-0.77	V	V_{DD} = 4.75; I_I = -20 mA
V_{THI}	Threshold, high to low	1.1	1.3	V	-
V_{TLI}	Threshold, low to high	1.5	1.7	V	-
V_{THI}-V_{TLI}	Hysteresis	200	400	mV	-
I_{OH}[1]	Output high current	2.5	24	mA	V_{OH} = 2.5 V
I_{OL}	Output low current	100	200	mA	V_{OL} = 0.5 V
I_{OSH}[1]	Short-circuit output high current	-	625	mA	Output driving low, pin shorted to V_{DD} supply[2]
I_{OSL}	Short-circuit output low current	-	95	mA	Output driving high, pin shorted to V_{SS} supply
I_{IH}	Input high leakage	-	10	µA	-0.5 < V_{DD} < 5.25 V_{PIN} = 2.7 V
I_{IL}	Input low leakage	-	-10	µA	-0.5 < V_{DD} < 5.25 V_{PIN} = 0.5 V
R_I	Input resistance	20	-	MΩ	SCSI pins[3]
C_P	Capacitance per pin	-	10	pF	PQFP
t_R[1]	Rise time, 10% to 90%	9.7	18.5	ns	Figure 7-1
t_F	Fall time, 90% to 10%	5.2	14.7	ns	Figure 7-1

Note: These values are guaranteed by periodic characterization; they are not 100% tested on every device.

[1] *Active negation outputs only: Data, Parity, SREQ/, SACK/*

[2] *Single pin only; irreversible damage may occur if sustained for one second*

[3] *SCSI RESET pin has 10 kΩ pull-up resistor*

Table 7-15: TolerANT Technology Electrical Characteristics (Continued)

Symbol	Parameter	Min	Max	Units	Test Conditions
dV_{H}/dt	Slew rate, low to high	0.15	0.49	V/ns	Figure 7-1
dV_{L}/dt	Slew rate, high to low	0.19	0.67	V/ns	Figure 7-1
ESD	Electrostatic discharge	2	-	KV	MIL-STD-883C; 3015-7
	Latch-up	100	-	mA	-
	Filter delay	20	30	ns	Figure 7-2
	Extended filter delay	40	60	ns	Figure 7-2

Note: These values are guaranteed by periodic characterization; they are not 100% tested on every device.
[1] Active negation outputs only: Data, Parity, SREQ/, SACK/
[2] Single pin only; irreversible damage may occur if sustained for one second
[3] SCSI RESET pin has 10 kΩ pull-up resistor

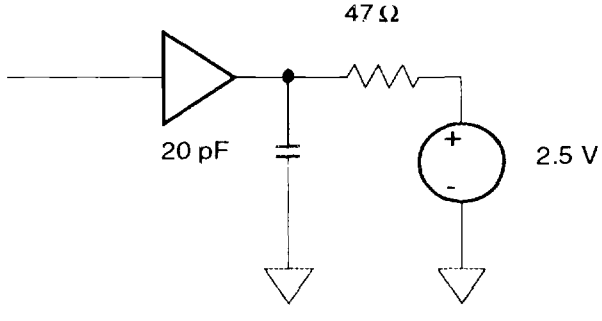


Figure 7-1: Rise and Fall Time Test Conditions

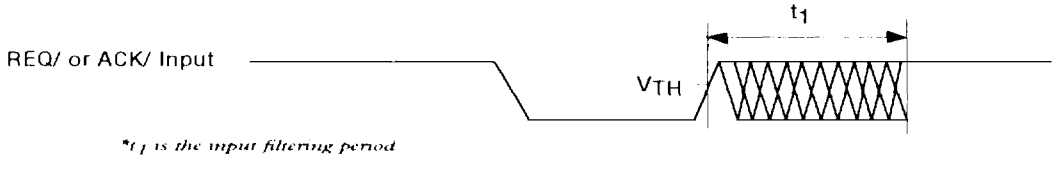


Figure 7-2: SCSI Input Filtering

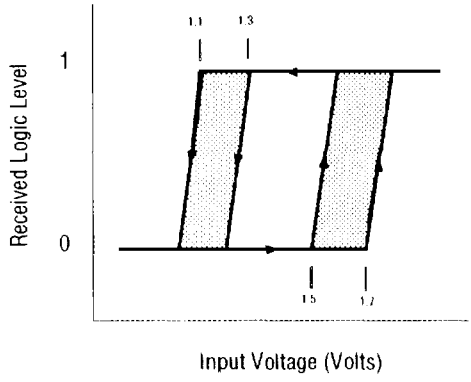


Figure 7-3: Hysteresis of SCSI Receiver

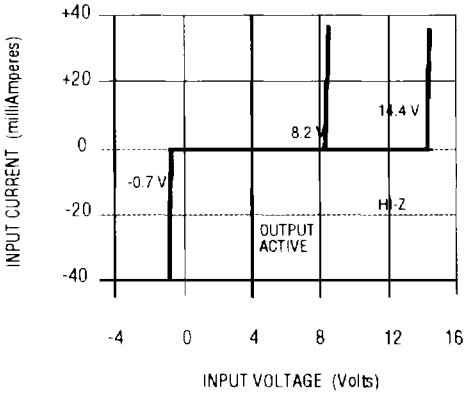


Figure 7-4: Input Current as a Function of Input Voltage

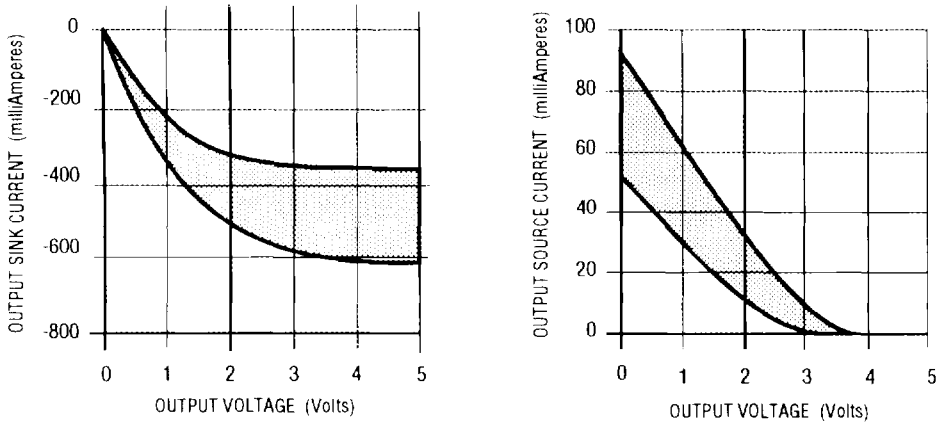


Figure 7-5: Output Current as a Function of Output Voltage

AC Characteristics

The AC characteristics described in this section apply over the entire range of operating conditions (refer to the DC Characteristics section). Chip timings are based on simulation at worst case voltage, temperature, and processing. Timings were developed with a load capacitance of 50 pF.

Figure 7-6: Clock Timing

Symbol	Parameter	Min	Max	Units
t_1	Bus clock cycle time	30	DC	ns
	SCSI clock cycle time (SCLK)*	15	60	ns
t_2	CLK low time**	12	-	ns
	SCLK low time**	6	33	ns
t_3	CLK high time**	12	-	ns
	SCLK high time**	6	33	ns
t_4	CLK slew rate	1	-	V/ns
	SCLK slew rate	1	-	V/ns

** This parameter must be met to insure SCSI timings are within specification*

***Duty cycle not to exceed 60/40*

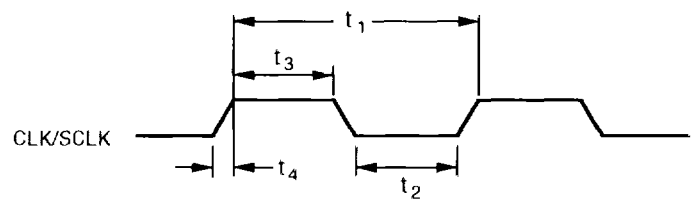
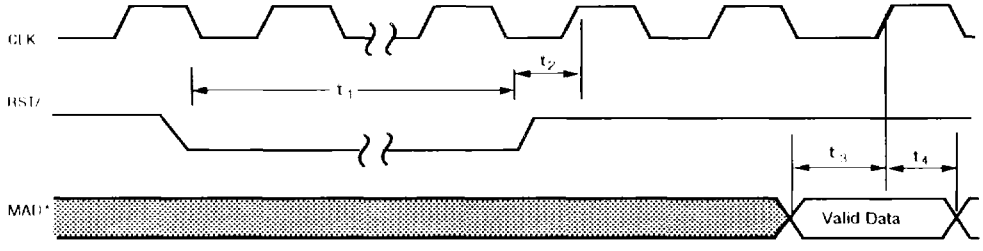


Figure 7-7: Reset Input

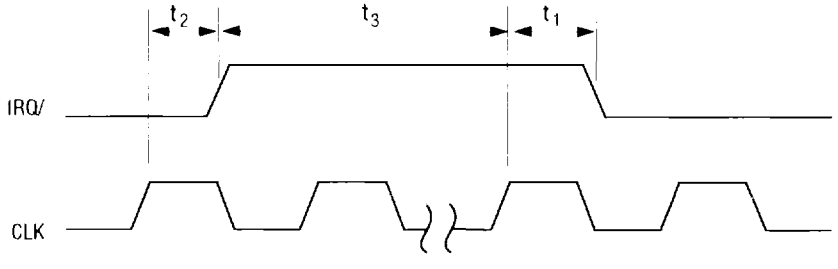
Symbol	Parameter	Min	Max	Units
t_1	Reset pulse width	10	-	t_{CLK}
t_2	Reset deasserted setup to CLK high	0	-	ns
t_3	MAD setup time to CLK high (for configuring the MAD bus only)	20	-	ns
t_4	MAD hold time from CLK high (for configuring the MAD bus only)	20	-	ns



*When enabled

Figure 7-8: Interrupt Output

Symbol	Parameter	Min	Max	Units
t_1	CLK high to IRQ/ low	20	-	ns
t_2	CLK high to IRQ/ high	40	-	ns
t_3	IRQ/ deassertion time	3	-	CLKs



PCI and External Memory Interface Timing Diagrams

Figure 7-9 through Figure 7-30 represent signal activity when the SYM53C825A accesses the PCI bus. The timings for the PCI and external memory buses are listed on page 7-32. This section includes timing diagrams for access to three groups of external memory configurations. The first group applies to systems with memory size of 128 KB and above; one byte read or write cycle, and fast or normal ROMs. The second group applies to systems with memory size of 128 KB and above, one-byte read or write cycles, and slow ROMs. The third group applies to systems with memory size of 64 KB or less, one-byte read or write cycles, and normal or fast ROM.

Note: multiple byte accesses to the external memory bus increase the read or write cycle by 11 clocks for each additional byte.

Timing diagrams included in this section

- PCI configuration register read
- PCI configuration register write
- Target read, without external memory
- Target write, without external memory
- Target read, with external memory
- Target write, with external memory
- Op code fetch, non-burst
- Burst op code fetch
- Back-to-back read
- Back-to-back write
- Burst read
- Burst write
- Read cycle, normal/fast ROM, single-byte access
- Write cycle, normal/fast ROM, single-byte access
- Read cycle, normal/fast ROM, multiple-byte access
- Write cycle, normal/fast ROM, multiple-byte access
- Read cycle, slow memory
- Write cycle, slow memory
- Read cycle, 16 KB ROM
- Write cycle, 16 KB ROM

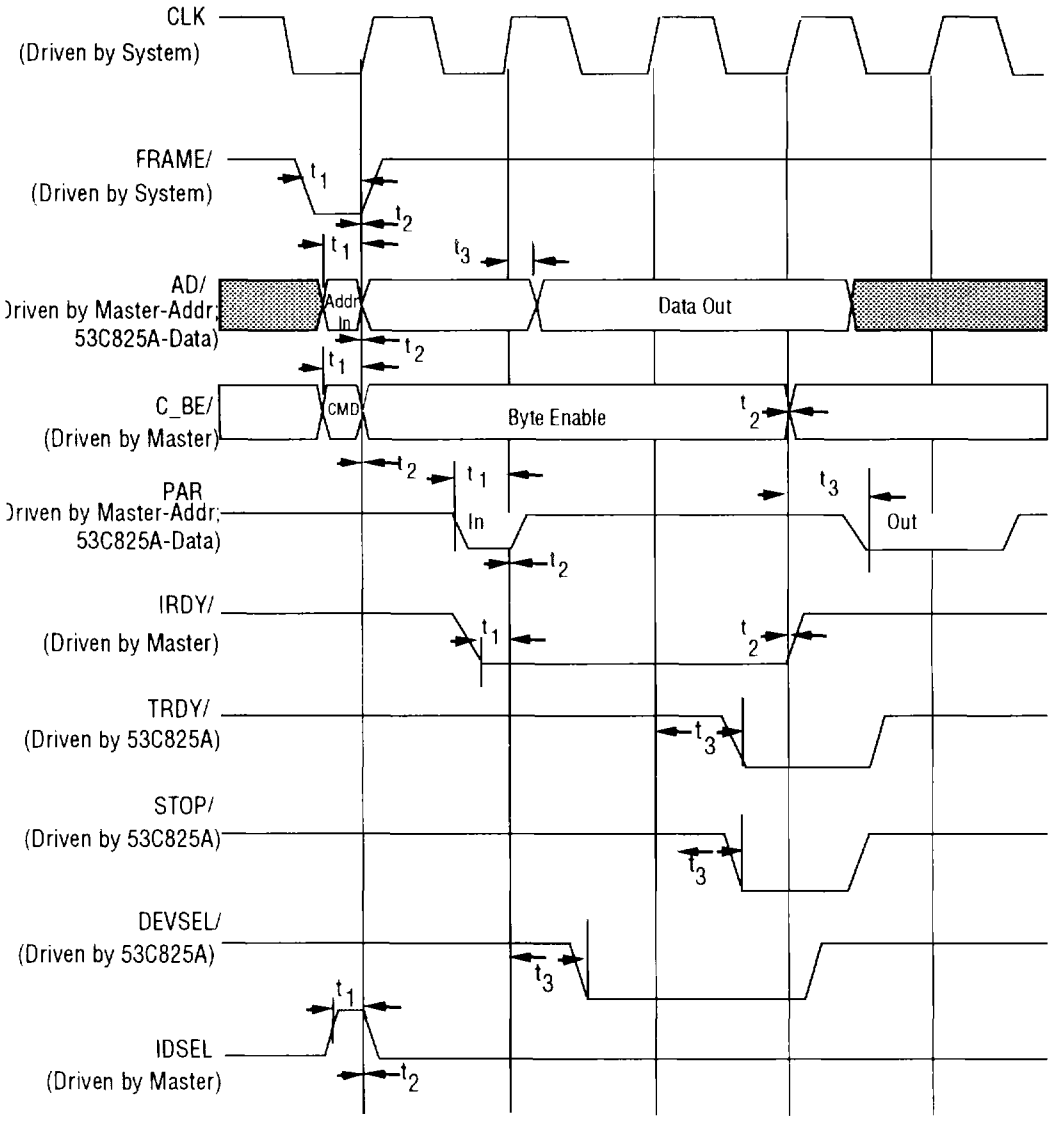


Figure 7-9: Configuration Register Read

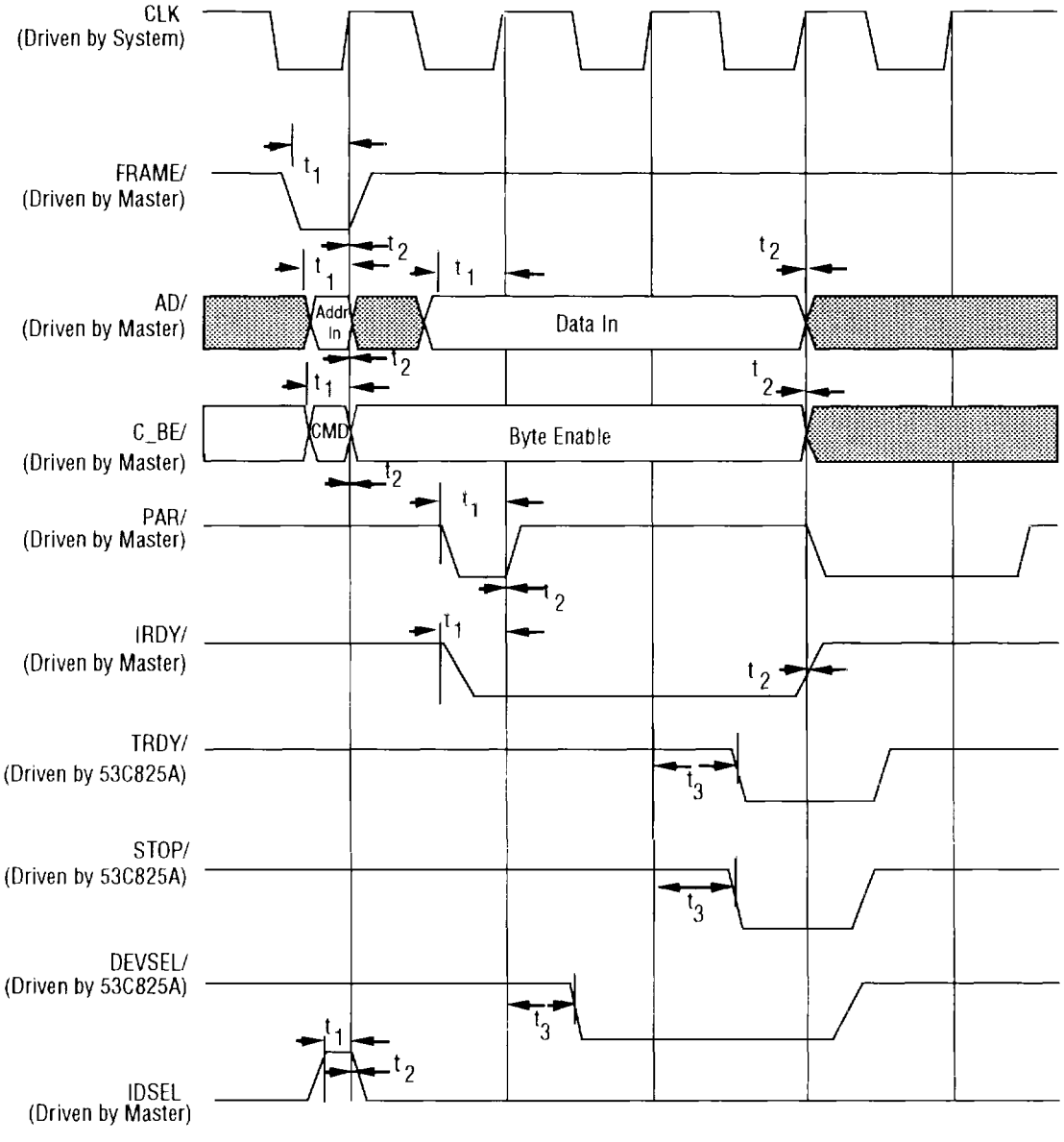


Figure 7-10: Configuration Register Write

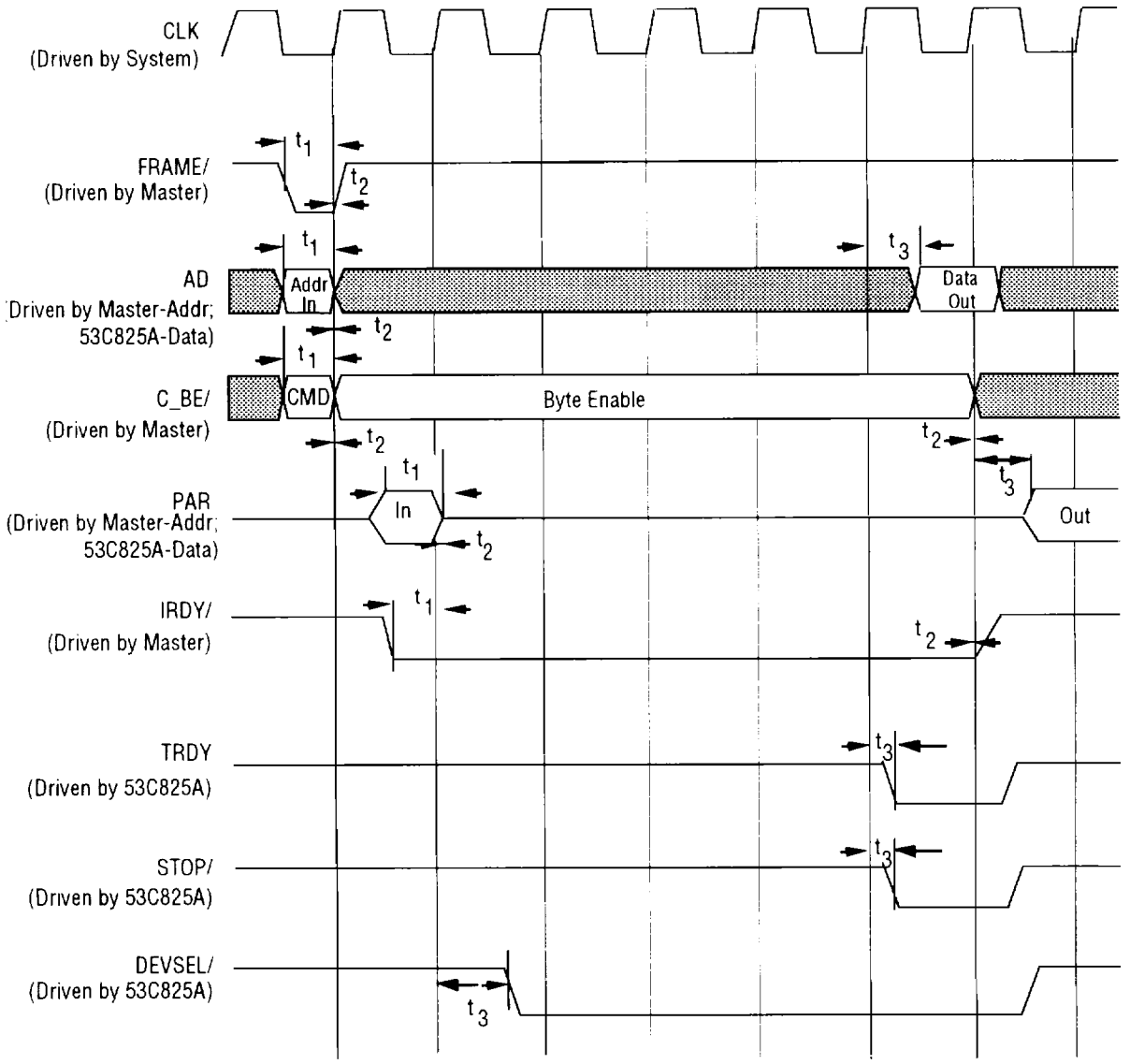


Figure 7-11: Target Read, not from external memory

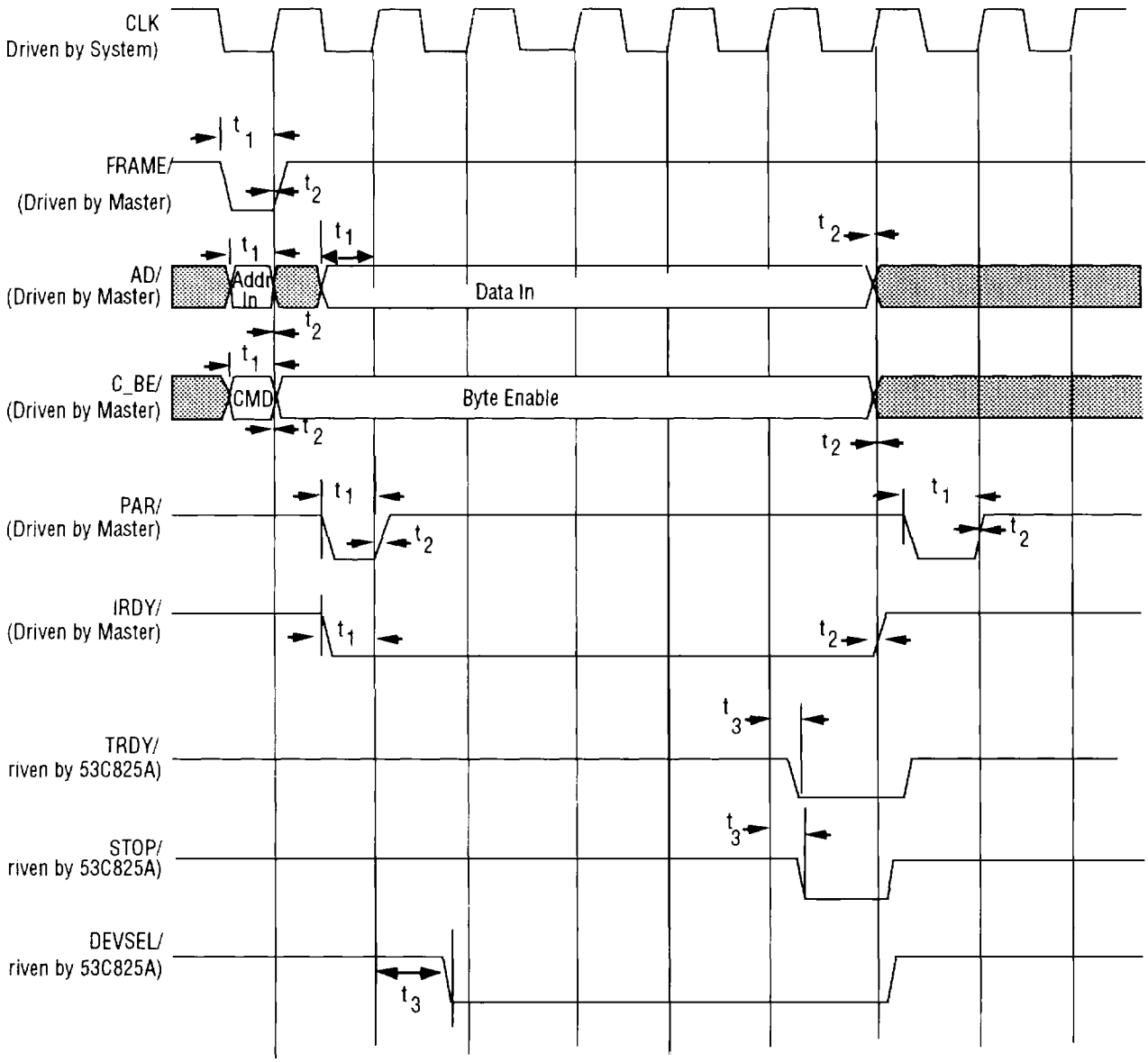


Figure 7-12: Target Write, not to external memory

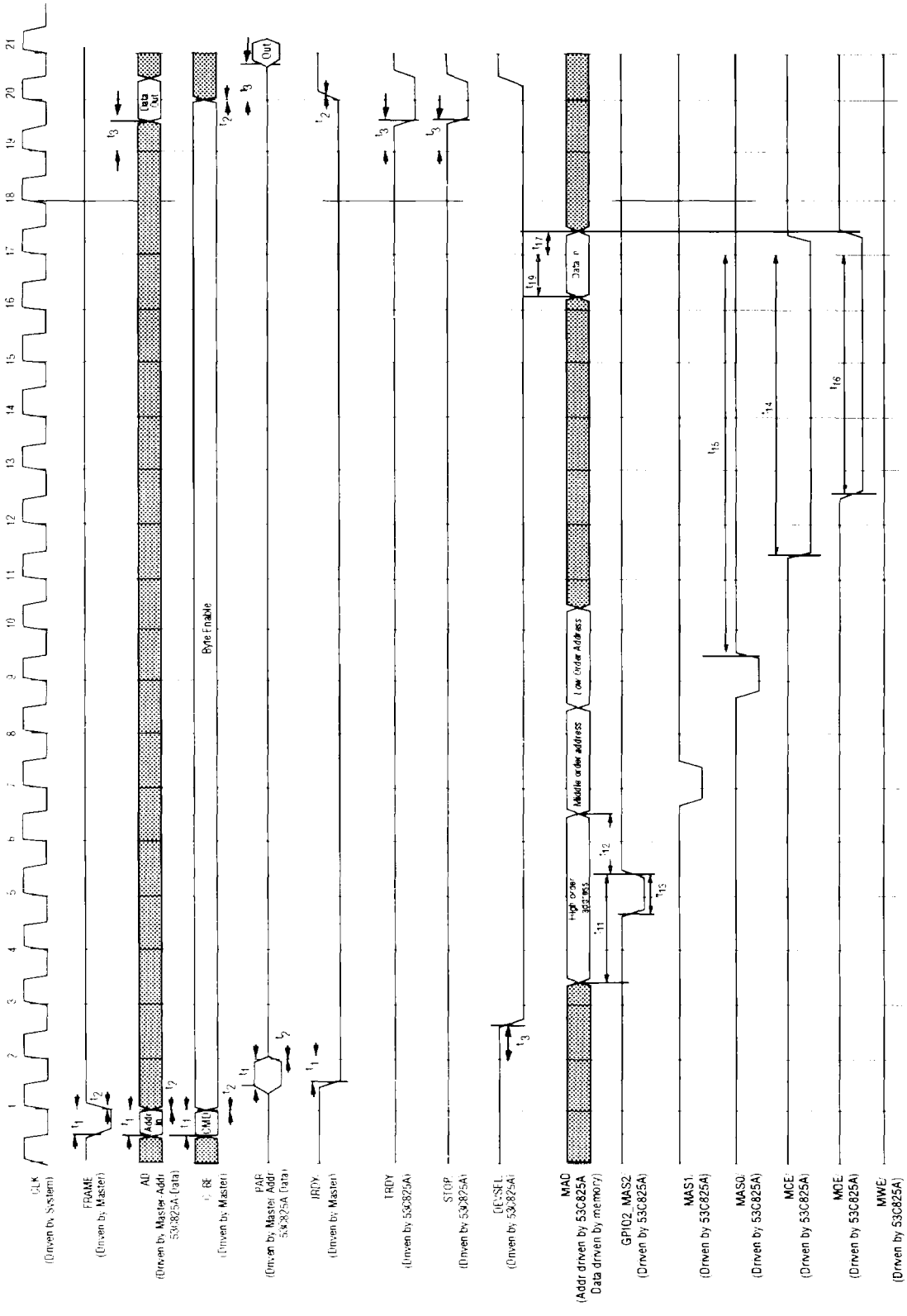


Figure 7-13: Target Read, from external memory

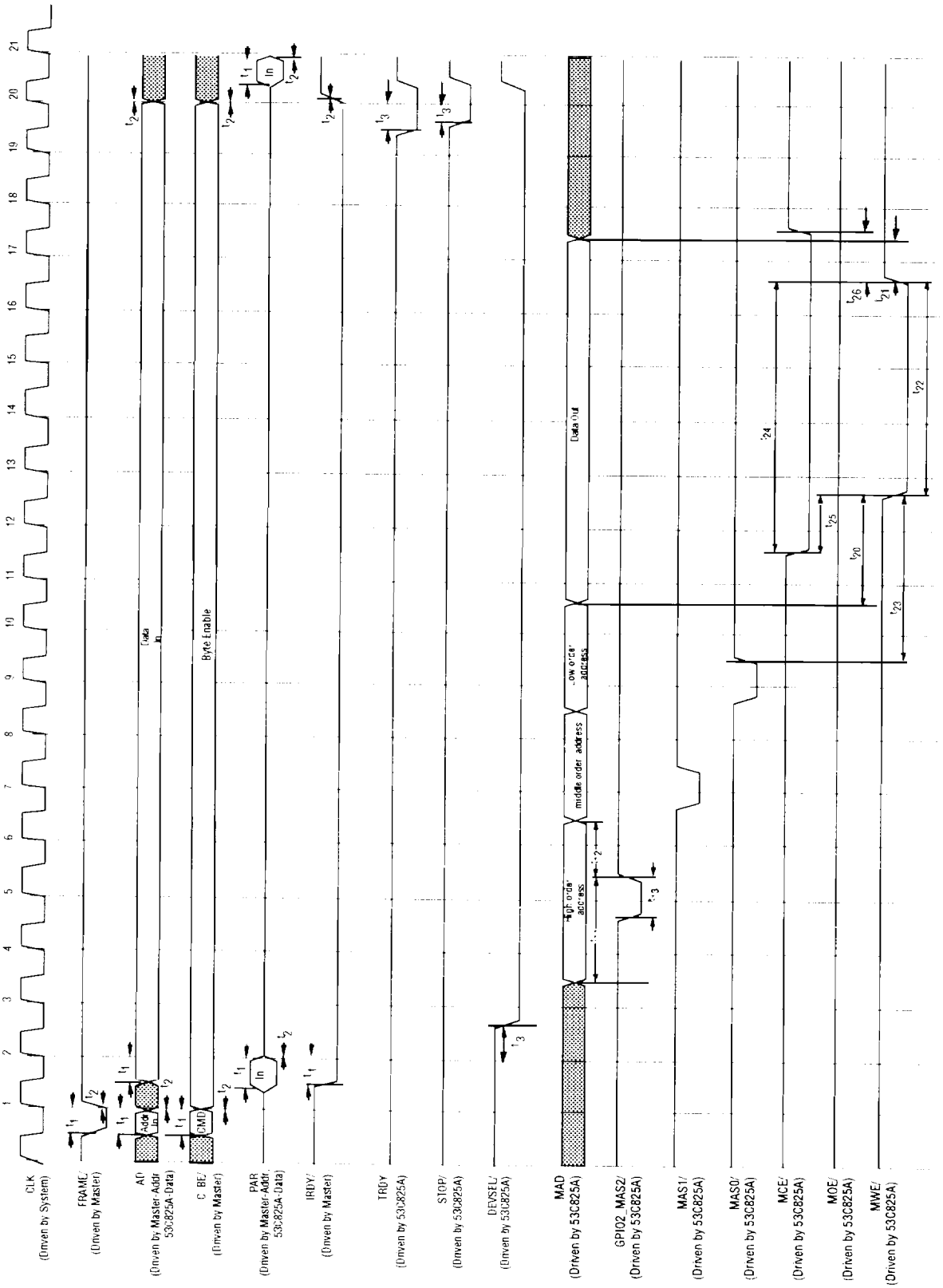


Figure 7-14: Target Write, to external memory

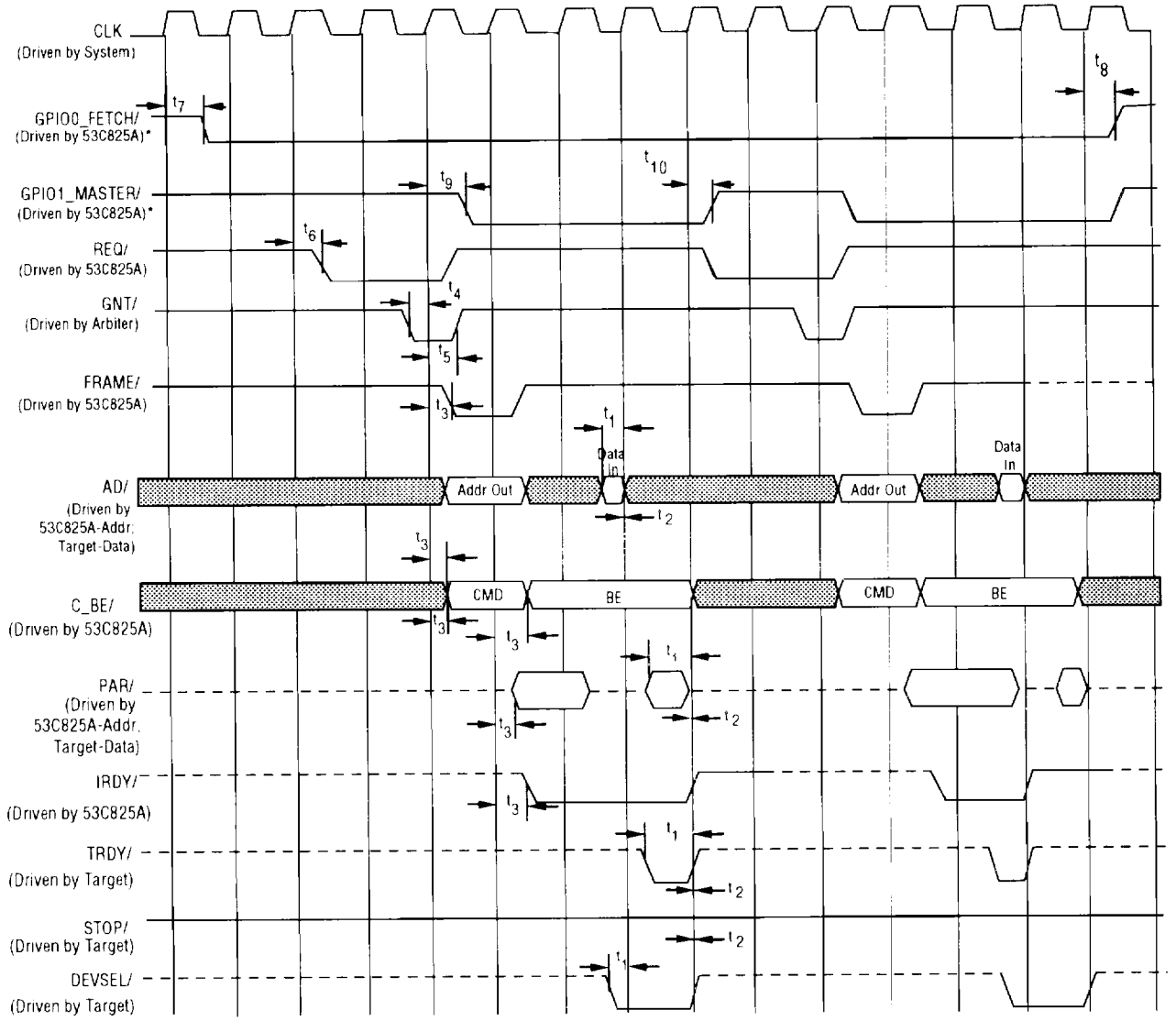


Figure 7-15: Op Code Fetch, non-burst

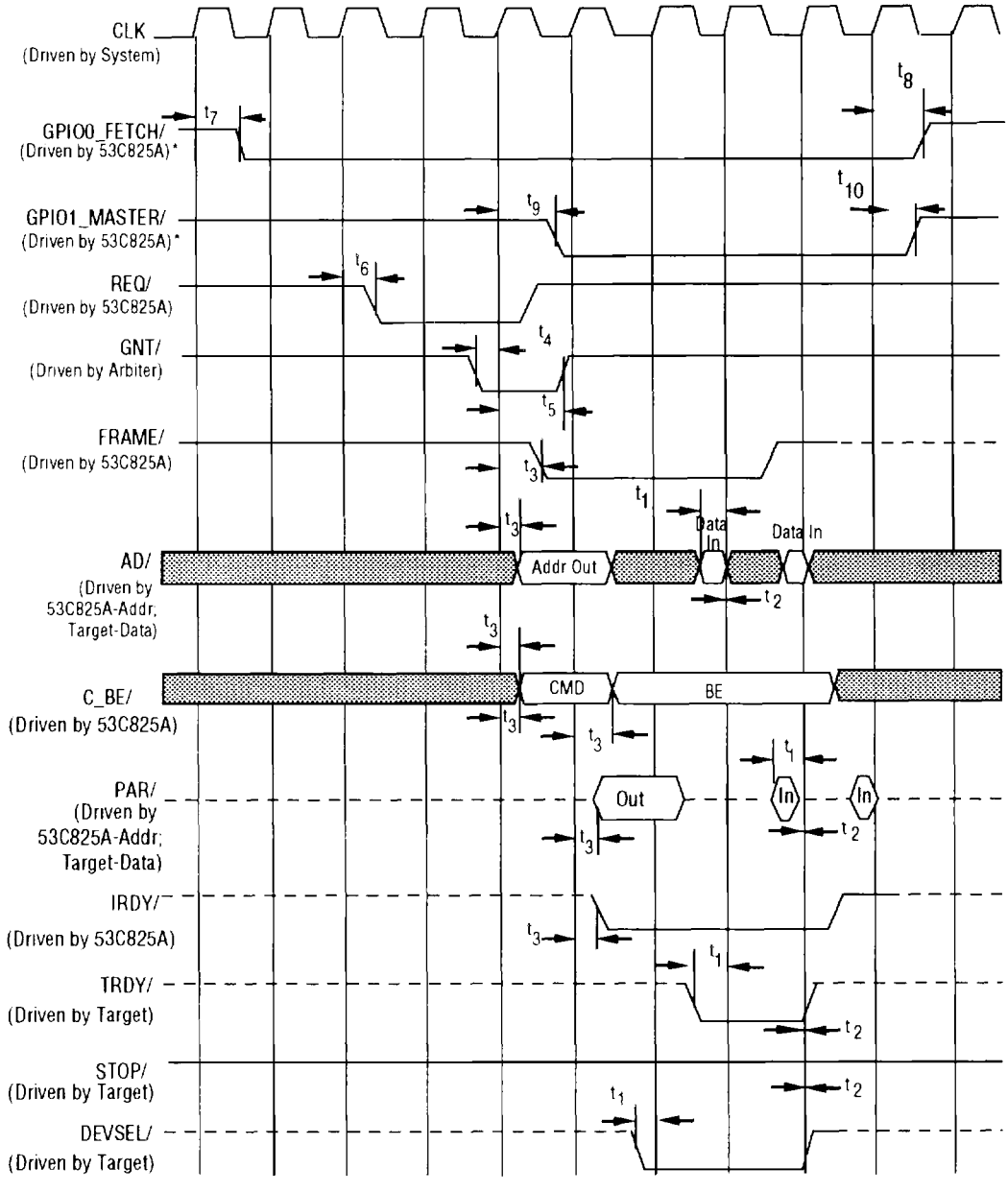


Figure 7-16: Burst Op Code Fetch

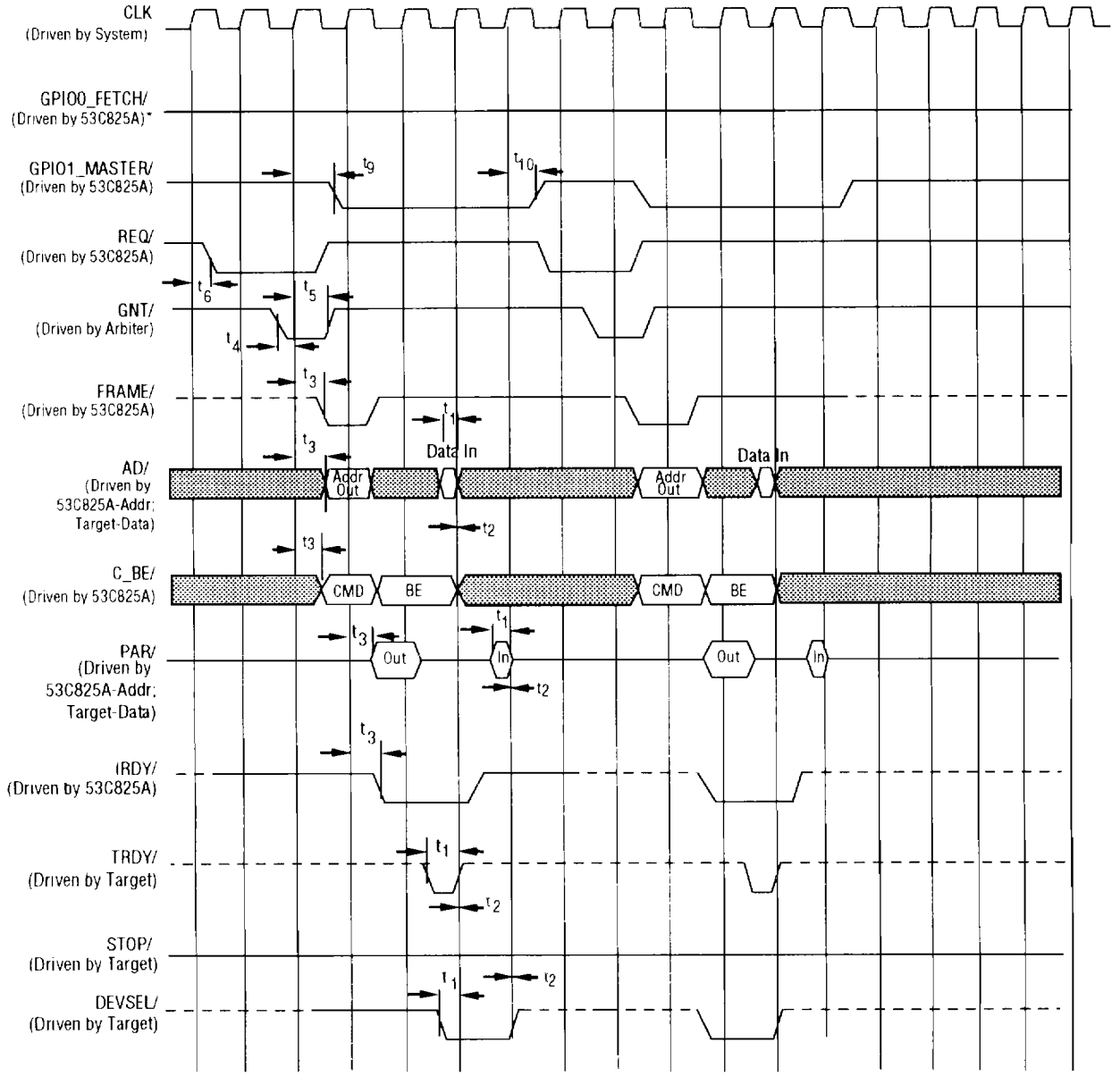


Figure 7-17: Back to Back Read

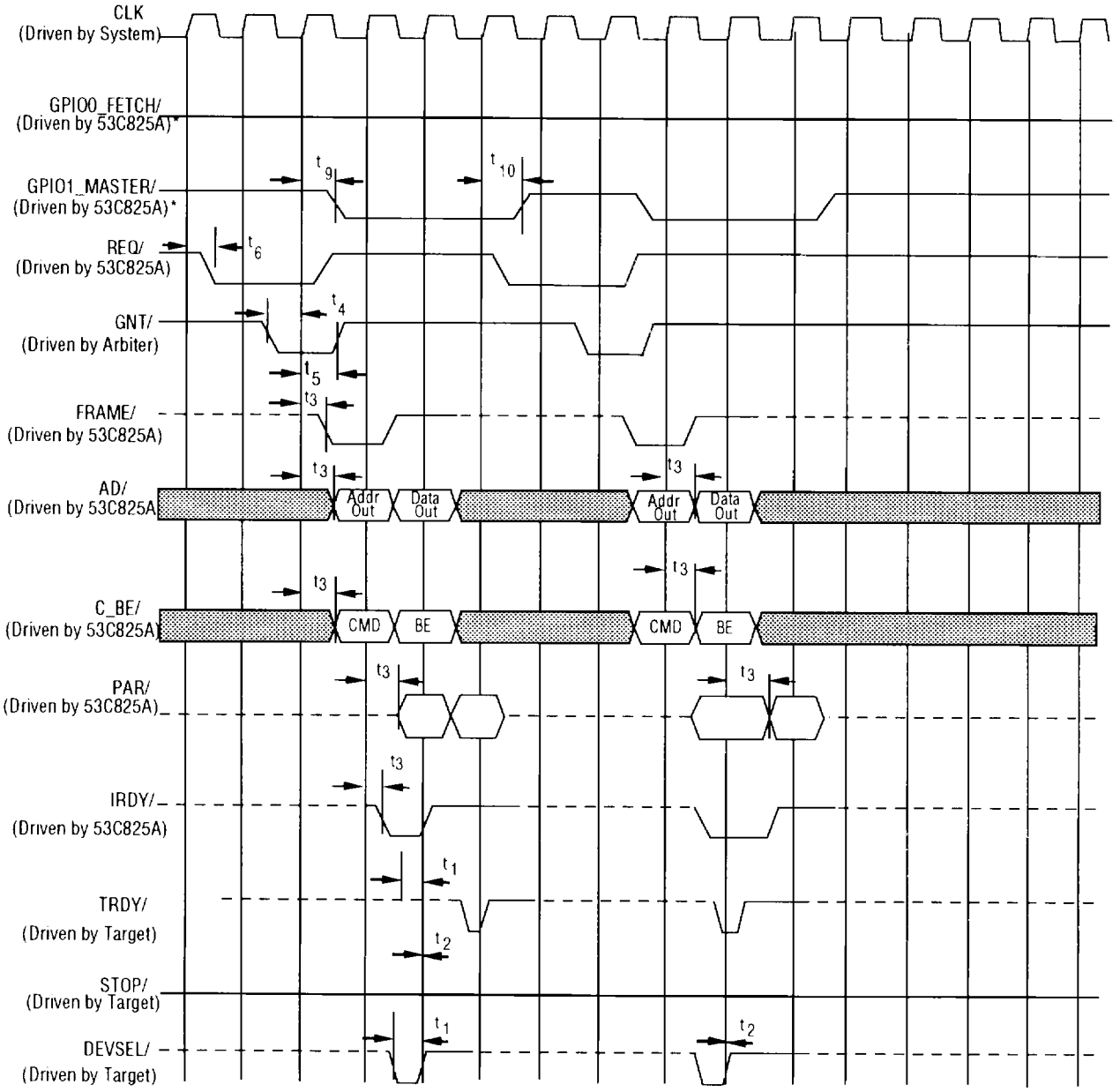


Figure 7-18: Back to Back Write

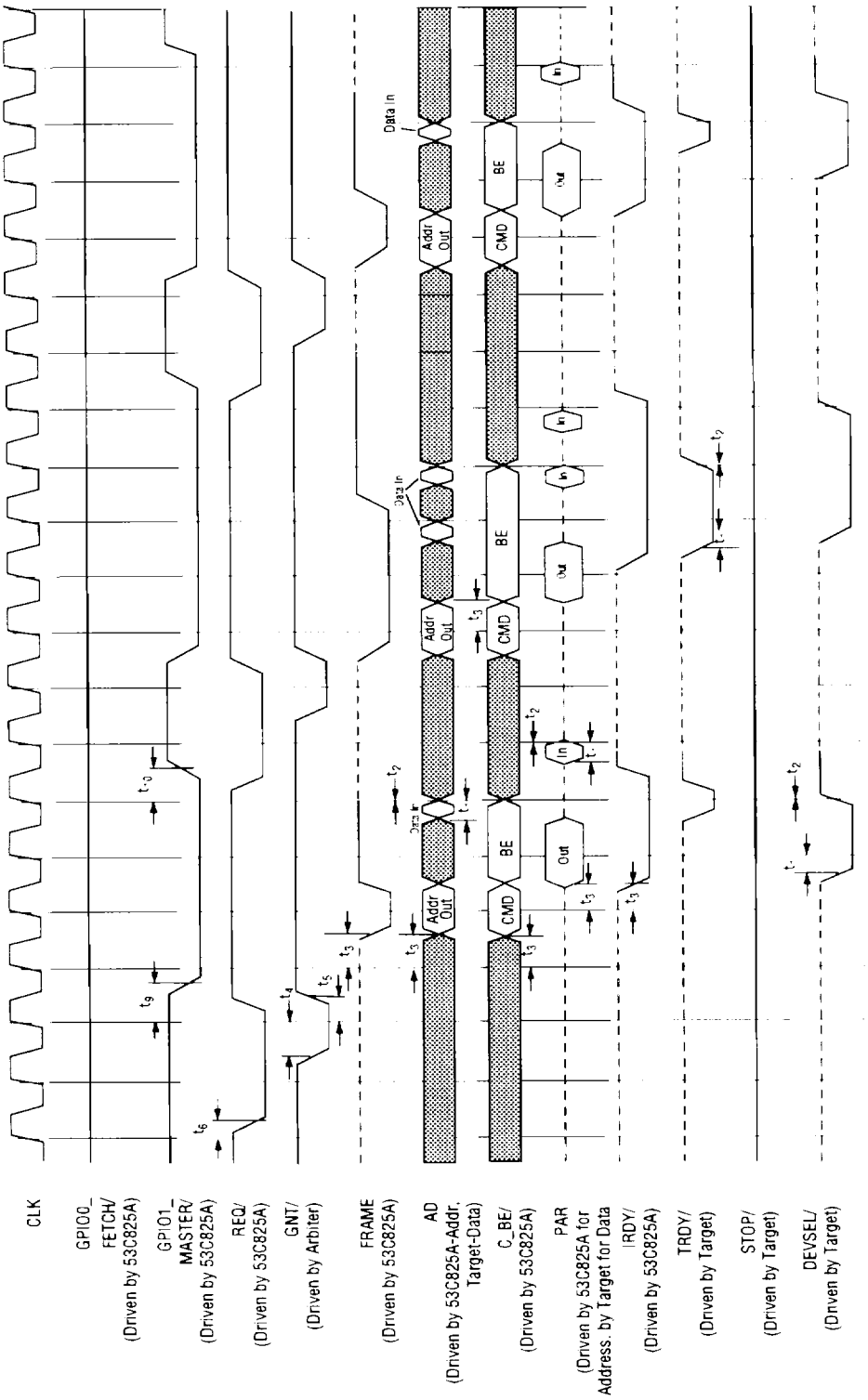


Figure 7-19: Burst Read

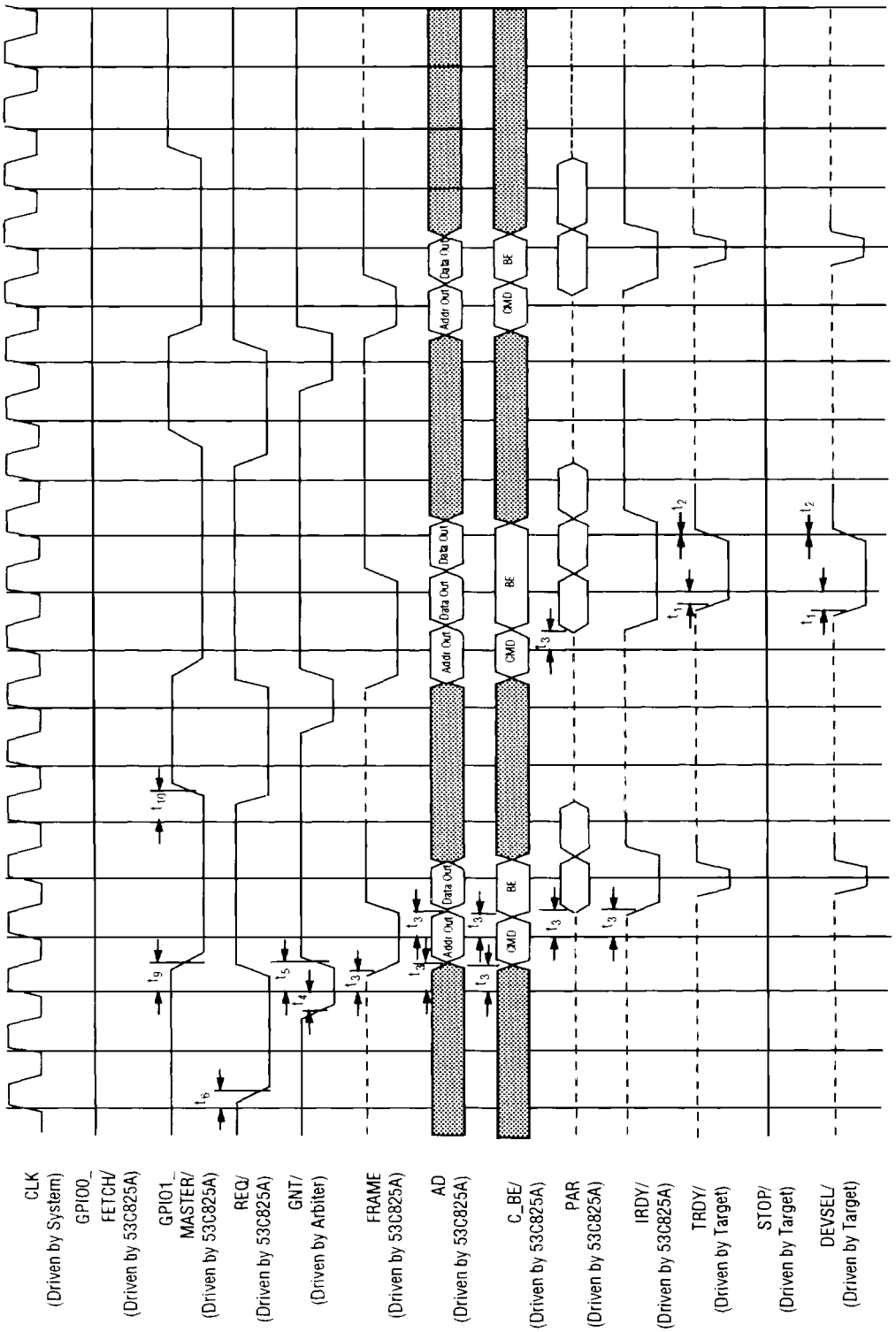


Figure 7-20: Burst Write

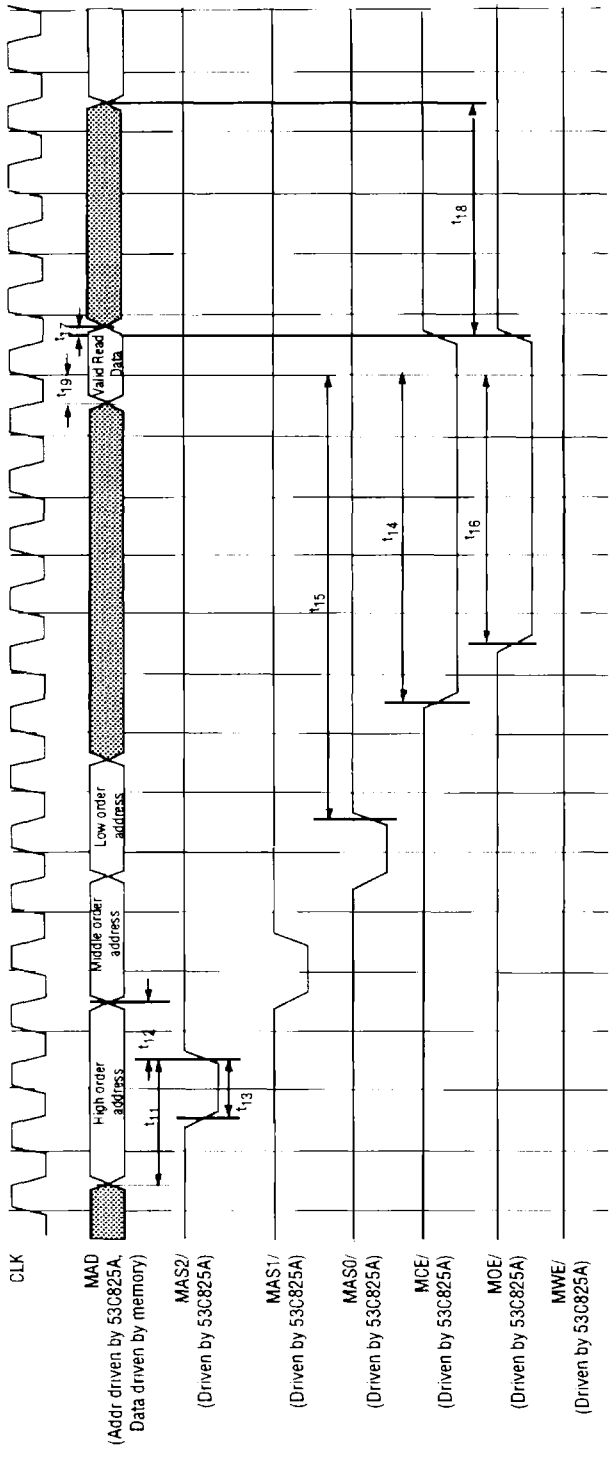


Figure 7-21: Read Cycle, Normal/Fast Memory (≥ 128 KB), single byte access

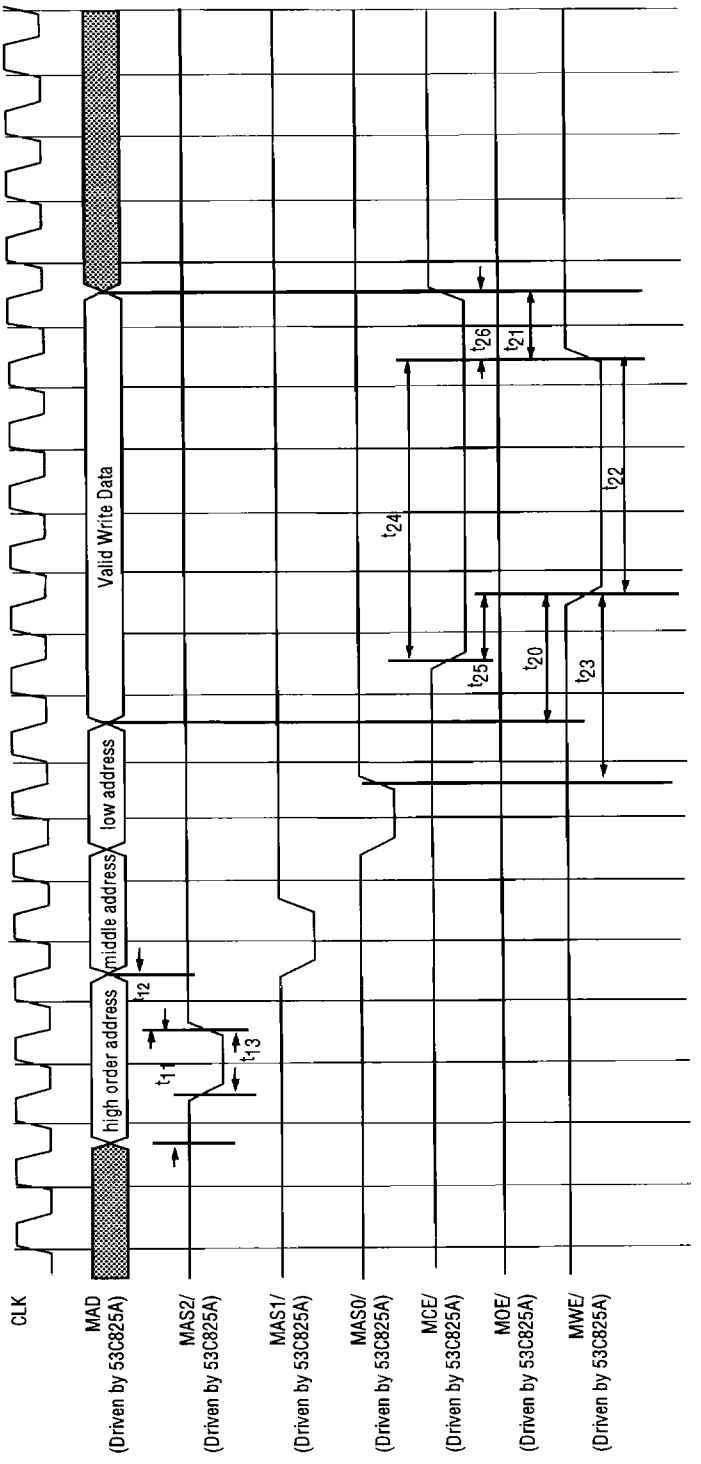


Figure 7-22: Write Cycle, Normal/Fast Memory (≥ 128 KB), single byte access

Electrical Characteristics
PCI and External Memory Interface Timing Diagrams

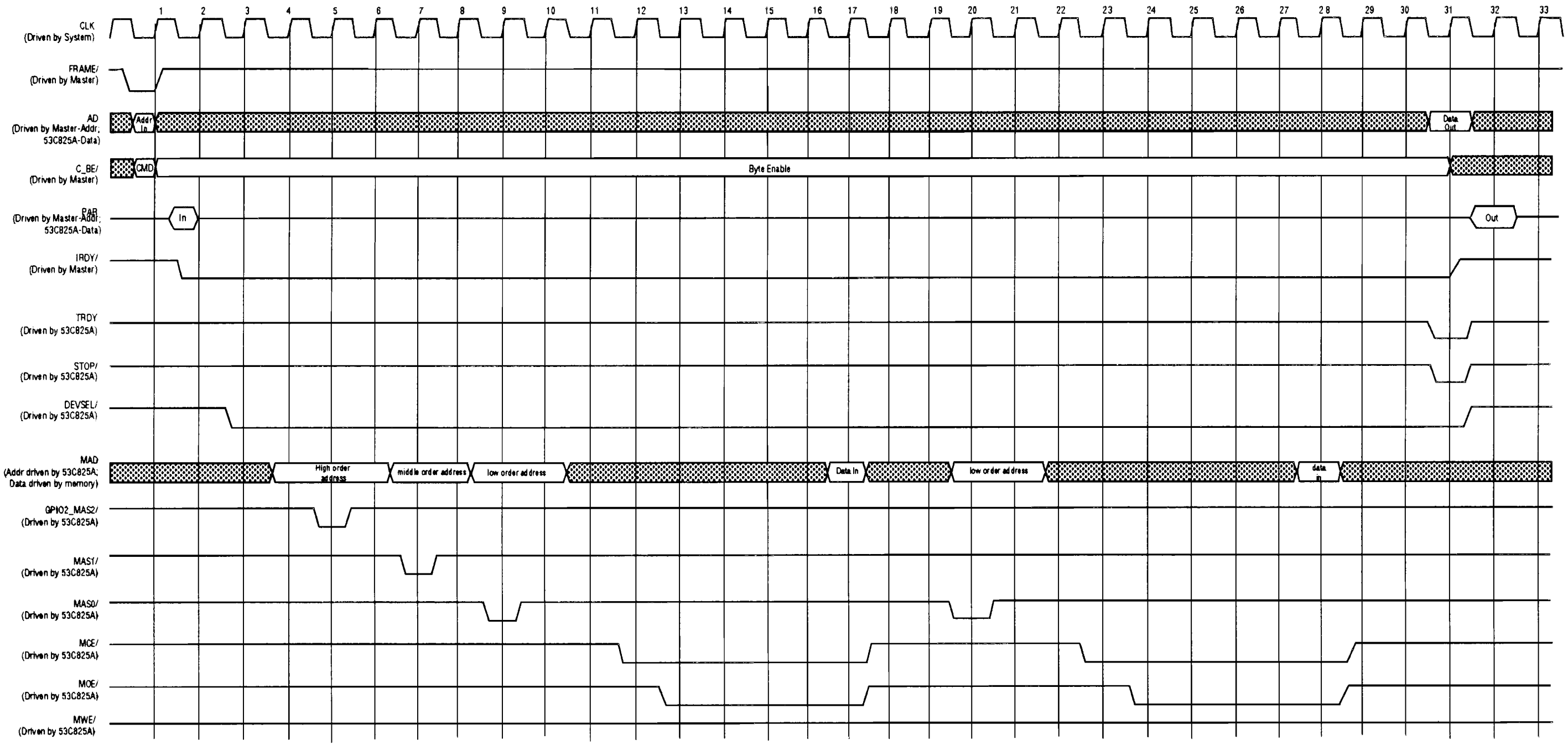


Figure 7-23: Read Cycle, Normal/Fast Memory (≥ 128 KB), multiple byte access

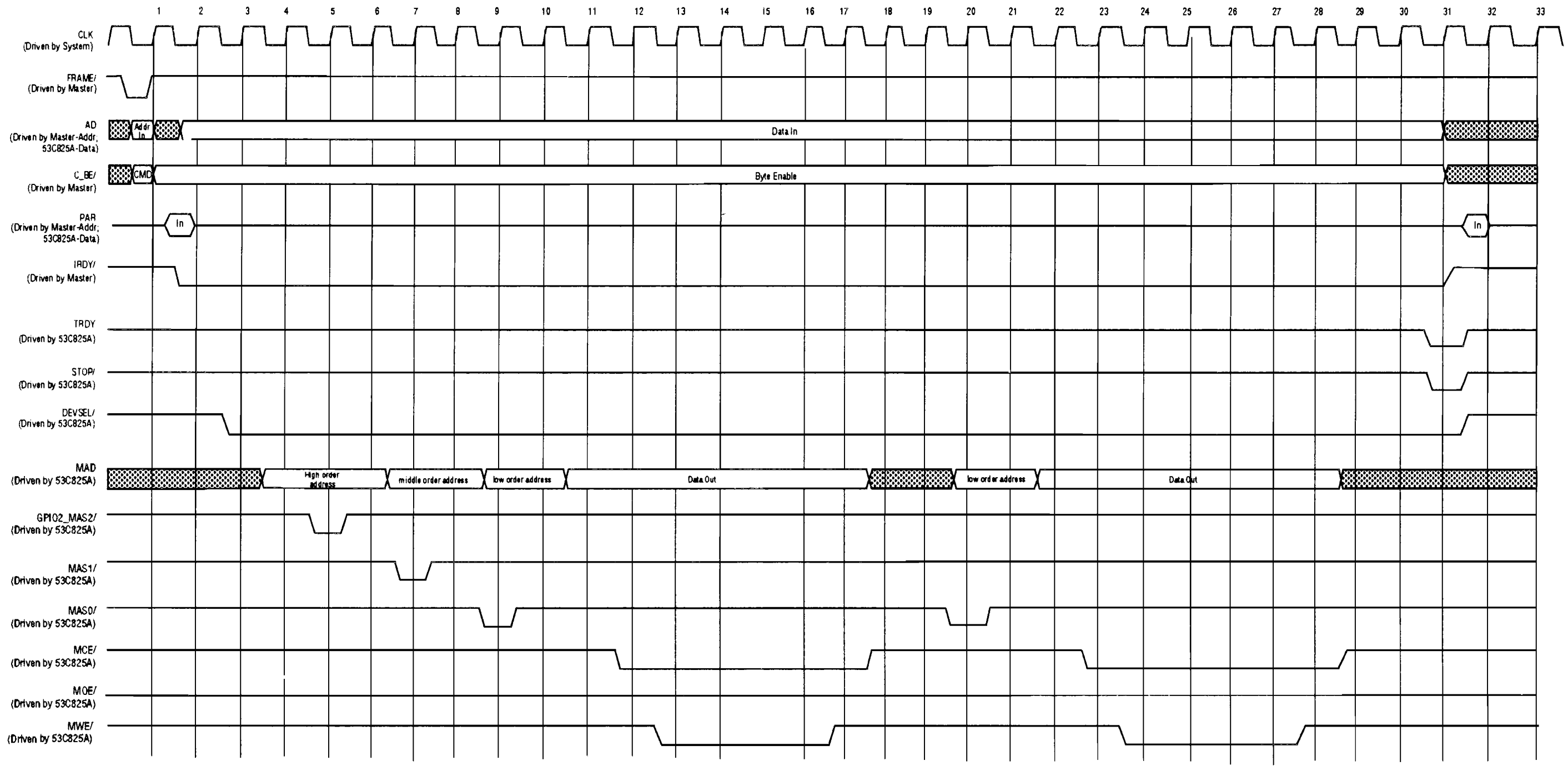


Figure 7-24: Write Cycle, Normal/Fast Memory (≥ 128 KB), multiple byte access

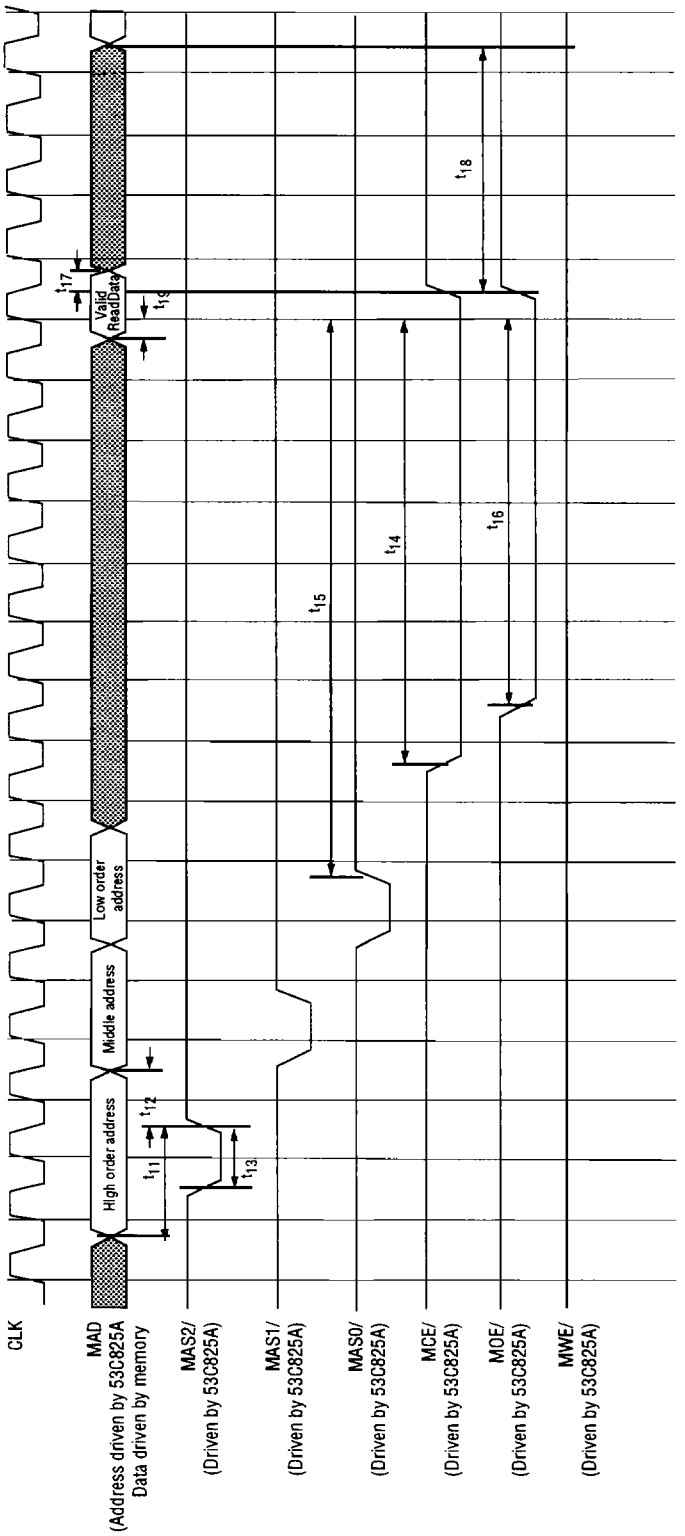


Figure 7-25: Read Cycle, Slow Memory (≥ 128 KB)

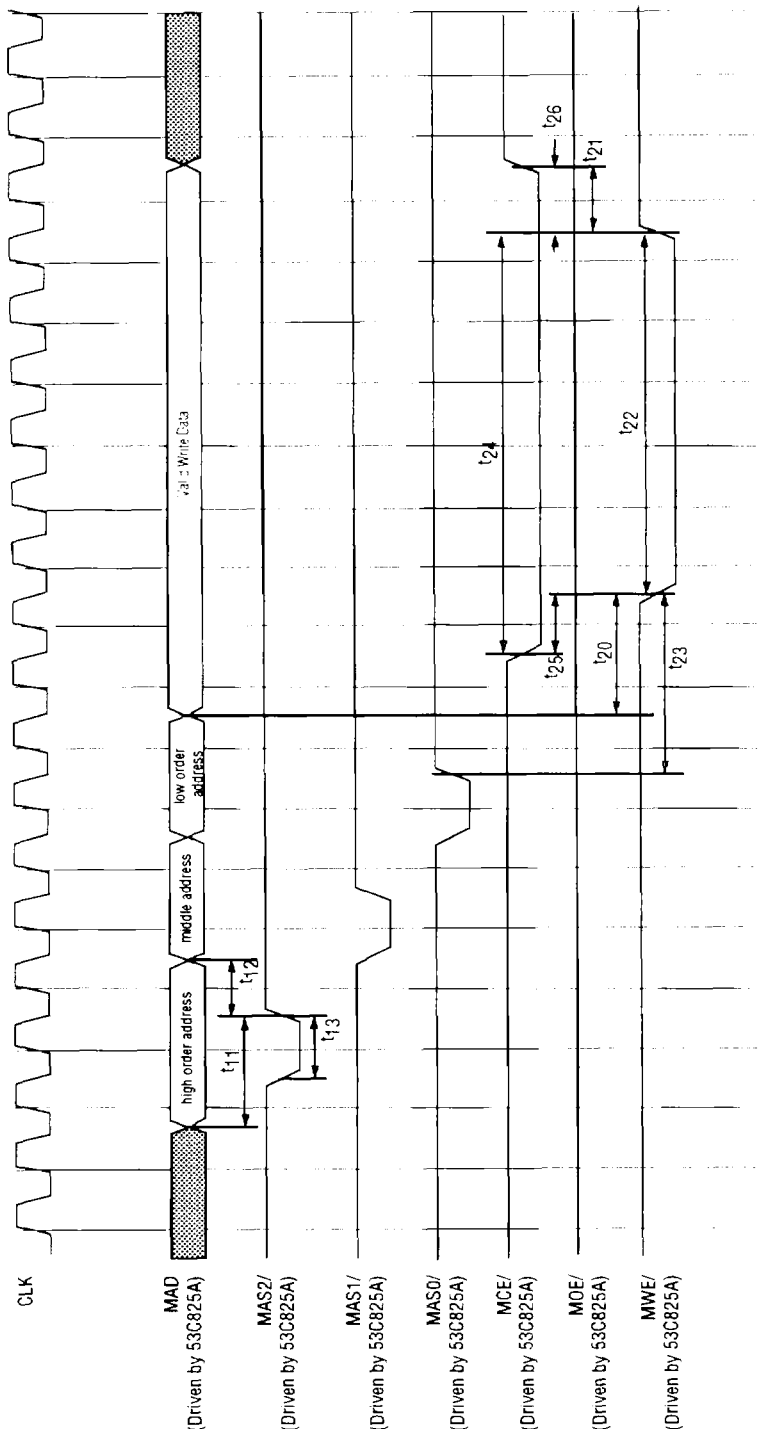


Figure 7-26: Write Cycle, Slow Memory (≥ 128 KB)

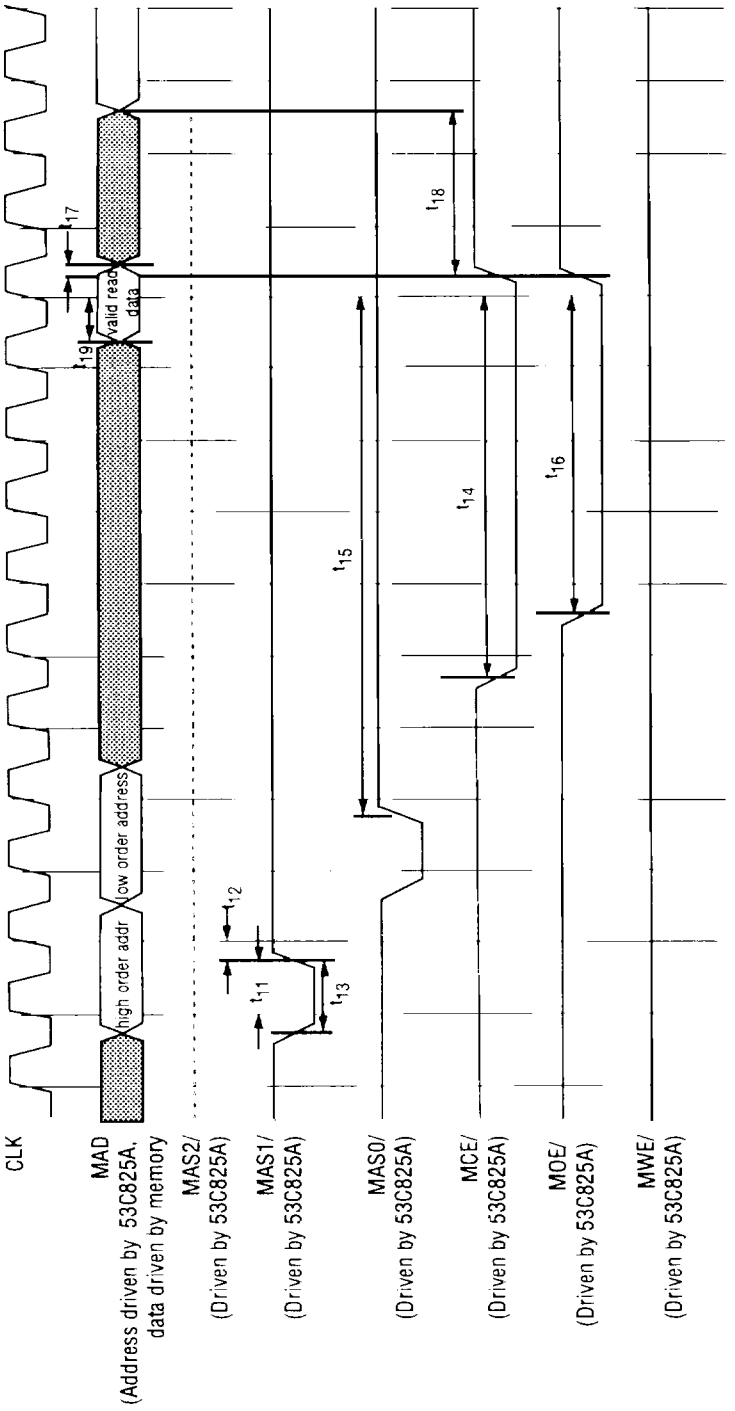


Figure 7-27: Read Cycle, 16 KB ROM

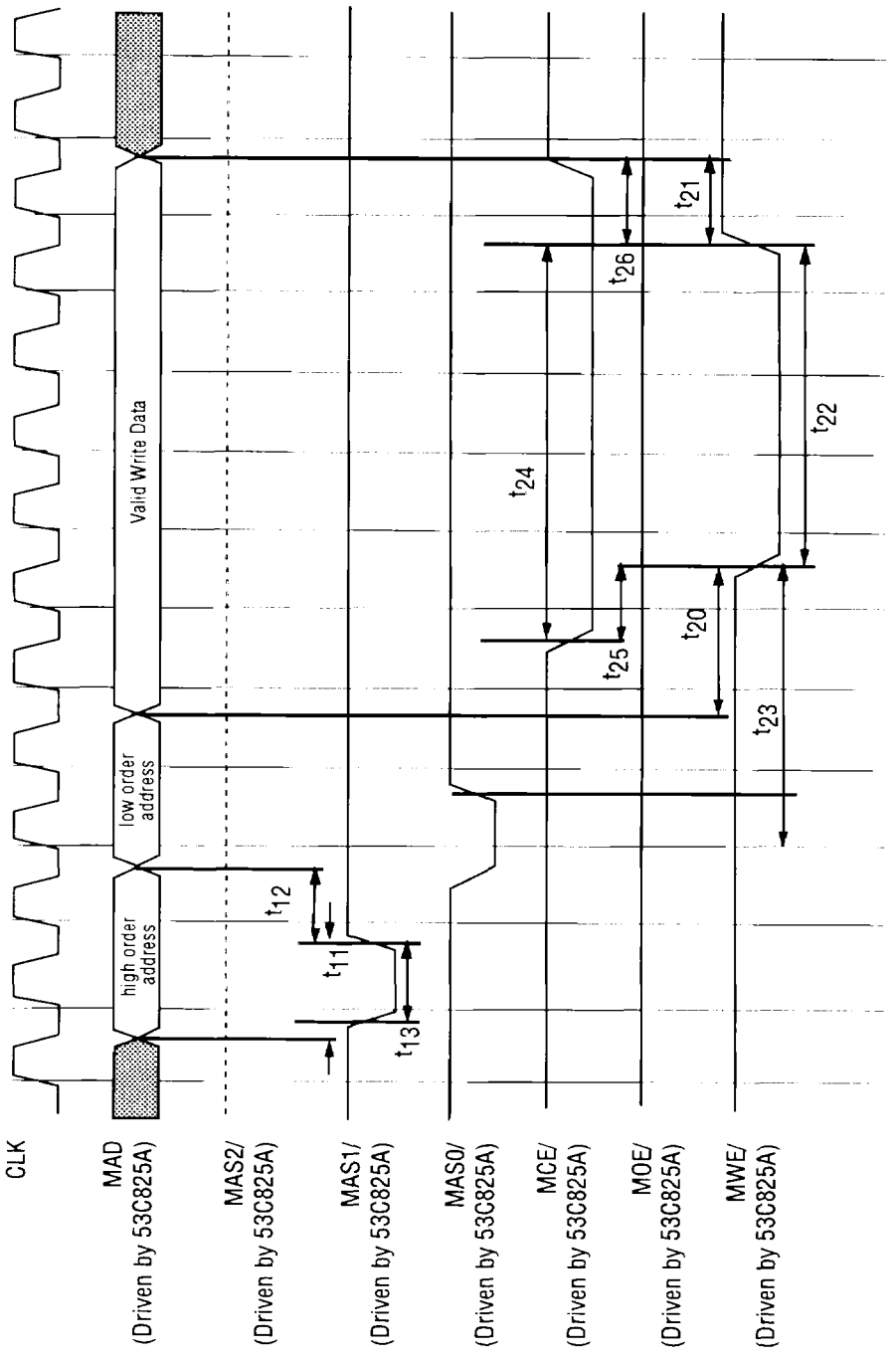


Figure 7-28: Write Cycle, 16 KB ROM

PCI and External Memory Interface Timings

Table 7-16: SYM53C825A PCI and External Memory Interface Timings

Symbol	Parameter	Min	Max	Unit
t_1	Shared signal input setup time	7	-	ns
t_2	Shared signal input hold time	0	-	ns
t_3	CLK to shared signal output valid	-	11	ns
t_4	Side signal input setup time	10	-	ns
t_5	Side signal input hold time	0	-	ns
t_6	CLK to side signal output valid	-	12	ns
t_7	CLK high to FETCH/ low	-	20	ns
t_8	CLK high to FETCH/ high	-	20	ns
t_9	CLK high to MASTER/ low	-	20	ns
t_{10}	CLK high to MASTER/ high	-	20	ns
t_{11}	Address setup to MAS/ high	25	-	ns
t_{12}	Address hold from MAS/ high	15	-	ns
t_{13}	MAS/ pulse width	25	-	ns
t_{14}	MCE/ low to data clocked in	160	-	ns
t_{15}	Address valid to data clocked in	205	-	ns
t_{16}	MOE/ low to data clocked in	100	-	ns
t_{17}	Data hold from address, MOE/, MCE/ change	0	-	ns
t_{18}	Address out from MOE/, MCE/ high	50	-	ns
t_{19}	Data setup to CLK high	5	-	ns
t_{20}	Data setup to MWE/ low	30	-	ns
t_{21}	Data hold from MWE/ high	20	-	ns
t_{22}	MWE/ pulse width	100	-	ns
t_{23}	Address setup to MWE/ low	75	-	ns
t_{24}	MCE/ low to MWE/ high	120	-	ns
t_{25}	MCE/ low to MWE/ low	25	-	ns
t_{26}	MWE/ high to MCE/ high	25	-	ns

SCSI Timings

Figure 7-29: Initiator Asynchronous Send

Symbol	Parameter	Min	Max	Units
t_1	SACK/ asserted from SREQ/ asserted	5	-	ns
t_2	SACK/ deasserted from SREQ/ deasserted	5	-	ns
t_3	Data setup to SACK/ asserted	55	-	ns
t_4	Data hold from SREQ/ deasserted	20	-	ns

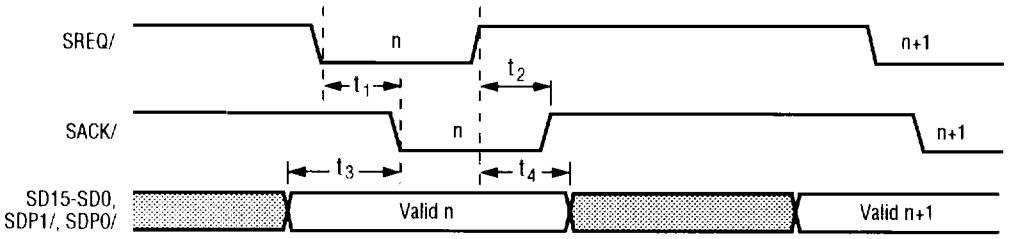


Figure 7-30: Initiator Asynchronous Receive

Symbol	Parameter	Min	Max	Units
t_1	SACK/ asserted from SREQ/ asserted	5	-	ns
t_2	SACK/ deasserted from SREQ/ deasserted	5	-	ns
t_3	Data setup to SREQ/ asserted	0	-	ns
t_4	Data hold from SACK/ asserted	0	-	ns

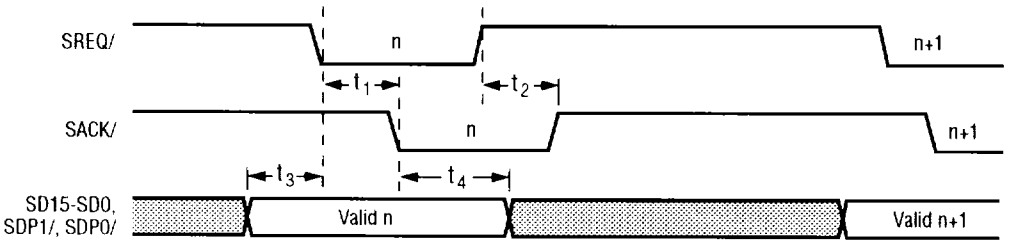


Figure 7-31: Target Asynchronous Send

Symbol	Parameter	Min	Max	Units
t_1	SREQ/ deasserted from SACK/ asserted	5	-	ns
t_2	SREQ/ asserted from SACK/ deasserted	5	-	ns
t_3	Data setup to SREQ/ asserted	55	-	ns
t_4	Data hold from SACK/ asserted	20	-	ns

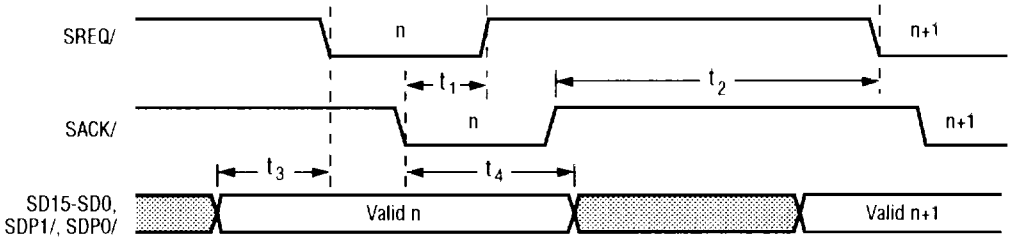
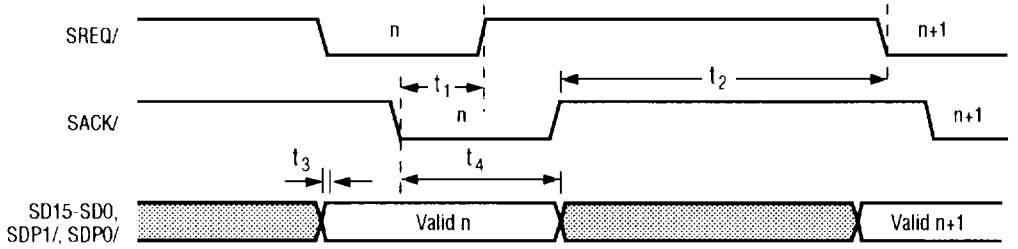


Figure 7-32: Target Asynchronous Receive

Symbol	Parameter	Min	Max	Units
t_1	SREQ/ deasserted from SACK/ asserted	5	-	ns
t_2	SREQ/ asserted from SACK/ deasserted	5	-	ns
t_3	Data setup to SACK/ asserted	0	-	ns
t_4	Data hold from SREQ/ deasserted	0	-	ns



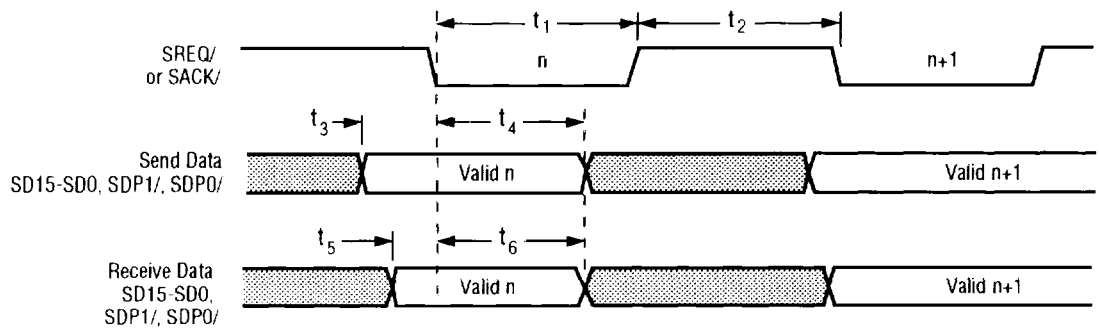


Figure 7-33: Initiator and Target Synchronous Transfers

Table 7-17: SCSI-1 transfers (Single-Ended, 5.0 MB/s)

Symbol	Parameter	Min	Max	Units
t_1	Send SREQ/ or SACK/ assertion pulse width	90	-	ns
t_2	Send SREQ/ or SACK/ deassertion pulse width	90	-	ns
t_1	Receive SREQ/ or SACK/ assertion pulse width	90	-	ns
t_2	Receive SREQ/ or SACK/ deassertion pulse width	90	-	ns
t_3	Send data setup to SREQ/ or SACK/ asserted	55	-	ns
t_4	Send data hold from SREQ/ or SACK/ asserted	100	-	ns
t_5	Receive data setup to SREQ/ or SACK/ asserted	0	-	ns
t_6	Receive data hold from SREQ/ or SACK/ asserted	45	-	ns

Table 7-18: SCSI-1 Transfers (Differential, 4.17 MB/s)

Symbol	Parameter	Min	Max	Units
t_1	Send SREQ/ or SACK/ assertion pulse width	96	-	ns
t_2	Send SREQ/ or SACK/ deassertion pulse width	96	-	ns
t_1	Receive SREQ/ or SACK/ assertion pulse width	84	-	ns
t_2	Receive SREQ/ or SACK/deassertion pulse width	84	-	ns
t_3	Send data setup to SREQ/ or SACK/ asserted	65	-	ns
t_4	Send data hold from SREQ/ or SACK/ asserted	110	-	ns
t_5	Receive data setup to SREQ/ or SACK/ asserted	0	-	ns
t_6	Receive data hold from SREQ/ or SACK/ asserted	45	-	ns

Table 7-19: SCSI-2 Fast Transfers (10.0 MB/s (8-bit transfers) or 20.0 MB/s (16-bit transfers), 40 MHz clock)

Symbol	Parameter	Min	Max	Units
t_1	Send SREQ/ or SACK/ assertion pulse width	35	-	ns
t_2	Send SREQ/ or SACK/ deassertion pulse width	35	-	ns
t_1	Receive SREQ/ or SACK/ assertion pulse width	20	-	ns
t_2	Receive SREQ/ or SACK/ deassertion pulse width	20	-	ns
t_3	Send data setup to SREQ/ or SACK/ asserted	33	-	ns
t_4	Send data hold from SREQ/ or SACK/ asserted	45	-	ns
t_5	Receive data setup to SREQ/ or SACK/ asserted	0	-	ns
t_6	Receive data hold from SREQ/ or SACK/ asserted	10	-	ns

Table 7-20: SCSI-2 Fast Transfers (10.0 MB/s (8-bit transfers) or 20.0 MB/s (16-bit transfers), 50 MHz clock)

Symbol	Parameter	Min	Max	Unit
t_1	Send SREQ/ or SACK/ assertion pulse width	35	-	ns
t_2	Send SREQ/ or SACK/ deassertion pulse width	35	-	ns
t_1	Receive SREQ/ or SACK/ assertion pulse width	20	-	ns
t_2	Receive SREQ/ or SACK/ deassertion pulse width	20	-	ns
t_3	Send data setup to SREQ/ or SACK/ asserted	33	-	ns
t_4	Send data hold from SREQ/ or SACK/ asserted	40**	-	ns
t_5	Receive data setup to SREQ/ or SACK/ asserted	0	-	ns
t_6	Receive data hold from SREQ/ or SACK/ asserted	10	-	ns

**Transfer period bits (bits 6-4 in the SXFER register) are set to zero and the Extra Clock Cycle of Data Setup bit (bit 7 in SCNTL1) is set.*

***Analysis of system configuration is recommended due to reduced driver skew margin in differential systems*

Note: for fast SCSI, set the TolerANT Enable bit (bit 7 in STEST3).