Digital-to-Analog Converter

8-Bit, 200MHz

The TDC1018 is an 8-bit digital-to-analog converter, designed for 200MHz operation and capable of directly driving a 75 Ohm load to standard video levels. Most applications require no extra registering, buffering, or deglitching. Four special level controls make the device ideal for video applications. All data and control inputs are ECL compatible.

The TDC1018 is built with TRW's OMICRON-B™ 1-micron bipolar process. On-chip data registers and precise matching of propagation delays make the TDC1018 inherently low-glitching. The TDC1018 offers high performance, low power consumption, and video compatibility in a 24 pin DIP or a 28 contact chip carrier.

Features

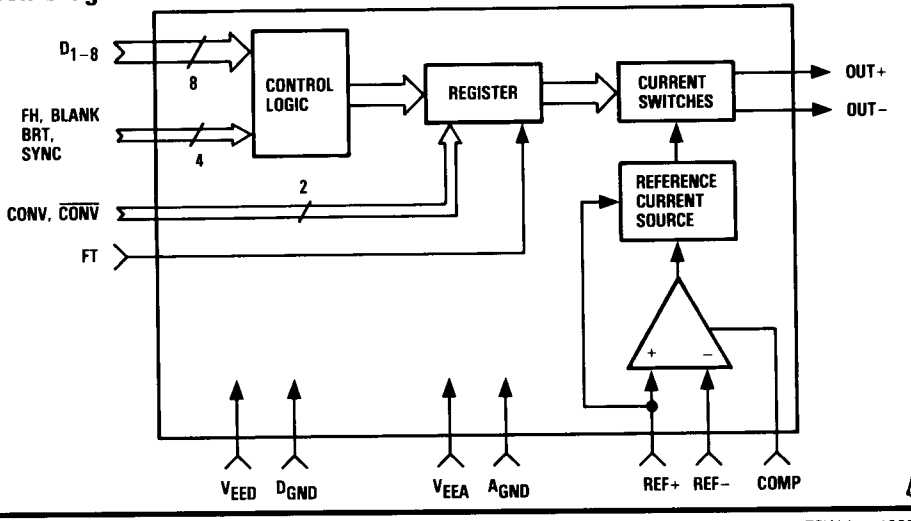
- Monolithic "Graphics-Ready"
- 125MHz Digital Update Rate, TDC1018
- 200MHz Digital Update Rate, TDC1018-1
- 8-Bit Resolution
- 1/2 LSB Linearity
- Registered Data And Video Controls
- Complementary Current Outputs
- Video Controls: SYNC, BLANK, BRIGHT, Force High
- Inherently Low Glitch Energy
- ECL Compatible Inputs
- Multiplying Mode Capability
- Can Be Operated In TTL Systems
- Available In A 24 Pin DIP And 28 Contact Chip Carrier
- Single −5.2V Power Supply

B

Applications

- RGB Graphics
- High Resolution Video
- Raster Graphic Displays
- Digital Synthesizers
- Automated Test Equipment
- Digital Transmitters/Modulators

Functional Block Diagram



TRW LSI Products Inc.
P.O. Box 2472
La Jolla, CA 92038

Phone: (619) 457-1000
FAX: (619) 455-6314

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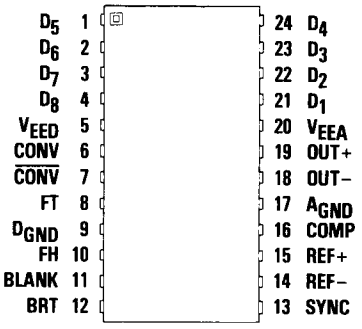
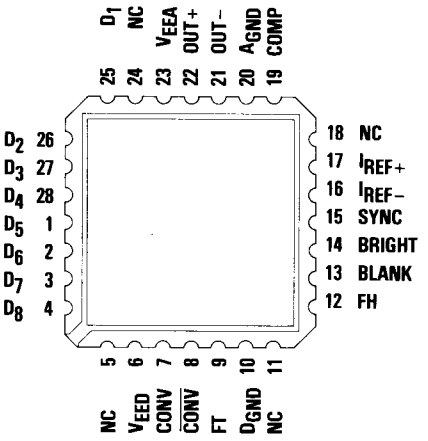
Pin Assignments



24 Pin CERDIP – B7 Package



28 Contact Chip Carrier – C3 Package

Functional Description

General Information

The TDC1018 develops complementary analog output currents proportional to the product of the digital input data and analog reference current. All data and control inputs are compatible with standard ECL logic levels. FeedThrough control (FT) determines whether data and control inputs are synchronous or asynchronous. If FT is LOW, each rising edge of the CONVert clock (CONV) latches decoded data and control values into an internal D-type register. The registered values are then converted into the appropriate analog output by switched current sinks. When FT is HIGH, data and control inputs are not registered, and the analog output asynchronously tracks the input values. FT is the only asynchronous input, and is normally used as a DC control.

The TDC1018 uses a segmented approach in which the four MSBs of the input data are decoded into a parallel "Thermometer" code, which drives fifteen identical current sinks to produce sixteen coarse output levels. The LSBs of the input drive four binary-weighted current switches, with a total contribution of one-sixteenth of full-scale. The LSB and MSB currents are summed to provide 256 analog output levels.

Special control inputs, SYNC, BLANK, Force High (FH) and BRight (BRT), drive appropriately weighted current sinks which add to the output current to produce specific output levels especially useful in video applications.

Power

To provide highest noise immunity, the TDC1018 operates from separate analog and digital power supplies, V_{EEA} and V_{EED}, respectively. Since the required voltage for both V_{EEA} and V_{EED} is $-5.2V$, these may ultimately be connected to the same power source, but individual high-frequency decoupling for each supply is recommended. A typical decoupling network is shown in *Figure 7*. The return for I_{EED}, the current drawn from the V_{EED} supply, is D_{GND}. The return for I_{EEA} is A_{GND}. All power and ground pins MUST be connected.

Although the TDC1018 is specified for a nominal supply of $-5.2V$, operation from a $+5.0V$ supply is possible provided that the relative polarities of all voltages are maintained.

For additional information concerning the use of ECL D/A converters in a $+5V$ system, refer to *TRW Application Note TP-33 "Using the TDC1018 and TDC1034 in a TTL Environment."*

Reference

The TDC1018 has two reference inputs: REF+ and REF−, which are noninverting and inverting inputs of an internal reference buffer amplifier. The output of this operational amplifier serves as a reference for the current sinks. The feedback loop is internally connected around one of the current sinks to achieve high accuracy (see *Figure 4*).

The analog output currents are proportional to the digital data and reference current, I_{REF}. The full-scale output value may be adjusted over a limited range by varying the reference current. Accordingly, the stability of the analog output depends primarily upon the stability of the reference. A method of achieving a stable reference is shown in *Figure 7*.

The reference current is fed into the REF+ input, while REF− is typically connected to a negative reference voltage through a resistor chosen to minimize input offset bias current effects.

A COMPensation input (COMP), is provided for external compensation of the TDC1018's reference amplifier. A capacitor (C_C) should be connected between COMP and the V_{EEA} supply, keeping lead lengths as short as possible. The value of the compensation capacitor determines the effective bandwidth of the amplifier. In general, decreasing C_C increases bandwidth and decreases amplifier stability. For applications in which the reference is constant, C_C should be large, while smaller values of C_C may be chosen if dynamic modulation of the reference is required.

Controls

The TDC1018 has four special video control inputs: SYNC, BLANK, Force High (FH), and BRighT (BRT), in addition to a clock FeedThrough control (FT). All controls are standard ECL level compatible, and include internal pulldown resistors to force unused controls to a logic LOW (inactive) state.

Typically the TDC1018 is operated in the synchronous mode, which assures the highest conversion rate and lowest spurious output noise. By asserting FT, the input registers are disabled, allowing data and control changes to asynchronously feed-through to the analog output. Propagation delay from input change (control or data) to analog output is minimized in the asynchronous mode of operation.

In the synchronous mode, the video control inputs are registered by the rising edge of the CONV clock in a manner similar to the data inputs. The controls, like data, must be present at the inputs for a setup time of t_S (ns) before, and a hold time of t_H (ns) after the rising edge of CONV in order to be registered. In the asynchronous mode, the setup and hold times are irrelevant and minimum pulse widths HIGH and LOW become the limiting factor.

Asserting the video controls produces various output levels which are used for frame synchronization, horizontal blanking, etc., as described in video system standards such as RS-170 and RS-343A. The effect of the video controls on the analog outputs is shown in *Table 1*. Special internal logic governs the interaction of these controls to simplify their use in video applications. BLANK, SYNC, and Force High override the data inputs. SYNC overrides all other inputs, and produces full negative video output. Force High drives the internal digital data to full-scale, giving a reference white video level output. The BRT control creates a "whiter than white" level by adding 10% of the full-scale value to the present output level, and is especially useful in graphics displays for highlighting cursors, warning messages, or menus. For non-video applications, the special controls can be left unconnected.

Data Inputs

Data inputs to the TDC1018 are standard single-ended ECL level compatible. Internal pulldown resistors force unconnected data inputs to logic LOW. Input registers are provided for synchronous data entry and lowest differential data propagation delay (skew), which minimizes glitching.

In the registered mode, valid data must be present at the input a setup time t_S (ns) before, and a hold time t_H (ns) after the rising edge of CONV. When FT is HIGH, data input is asynchronous and the input registers are disabled. In this case the analog output changes asynchronously in direct response to the input data.

Convert

CONVert (CONV) is a differential ECL compatible clock input whose rising edge synchronizes data and control entry into the TDC1018. Within the constraints shown in *Figure 2*, the actual switching threshold of CONV is determined by $\overline{CONV}$. CONV may be driven single-ended by connecting $\overline{CONV}$ to a suitable bias voltage (V_{BB}). The bias voltage chosen will determine the switching threshold of CONV. However, for best performance, CONV must be driven differentially. This will minimize clock noise and power supply/output intermodulation. Both clock inputs must normally be connected, with $\overline{CONV}$ being the complement of CONV.

Analog Outputs

The two analog outputs of the TDC1018 are high-impedance complementary current sinks which vary in proportion to the input data, controls, and reference current values. The outputs are capable of directly driving a dual 75 Ohm load to standard video levels. The output voltage will be the product of the output current and effective load impedance, and will usually be between 0V and −1.07V in the standard configuration (see *Figure 5*). In this case, the OUT− output gives a DC shifted video output with "sync down." The corresponding output from OUT+ is also DC shifted and inverted, or "sync up."

Package Interconnections

Signal Type	Signal Name	Function	Value	B7 Package Pins	C3 Package Pins
Power	V_{EEA}	Analog Supply Voltage	−5.2V	20	23
	V_{EED}	Digital Supply Voltage	−5.2V	5	6
	A_{GND}	Analog Ground	0.0V	17	20
	D_{GND}	Digital Ground	0.0V	9	10
Reference	REF−	Reference Current − Input	Op-Amp Virtual Ground	14	16
	REF+	Reference Current + Input	Op-Amp Virtual Ground	15	17
	COMP	COMPensation Input	C_C	16	19
Controls	FT	Register FeedThrough Control	ECL	8	9
	FH	Data Force High Control	ECL	10	12
	BLANK	Video BLANK Input	ECL	11	13
	BRT	Video BRighT Input	ECL	12	14
	SYNC	Video SYNC Input	ECL	13	15
Data Inputs	D_1	Data Bit 1 (MSB)	ECL	21	25
	D_2		ECL	22	26
	D_3		ECL	23	27
	D_4		ECL	24	28
	D_5		ECL	1	1
	D_6		ECL	2	2
	D_7		ECL	3	3
	D_8	Data Bit 8 (LSB)	ECL	4	4
Convert	CONV	CONVert Clock Input	ECL	6	7
	$\overline{CONV}$	CONVert Clock Input, Complement	ECL	7	8
Analog Outputs	OUT−	Output Current −	Current Sink	18	21
	OUT+	Output Current +	Current Sink	19	22

Figure 1. Timing Diagram

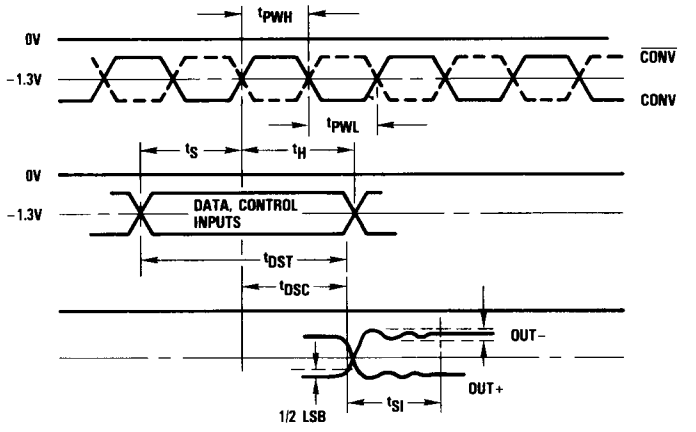


Figure 2. CONVert, CONVert Switching Levels

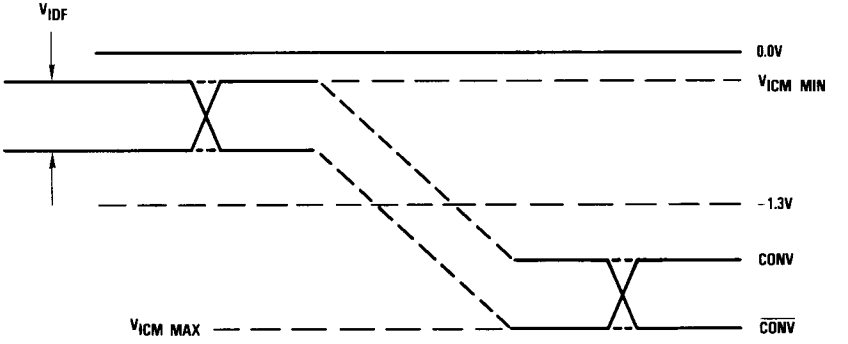


Figure 3. Equivalent Input Circuits

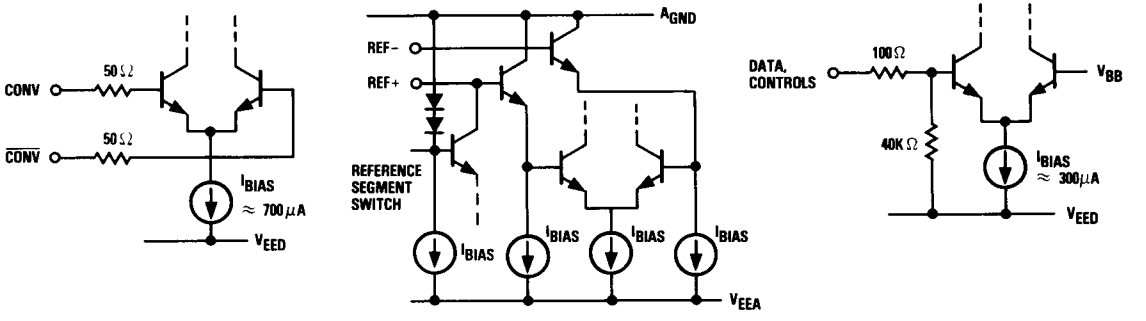


Figure 4. Equivalent Output Circuit

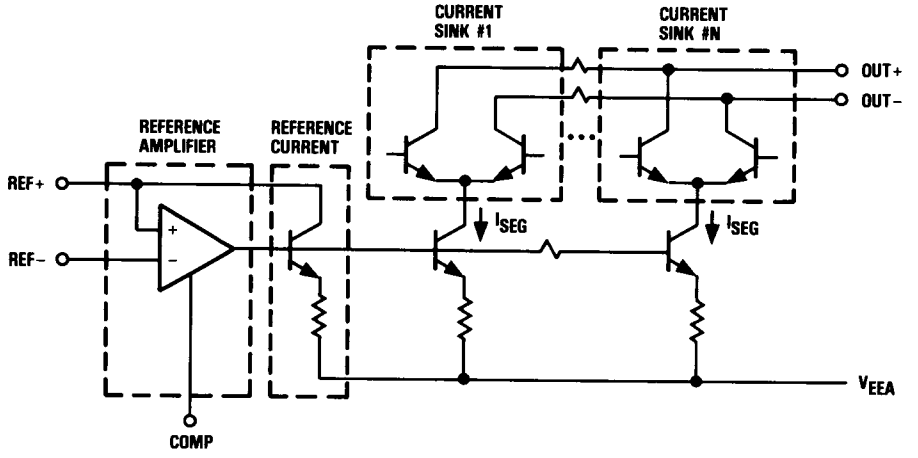
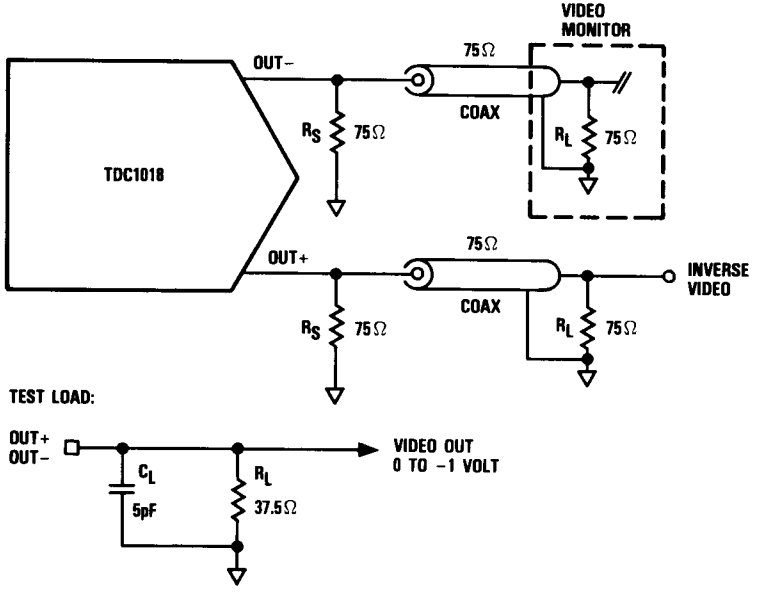


Figure 5. Standard Load Configuration



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltages

V_{EED} (measured to D_{GND})	−7.0 to 0.5V
V_{EEA} (measured to A_{GND})	−7.0 to 0.5V
A_{GND} (measured to D_{GND})	−0.5 to 0.5V

Input Voltages

CONV, Data, and Controls (measured to D_{GND})	V_{EED} to 0.5V
Reference input, applied voltage (measured to A_{GND})[2]	
REF+	V_{EEA} to 0.5V
REF−	V_{EEA} to 0.5V
Reference input, applied current, externally forced[3,4]	
REF+	6.0mA
REF−	0.5mA

Output

Analog output, applied voltage (measured to A_{GND})	
OUT+	−2.0 to +2.0V
OUT−	−2.0 to +2.0V
Analog output, applied current, externally forced[3,4]	
OUT+	50mA
OUT−	50mA
Short circuit duration	Unlimited sec

Temperature

Operating, ambient	−60 to +140°C
junction	+175°C
Lead, soldering (10 seconds)	+300°C
Storage	−60 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current when flowing into the device.

Operating conditions

Parameter			Temperature Range Standard Min	Nom	Max	Units
V_{EED}	Digital Supply Voltage (measured to D_{GND})		-4.9	-5.2	-5.5	V
V_{EEA}	Analog Supply Voltage (measured to A_{GND})		-4.9	-5.2	-5.5	V
V_{AGND}	Analog Ground Voltage (measured to D_{GND})		-0.1	0.0	+0.1	V
$V_{EEA}-V_{EED}$	Supply Voltage Differential		-0.1	0.0	+0.1	V
V_{ICM}	CONV Input Voltage, Common Mode Range (Figure 2)		-0.5		-2.5	V
V_{IDF}	CONV Input Voltage, Differential (Figure 2)		0.4		1.2	V
t_{PWL}	CONV Pulse Width, LOW		4			ns
t_{PWH}	CONV Pulse Width, HIGH		4			ns
t_S	Setup Time, Data and Controls		3.5			ns
t_H	Hold Time, Data and Controls		0			ns
V_{IL}	Input Voltage, Logic LOW				-1.49	V
V_{IH}	Input Voltage, Logic HIGH		-1.045			V
I_{REF}	Reference Current	Video standard output levels[1]	1.059	1.115	1.171	mA
		8-bit linearity	1.0		1.3	mA
C_C	Compensation Capacitor		2000	3900		pF
T_A	Ambient Temperature, Still Air		0		70	°C

Note:

1. Minimum and Maximum values allowed by ±5% variation given in RS343A and RS170 after initial gain correction of device.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Standard Min	Max	Units
$I_{EEA}+I_{EED}$	Supply Current	$V_{EEA} = V_{EED}$ = MAX, static[1]			
		T_A = 0°C to 70°C		170	mA
		T_A = 70°C		130	mA
C_{REF}	Equivalent Input Capacitance, REF+, REF-			5	pF
C_I	Input Capacitance, Data and Controls			5	pF
V_{OCP}	Compliance Voltage, + Output		-1.2	+1.5	V
V_{OCN}	Compliance Voltage, - Output		-1.2	+1.5	V
R_O	Equivalent Output Resistance		20		KOhms
C_O	Equivalent Output Capacitance			20	pF
I_{OP}	Max Current, + Output	V_{EEA} = NOM, SYNC = BLANK = 0, FH = BRT = 1		30	mA
I_{ON}	Max Current, - Output	V_{EEA} = NOM, SYNC = 1		30	mA
I_{IL}	Input Current, Logic LOW, Data and Controls	V_{EED} = MAX, V_I = -1.49V		200	μA
I_{IH}	Input Current, Logic HIGH, Data and Controls	V_{EED} = MAX, V_I = -1.045V		200	μA
I_{IC}	Input Current, Convert	V_{EED} = MAX, $-1.49V < V_I < -1.045V$		50	μA

Note:

1. Worst case over all data and control states.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
F_S	Maximum Data Rate	V_{EEA}, V_{EED} = MIN			
		TDC1018	125		MSPS
		TDC1018-1	200		MSPS
t_{DSC}	Clock to Output Delay, Clocked Mode	V_{EEA}, V_{EED} = MIN, FT = 0		8	ns
t_{DST}	Data to Output Delay, Transparent Mode	V_{EEA}, V_{EED} = MIN, FT = 1		13	ns
t_{SI}	Current Settling Time, Clocked Mode	V_{EEA}, V_{EED} = MIN, FT = 0			
		0.2%		10	ns
		0.8%		8	ns
		3.2%		5	ns
t_{RI}	Risetime, Current	10% to 90% of Gray Scale		1.7	ns

B

System performance characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Standard Min	Temperature Range Standard Max	Units
E_{LI}	Linearity Error Integral, Terminal Based	V_{EEA}, V_{EED}, I_{REF} = NOM		0.2	% of Gray Scale
E_{LD}	Linearity Error Differential	V_{EEA}, V_{EED}, I_{REF} = NOM		0.2	% of Gray Scale
I_{OF}	Output Offset Current	V_{EEA}, V_{EED} = MAX, SYNC = BLANK = 0, FH = BRT = 1		10	μA
E_G	Absolute Gain Error	V_{EEA}, V_{EED} = MIN, I_{REF} = NOM		±5	% of Gray Scale
TC_G	Gain Error Tempco			±0.024	% of Gray Scale/°C
BWR	Reference Bandwidth, -3dB	C_C = MIN, ΔV_{REF} = 1mV p-p	1		MHz
DP	Differential Phase	4 x NTSC		1.0	Degrees
DG	Differential Gain	4 x NTSC		2.0	%
PSRR	Power Supply Rejection Ratio	V_{EEA}, V_{EED}, I_{REF} = NOM[1]		45	dB
		V_{EEA}, V_{EED}, I_{REF} = NOM[2]		55	dB
PSS	Power Supply Sensitivity	V_{EEA}, V_{EED}, I_{REF} = NOM		120	μA/V
G_C	Peak Glitch Charge	Registered Mode[3,4]		800	fCoulomb
G_I	Peak Glitch Current	Registered Mode		1.2	mA
G_E	Peak Glitch "Energy" (Area)	Registered Mode[4]		30	pV-Sec
FT_C	Feedthrough Clock	Data = Constant[5]		-50	dB
FT_D	Feedthrough Data	Clock = Constant[5]		-50	dB

Notes:

1. 20KHz, ±0.3V ripple superimposed on V_{EEA}, V_{EED}; dB relative to full gray scale.
2. 60Hz, ±0.3V ripple superimposed on V_{EEA}, V_{EED}; dB relative to full gray scale.
3. fCoulombs = microamps x nanoseconds
4. 37.5Ω load. Because glitches tend to be symmetric, average glitch area approaches zero.
5. dB relative to full gray scale, 250MHz bandwidth limit.

Table 1 Video Control Truth Table

Sync	Blank	Force High	Bright	Data Input	Out− (mA)[1]	Out− (V)[2]	Out− (IRE)[3]	Description[4]
1	X	X	X	X	28.57	−1.071	−40	Sync Level
0	1	X	X	X	20.83	−0.781	0	Blank Level
0	0	1	1	X	0.00	0.00	110	Enhanced High Level
0	0	1	0	X	1.95	−0.073	100	Normal High Level
0	0	0	0	000...	19.40	−0.728	7.5	Normal Low Level
0	0	0	0	111...	1.95	−0.073	100	Normal High Level
0	0	0	1	000...	17.44	−0.654	17.5	Enhanced Low Level
0	0	0	1	111...	0.00	0.00	110	Enhanced High Level

Notes:

1. Out+ is complementary to Out−. Current is specified as conventional current when flowing into the device.
2. Voltage produced when driving the standard load configuration (37.5 Ohms). See Figure 5.
3. 140 IRE units = 1.00V.
4. RS-343-A tolerance on all control values is assumed.

Figure 6. Video Output Waveforms for Out− and Out+ with Standard Load Configuration

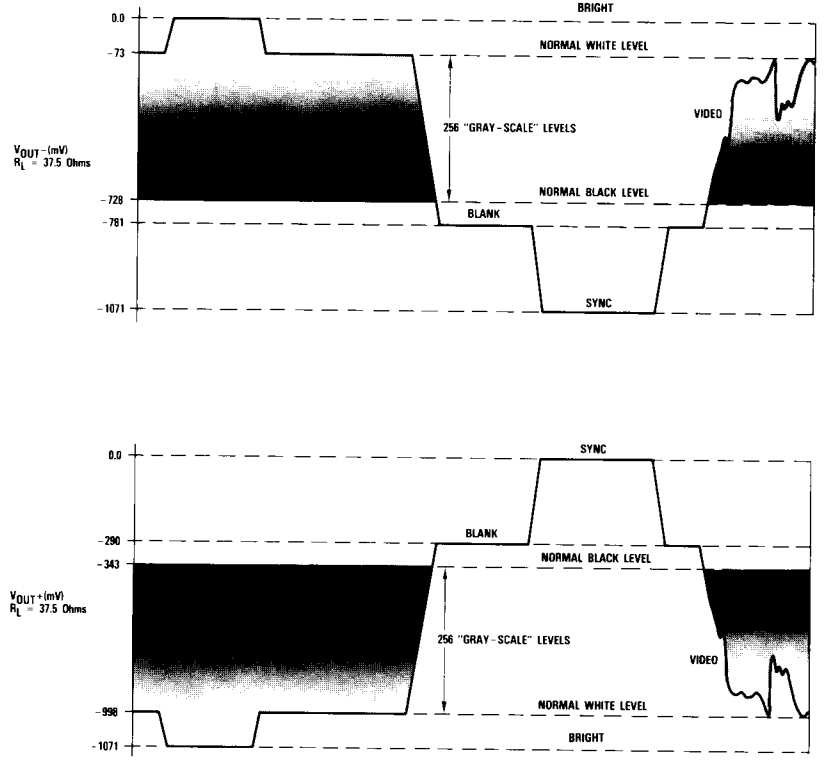
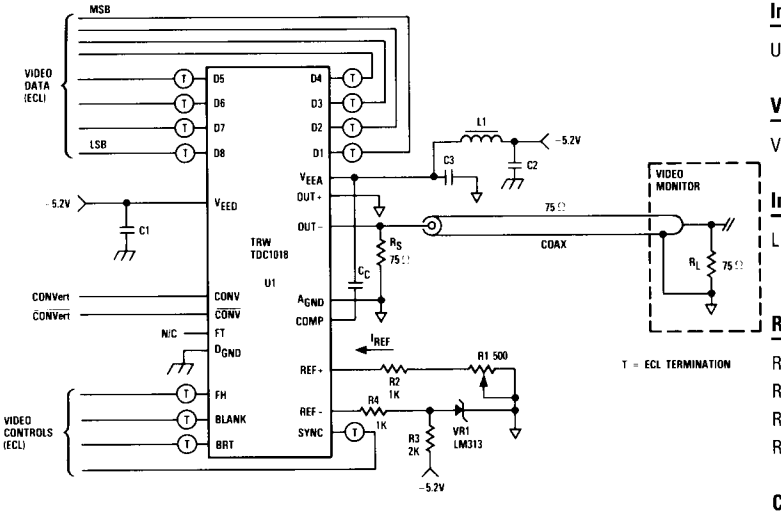


Figure 7. Typical Interface Circuit



Parts List

Integrated Circuits

U1 TDC1018 D/A Converter

Voltage References

VR1 LM113 or LM313 Bandgap Reference

Inductors

L1 Ferrite Bead Shield Inductor
Fair-Rite P/N 2743001112 or Similar

Resistors

R1	1KΩ	Pot	10 Turn
R2	1.00KΩ	1/8W	1% Metal Film
R3	2.00KΩ	1/8W	1% Metal Film
R4	1.00KΩ	1/8W	1% Metal Film

Capacitors

C1 – C3	0.1μF	50V	Ceramic Disc
C_C	0.01μF	50V	Ceramic Disc

B

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1018B7C	STD – T_A = 0°C to 70°C	Commercial	24 Pin CERDIP	1018B7C
TDC1018B7C1	STD – T_A = 0°C to 70°C	Commercial	24 Pin CERDIP	1018B7C1
TDC1018C3C	STD – T_A = 0°C to 70°C	Commercial	28 Contact Chip Carrier	1018C3C
TDC1018C3C1	STD – T_A = 0°C to 70°C	Commercial	28 Contact Chip Carrier	1018C3C1