PRELIMINARY

TS 83510

BIPOLAR HIGH SPEED 10-BIT A/D CONVERTER

DESCRIPTION

The TS 83510 is a monolithic sampling 10-bit A/D converter, designed for applications requiring high speed conversion, while maintaining low power requirements.

Combining on-board track-and-hold amplifier, internal reference and innovative subranging architecture on a high speed bipolar technology, the TS 83510 can sample up to 60 MHz and achieves 8.3 effective numbers of bits at F_S = 50MHz and F_{in} = 10 MHz.

Digital inputs and outputs are TTL compatible. The analog input requires a signal of 2 V p-p amplitude. The TS 83510 is specified to operate from commercial to military temperature ranges with analog input frequency up to 20 MHz, making it ideal for a wide range of applications and environments.

This product is packaged in hermetic ceramic 28-pin Ceramic DIL, plastic SOIC 28, PDIP 28 and dual ceramic flat pack 28.

MAIN FEATURES

- Up to 60 MHz conversion speed.
- SINAD = 52 dB at F_S = 50 MHz, F_{in} = 10 MHz.
- Low power : 1.1 W.
- Internal reference.
- On-board T/H amplifier.
- 2 V p-p analog input.
- Digital input and outputs TTL compatible.
- Pin compatible with AD 9040A.
- Similar to AD 9020/9060.
- Evaluation board TSEV 83510J available.
- NRZ circuit (see TS 83510 digital coding).

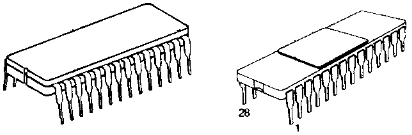
APPLICATIONS

- Medical imaging.
- Digital oscilloscopes.
- Image processing.
- Communications.
- Advanced television.
- High energy physics.
- Military systems.
- Radar pulse analysis.

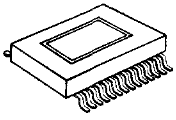
PACKAGING INFORMATION

The TS 83510 will be available in three versions (Mil. Temp. : −55°C to +125°C : M suffix ; Ind. Temp. : −40°C to +85°C : V suffix ; Commercial Temp. : 0°C to +70°C : C suffix) :

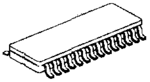
- 28-pin Ceramic DIL,
- 28-pin Ceramic dual flat pack (upon request).
- 28-pin plastic SOIC (to be introduced), for commercial temperature range only.
- 28-pin plastic DIP, for commercial temperature range only (to be introduced).



P, J or C suffix
DIL 28
PDIP, Cerdip or Side brazed packages



Z suffix
DFP 28
Dual Ceramic flat pack



S suffix
Plastic SOIC 28

ABSOLUTE MAXIMUM RATINGS (see Note)

Parameter		Symbol	Comments	Value	Unit
Positive supply voltage		AV_{CC}, DV_{CC}		0 to 6	V
Negative supply voltage		V_{EE}		− 6 to 0	V
Analog input voltage		V_{IN}		V_{EE} to V_{CC}	V
Reference input voltage		V_{REF}		0 to V_{CC}	V
Clock input voltage		CLK		0 to V_{CC}	V
Maximum difference between positive supplies		DV_{CC} to AV_{CC}		0.5	V
Digital output current		I_D		20	mA
Junction temperature	Plastic package	T_j		+ 150	°C
	Ceramic package			+ 175	
Storage temperature		T_{stg}		− 65 to + 150	°C
Operating temperature range		T_{case}	Civil : «C» grade Industrial : «V» grade Military : «M» grade	0 to 70 − 40 to + 85 − 55 to + 125	°C °C °C
Lead temperature (soldering 10 s)		T_{leads}		+ 260	°C

Note : Absolute maximum ratings are limiting values applied individually while other parameters are within specified operating conditions.
Long exposure to maximum rating may affect device reliability.

USER WARNING

The power supplies must be applied before all the other signals to prevent damage from occuring on the device.

RECOMMENDED CONDITIONS OF USE

Parameter	Symbol	Comments	Min.	Typ.	Max.	Unit
Positive supply voltage	AV_{CC}, DV_{CC}			5		V
Negative supply voltage	V_{EE}			− 5.2		V
Reference input voltage	V_{REF}	Available from V_{OUT}		2.5		V
Analog input voltage	V_{IN}			± 1		V
Clock input voltage	CLK		TTL levels			
Load		Single LS latch		6	10	pF
Decoupling		All power supplies and V_{REF} must be decoupled with external 100 nF chip capacitors.				
Operating temperature range	T_{case}	Civil : «C» grade Industrial : «V» grade Military : «M» grade	0 to 70 − 40 to + 85 − 55 to + 125			°C °C °C

SPECIFICATIONS

Electrical operating characteristics

$V_{EE} = -5.2\ V$; $DV_{CC} = AV_{CC} = 5\ V$; $T_C = 25°C$ (unless otherwise specified)

Parameter	T_{case}	Test level	Min.	Typ.	Max.	Unit
RESOLUTION				10		Bits
DIGITAL INPUTS AND OUTPUTS						
Logic compatibility				TTL		
Clock inputs						
• Logic «0» voltage	full	IV	0		0.8	V
• Logic «1» voltage	full	IV	2		5	V
Output data						
• Logic «0» voltage (Note 1)	full	II,D	0		0.5	V
• Logic «1» voltage (Note 1)	full	II, D	2.4		5	V
MAXIMUM CLOCK FREQUENCY		III	50	60		MHz
MINIMUM CLOCK FREQUENCY		III		0.5	1	MHz
ANALOG INPUT						
Voltage range	full	V		± 1		V
Input capacitance		IV		15	20	pF
Input bias current		I, D		10	20	μA
Input resistance		I, D	500	2000		kΩ
Analog bandwidth (Note 2)		V		100		MHz
REFERENCE VOLTAGE						
Internal band-gap reference voltage (V_{OUT})	full	I, D	2.4	2.5	2.6	V
Temperature coefficient	full	IV		100		ppm/°C
Input reference voltage (V_{REF})	full	IV	2.4	2.5	2.6	V
POWER REQUIREMENTS						
Positive supply voltage		I, D	4.5	5	5.5	V
	full	II	4.5	5	5.5	V
Positive supply current		I, D		165	TBD	mA
	full	II		190	TBD	mA
Negative supply voltage		I, D	−5.7	−5.2	−4.7	V
	full	II	−5.7	−5.2	−4.7	V
Negative supply current		I, D		60	TBD	mA
	full	II		70	TBD	mA
Nominal power dissipation		V		1.1	1.3	W
ACCURACY						
Integral nonlinearity (Notes 2 and 3)		I		1.4	2	LSB
	full	II		2	2.5	LSB
Differential nonlinearity (Notes 2 and 3)		I		0.5	0.9	LSB
	full	II		0.7	1.25	LSB
Monotonicity and no missing codes	full	II	Guaranteed over specified temperature range			

SPECIFICATIONS (Continued)

Electrical operating characteristics

$V_{EE} = -5.2$ V ; $DV_{CC} = AV_{CC} = 5$ V ; $T_C = 25°C$ (unless otherwise specified)

Parameter	T_{case}	Test level	Min.	Typ.	Max.	Unit
DYNAMIC CHARACTERISTICS (Note 4)						
Signal to Noise Ratio (SNR) (Note 2)						
F_S = 40 MHz F_{in} = 2.3 MHz		I	TBD	55		dB
F_S = 40 MHz F_{in} = 10.3 MHz		I	TBD	54		dB
F_S = 40 MHz F_{in} = 20 MHz		IV	TBD	51		dB
F_S = 50 MHz F_{in} = 2.3 MHz		I	TBD	54		dB
F_S = 50 MHz F_{in} = 10.3 MHz		I	TBD	53		dB
F_S = 50 MHz F_{in} = 20 MHz		IV	TBD	50		dB
Total Harmonic Distorsion (THD) (Note 2)						
F_S = 40 MHz F_{in} = 2.3 MHz		I	TBD	62		dBc
F_S = 40 MHz F_{in} = 10.3 MHz		I	TBD	59		dBc
F_S = 40 MHz F_{in} = 20 MHz		IV	TBD	49		dBc
F_S = 50 MHz F_{in} = 2.3 MHz		I	TBD	62		dBc
F_S = 50 MHz F_{in} = 10.3 MHz		I	TBD	59		dBc
F_S = 50 MHz F_{in} = 20 MHz		IV	TBD	49		dBc
Signal to Noise And Distortion ratio (SINAD) (Note 2)						
F_S = 40 MHz F_{in} = 2.3 MHz		I	TBD	54		dB
F_S = 40 MHz F_{in} = 10.3 MHz		I	TBD	53		dB
F_S = 40 MHz F_{in} = 20 MHz		IV	TBD	47		dB
F_S = 50 MHz F_{in} = 2.3 MHz		I	TBD	53		dB
F_S = 50 MHz F_{in} = 10.3 MHz		I	TBD	52		dB
F_S = 50 MHz F_{in} = 20 MHz		IV	TBD	46		dB
Effective Number Of Bits (ENOB)						
F_S = 40 MHz F_{in} = 2.3 MHz		I	TBD	8.7		Bits
F_S = 40 MHz F_{in} = 10.3 MHz		I	TBD	8.5		Bits
F_S = 40 MHz F_{in} = 20 MHz		IV	TBD	7.5		Bits
F_S = 50 MHz F_{in} = 2.3 MHz		I	TBD	8.6		Bits
F_S = 50 MHz F_{in} = 10.3 MHz		I	TBD	8.3		Bits
F_S = 50 MHz F_{in} = 20 MHz		IV	TBD	7.4		Bits

Note 1 : With $I_{OL} = -0.4$ mA and $I_{OH} = 20\ \mu A$.

Note 2 : See definition of terms.

Note 3 : Histogram based on sampling of 1 MHz sinusoïdal analog signal with an encode rate of 5 MHz.

Note 4 : For dynamic performance, duty cycle of encode command should be 50 % ± 10 %.
For frequencies above 35 MHz, prefere duty cycle of 60 % (high level of the clock).

EXPLANATION OF TEST LEVELS

Test level	
I	100 % production tested at +25°C.
II	100 % production tested at +25°C, and sample tested at specified temperatures (AC testing done on sample basic).
III	Sample tested only.
IV	Parameter is guaranteed by design and characterization testing.
V	Parameter is a typical value only.
VI	All devices are 100 % production tested at +25°C. 100 % production tested at temperature extremes for military temperature devices, guaranteed by design and and characterization testing for (civil) and industrial devices.
D	100 % probe tested on wafer at T_{amb} = +25°C.

THERMAL CHARACTERISTICS

Package	Parameter	Symbol	Typ.	Unit
DIL 28	Thermal resistance - Ceramic junction to ambient Thermal resistance - Ceramic junction to case	θ JA θ JC	42 10	°C/W °C/W
PDIP 28	Thermal resistance - Plastic junction to ambient Thermal resistance - Plastic junction to case	θ JA θ JC	52 10	°C/W °C/W
DFP 28	Thermal resistance - Ceramic junction to ambient Thermal resistance - Ceramic junction to case	θ JA θ JC	56 13	°C/W °C/W
SOIC 28	Thermal resistance - Plastic junction to ambient Thermal resistance - Plastic junction to case	θ JA θ JC	57 10	°C/W °C/W

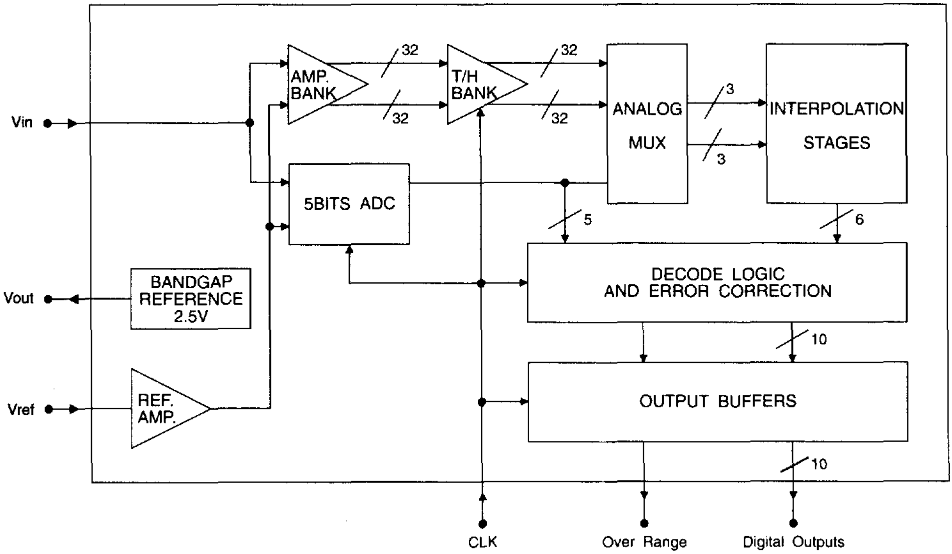


Figure 1 : TS 83510 block diagram.

FUNCTIONAL DESCRIPTION

The TS 83510 utilizes an innovative subranging architecture* (see figure 1 : TS 83510 block diagram).

It is based on analog parallel subrange selection and serial interpolation.

The analog input is applied to a 5 bit flash ADC which provides the coarse quantization.

Simultaneously, this input is compared with the 32 ladder references through a bank of amplifiers which provide 32 residue signals.

These analog residues are held by 32 T/Hs on the rising edge of the clock command.

Three of these high precision residue voltages are then selected through analog multiplexers, which are activated by the output of the 5 bit ADC.

These selected residue signals are then fed into serial interpolation cells to perform the fine quantization (5 + 1 overlapping bits).

At last, Decode logic and Error correction blocks combine coarse and fine datas to give the final 10 bit digital word.

* Patent pending.

SWITCHING PERFORMANCES (Note 1) - see Figure 2

Parameter	Symbol	Typ.	Unit
Minimum Clock pulse width (high) (Note 2)	TC1	8.5	ns
Minimum Clock pulse width (low) (Note 2)	TC2	8.5	ns
Aperture delay (Note 3)	TA	TBD	ns
Aperture uncertainty (Note 3)	Jitter	10	ps_{rms}
Output delay (Notes 3 and 4)	TOD	14	ns
Output rise time (Note 4)		8	ns
Output fall time (Note 4)		8	ns

Note 1 : $V_{EE} = -5.2$ V ; $AV_{CC} = DV_{CC} = 5$ V ; $T_C = 25$°C.

Note 2 : For dynamic performance, duty cycle of encode command should be 50 % ± 10 %.
For frequencies above 35 MHz, prefere duty cycle of 60 % (high level of the clock).

Note 3 : See definitions of terms.

Note 4 : Outputs connected to a single LS latch. $C_{load} < 10$ pF.

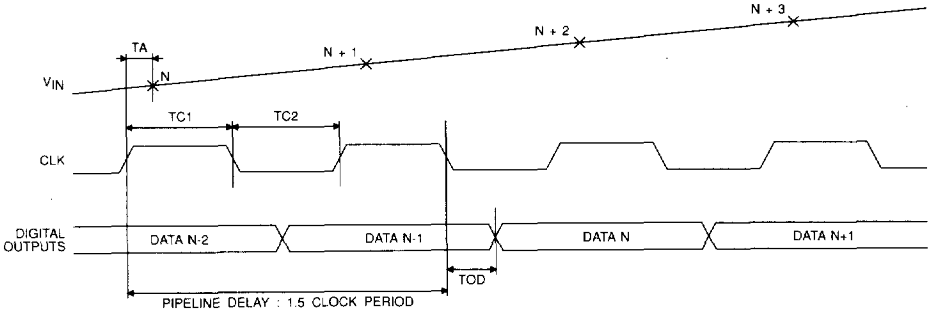
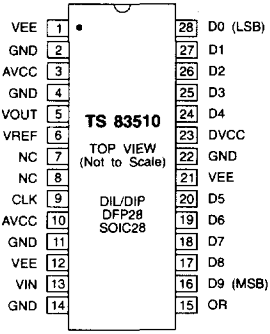


Figure 2 : TS 83510 timing diagram.

PIN DESCRIPTION

Pin	Name	Function
1, 12, 21	V_{EE}	−5.2 V power supply.
2, 4, 11, 14 22	GND	Ground.
3, 10	VCC	Analog +5 V power supply.
5	V_{OUT}	Internal bandgap voltage reference (nominally +2.5 V).
6	V_{REF}	Non-inverting input to reference amplifier. ADC voltage reference is connected here.
7	NC	No connection internally (connected to external 0.1 µF by pass capacitor on AD 9040 serie).
8	NC	No connection internally.
9	CLK	TTL encode clock input to ADC. Internal T/H is placed in hold hold mode (ADC is encoding) on rising edge of encode signal.
13	V_{IN}	Analog input.
15	OR	Over range condition output. Active high when analog input exceeds input range of ADC (< −FS, > +FS) - NRZ mode.
16	D9 (MSB)	Most significant bit ; TTL output.
17 - 20	D8 - D5	Digital TTL output bits.
23	D_{VCC}	Digital +5 V power supply.
24 - 27	D4 - D1	Digital TTL output bits.
28	D0 (LSB)	Least significant bit ; TTL output.



DEFINITION OF TERMS

Analog bandwidth

The analog input frequency at which the fundamental component in the reconstructed output has fallen by 3 dB with respect to its low frequency value (determined by FFT analysis).

Differential non linearity (DNL)

The differential non linearity for an output code i is the difference between the measured step size of code i and the ideal LSB step size. DNL (i) is expressed in LSBs. DNL is the maximum value of all |DNL (i)|. DNL error specification of less than 1 LSB guarantees that there are no missing output codes, and that the transfer function is monotonic.

Integral non linearity (INL)

The integral non linearity for an output code i is the difference between the measured input voltage at which the transition occurs and the ideal value of this transition. INL (i) is expressed in LSBs, and is the maximum value of all |INL (i)|.

Signal to noise ratio (SNR)

The ratio of the RMS signal amplitude to the RMS sum of all other spectral components, without harmonics.

Total harmonic distortion (THD)

The ratio of the most significant harmonic components in the spectrum of the quantized representation, to the fundamental spectral component.

Signal to noise and distortion ratio (SINAD)

The ratio of the RMS signal amplitude to the RMS sum of all other spectral components, including the most significant harmonics except DC.

Aperture delay (TA)

The delay between the rising edge of CLK signal and the time at which V_{IN} is sampled.

Aperture uncertainty (JITTER)

The sample to sample variation in aperture delay. The voltage error due to jitter depends on the slew rate of the signal at the sampling point.

Output delay (TOD)

The delay from the falling edge of CLK (50 % point) to the $V_{OH} = 2$ V or $V_{OL} = 0.8$ V of the digital outputs with 10 pF maximum load.

Non return to zero (NRZ)

If V_{IN} exeeds positive full scale (+ 1 V), output data remain at high level (Non Return to Zero).

DIGITAL CODING - NZR mode (see definition of terms)

Analog input	Voltage level	Over range	Digital output
+ 1.002 V	Positive full scale + 1 LSB	1	MSB ... LSB 1111111111
+ 1 V	Positive full scale	0	1111111111
	Full scale – 1 LSB	0	1111111110
+ 1/2 V	Positive 1/2 scale	0	1100000000
	1/2 scale – 1 LSB	0	1011111111
0 V	Bipolar zero (offset zero)	0	1000000000
		0	0111111111
– 1/2 V	1/2 scale + 1 LSB	0	0100000000
	Negative 1/2 scale	0	0011111111
– 1 V	Full scale + 1 LSB	0	0000000001
	Negative full scale	0	0000000000
– 1.002 V	Negative full scale – 1 LSB	1	0000000000

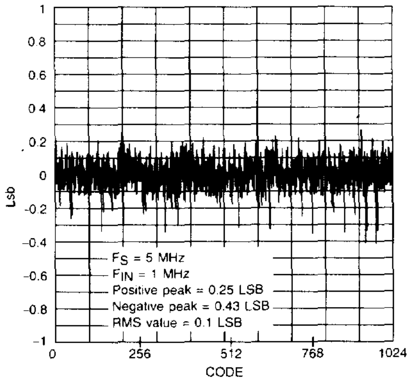


Figure 3 : Differential non linearity.

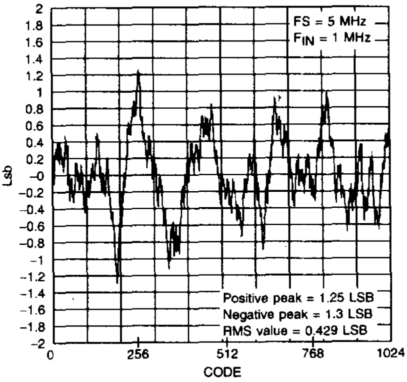


Figure 4 : Integral non linearity.

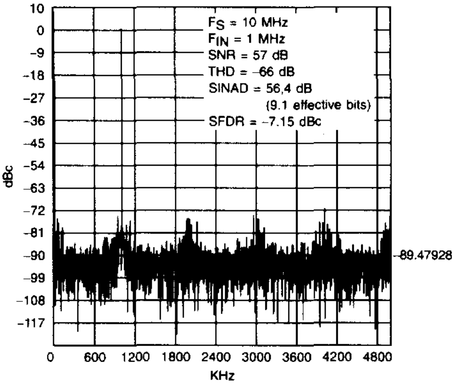


Figure 5 : FFT @ 10 MHz / 1 MHz.

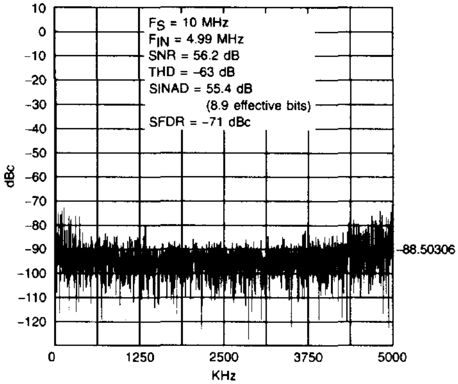


Figure 6 : FFT @ 10 MHz / 4.99 MHz.

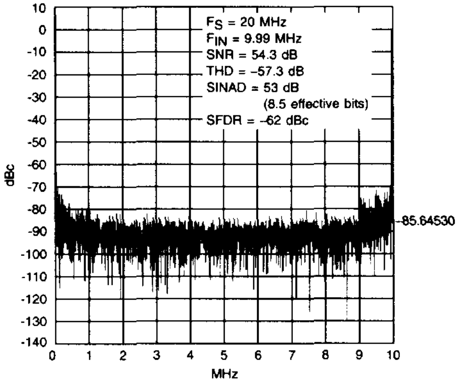


Figure 7 : FFT @ 20 MHz / 9,99 MHz.

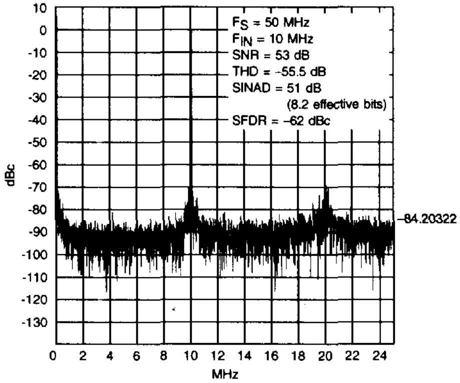


Figure 8 : FFT @ 50 MHz / 10 MHz.

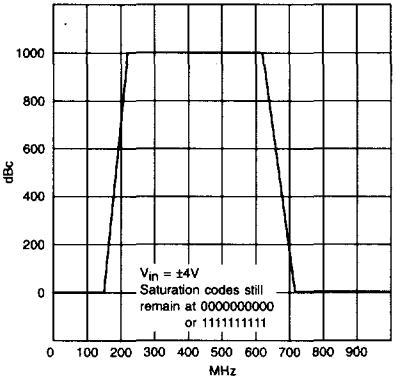


Figure 9 : High level input signal (± 4 V).

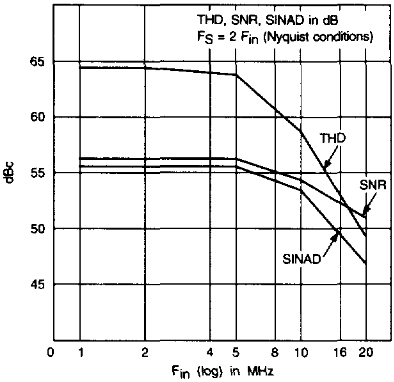


Figure 10 : FFT at Nyquist conditions.

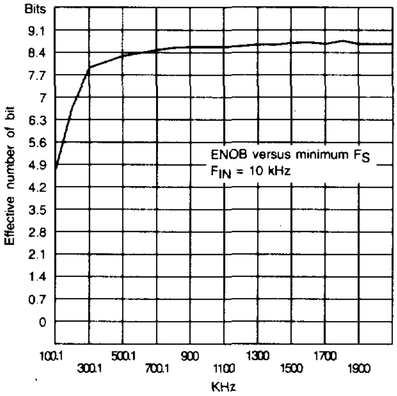


Figure 11 : Effective Number of bit @ F_{IN} = 10 kHz.

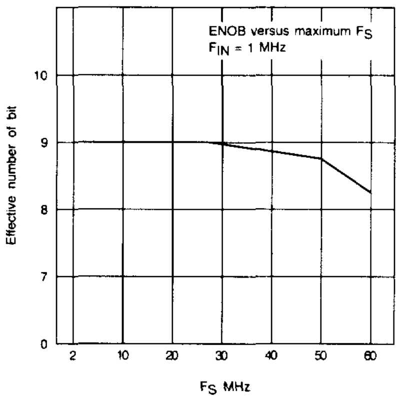
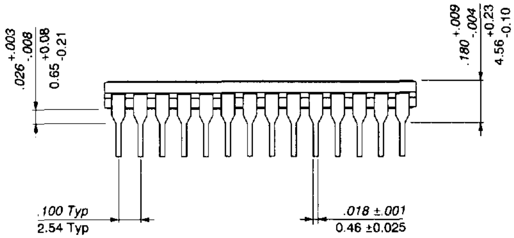
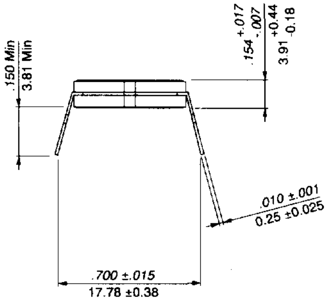


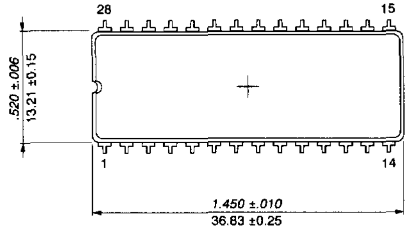
Figure 12 : Effective number of bit @ F_{IN} = 1 MHz.

OUTLINE DIMENSIONS

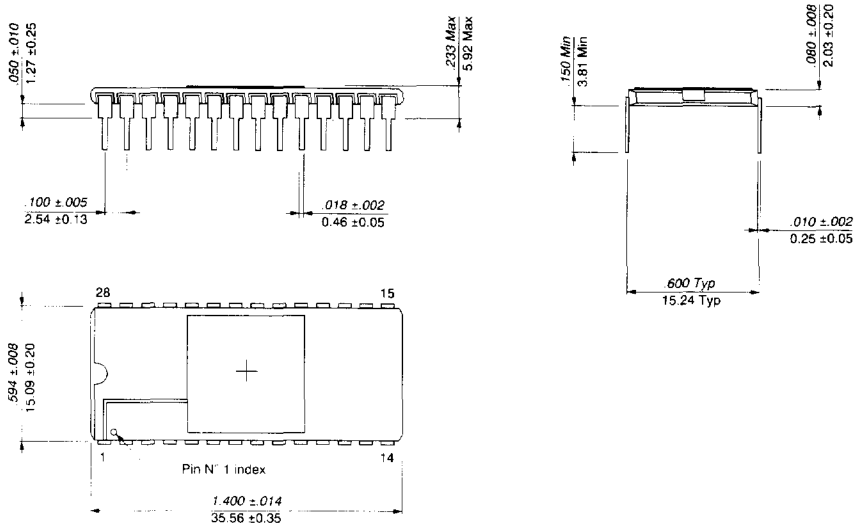
DIL 28 - Cerdip package (J suffix) (Dimensions in inches and mm)



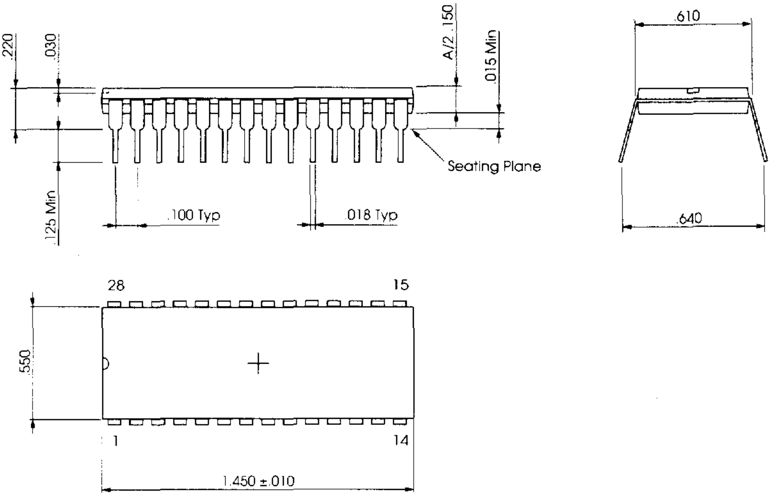




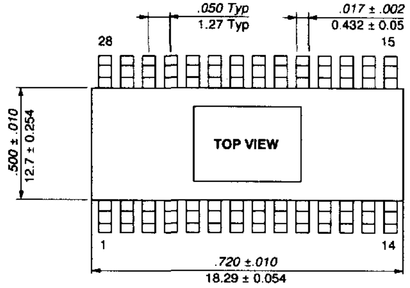
DIL 28 - Ceramic package (C suffix) (Dimensions in inches and mm)

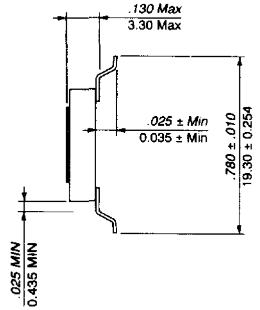


PDIP 28 - Plastic package (P suffix) (Dimensions in inches)

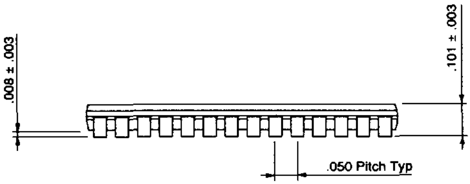


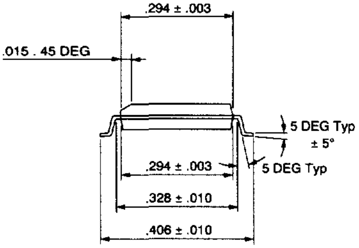
DFP 28 - Dual Ceramic flat pack (Z suffix) (Dimensions in inches and mm)

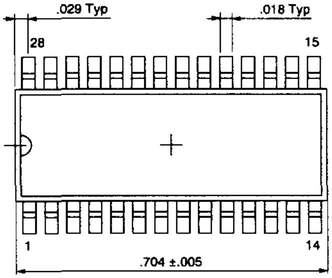




SOIC 28 - Plastic package (S suffix) (Dimensions in inches)







DIE MECHANICAL INFORMATION : JTS 83510

Pad layout : VB22C

Die size : 3.090 × 4.760 mm

Pad size : 0.120 × 0.120 mm

Die thickness : 380 μm

Metallization : Al-Ni-Au (Back side)
Al-Si-Ti (Front side)

Passivation : Nitride

Revision : A

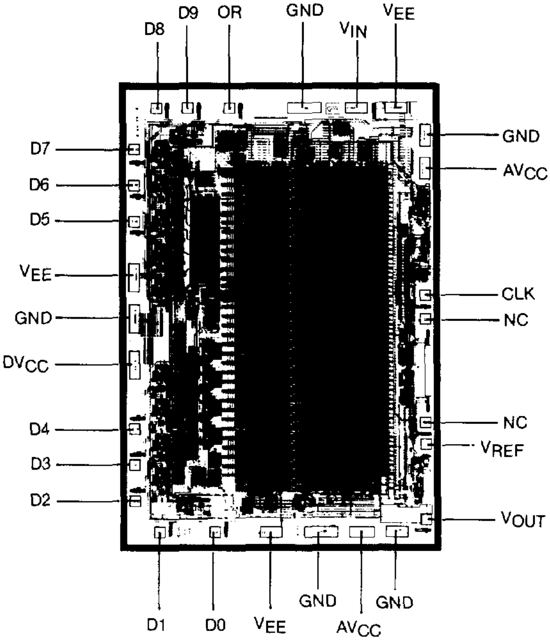
Qualification lot package : DIL 28

Back side potential : V_{EE}

Transistor count : 7530

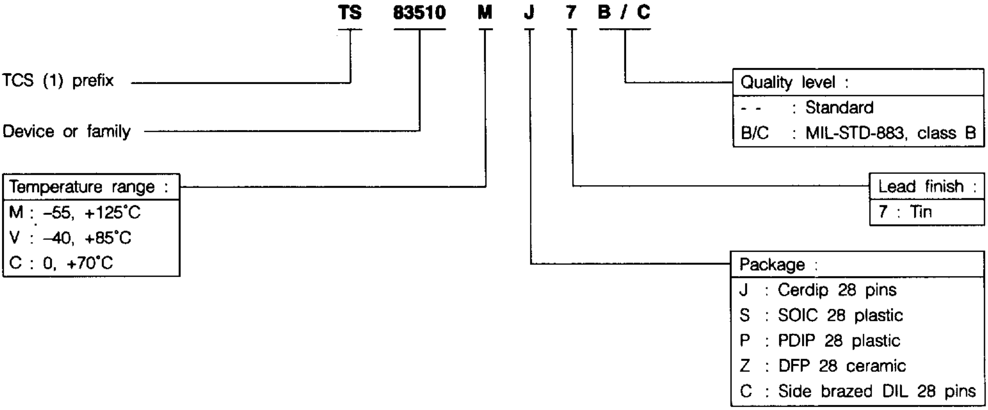
Die attach : eutectic Al-Ni-Au

Bond wire : Al



ORDERING INFORMATION

Package device



TS 83510 M J 7 B / C

TCS (1) prefix

Device or family

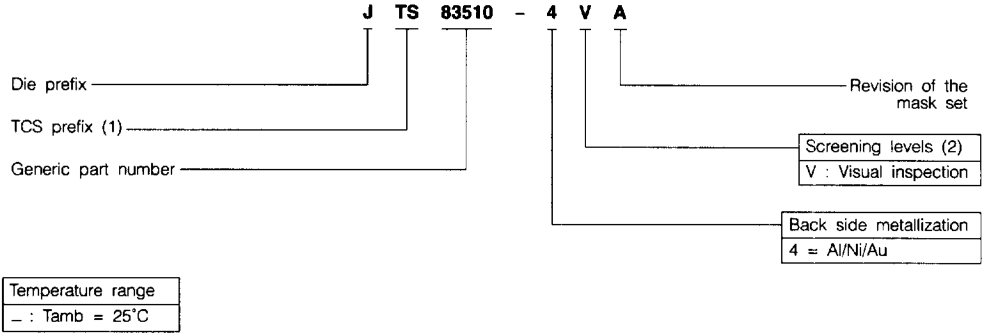
Temperature range :
M : –55, +125°C
V : –40, +85°C
C : 0, +70°C

Quality level :
- - : Standard
B/C : MIL-STD-883, class B

Lead finish :
7 : Tin

Package :
J : Cerdip 28 pins
S : SOIC 28 plastic
P : PDIP 28 plastic
Z : DFP 28 ceramic
C : Side brazed DIL 28 pins

Die form



J TS 83510 – 4 V A

Die prefix

TCS prefix (1)

Generic part number

Revision of the mask set

Screening levels (2)
V : Visual inspection

Back side metallization
4 = Al/Ni/Au

Temperature range
_ : Tamb = 25°C

Note 1 : THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES.

Note 2 : For availability of the different available versions contact your TCS sale office.