



Integrated Device Technology, Inc.

128K x 8 3.3V SYNCHRONOUS SRAM WITH ZBT™ AND FLOW-THROUGH OUTPUT

ADVANCE INFORMATION IDT71V509

FEATURES:

- 128K x 8 memory configuration
- High speed - 66 MHz (9 ns Clock-to-Data Access)
- Flow-Through Output
- No dead cycles between Write and Read Cycles
- Low power deselect mode
- Single 3.3V power supply ($\pm 5\%$)
- Packaged in 44-lead SOJ

DESCRIPTION:

The IDT71V509 is a 3.3V high-speed 1,024,576-bit synchronous SRAM organized as 128K x 8. It is designed to eliminate dead cycles when turning the bus around between reads and writes, or writes and reads. Thus, it has been given the name ZBT™, or Zero Bus Turnaround™.

Addresses and control signals are applied to the SRAM

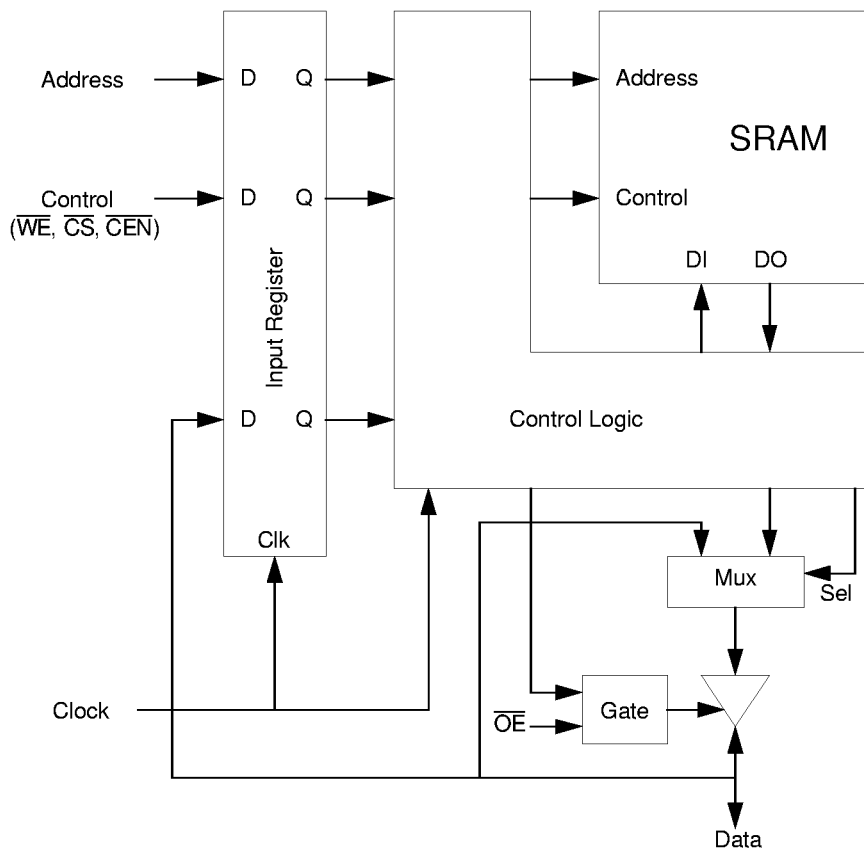
during one clock cycle, and one clock cycle later its associated data cycle occurs, be it read or write.

The IDT71V509 contains data, address, and control signal registers. Output Enable is the only asynchronous signal, and can be used to disable the output at any time.

A Clock Enable (\overline{CEN}) pin allows operation of the IDT71V509 to be suspended as long as necessary. All synchronous inputs are ignored when \overline{CEN} is high. A Chip Select (\overline{CS}) pin allows the user to deselect the device when desired. If \overline{CS} is high, no new memory operation is initiated, but any pending data transfers (reads and writes) will still be completed.

The IDT71V509 utilizes IDT's high-performance 3.3V CMOS process, and is packaged in a JEDEC Standard 400-mil 44-lead small outline J-lead plastic package (SOJ) for high board density.

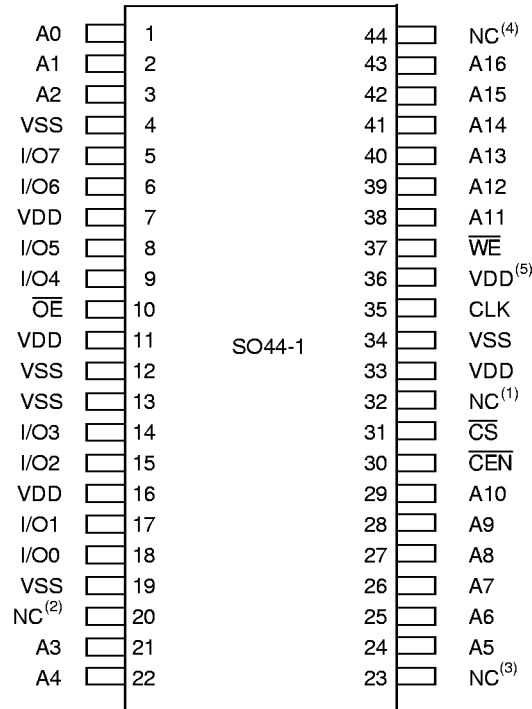
FUNCTIONAL BLOCK DIAGRAM



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PowerPC is a trademark of International Business Machines, Inc.

PIN CONFIGURATION



Notes:

1. Pin 32: Future control input
2. Pin 20: Future I/O8
3. Pin 23: Future A17
4. Pin 44: Future A18
5. Pin 36 does not need to be connected directly to VDD, as long as it is \geq VIH.

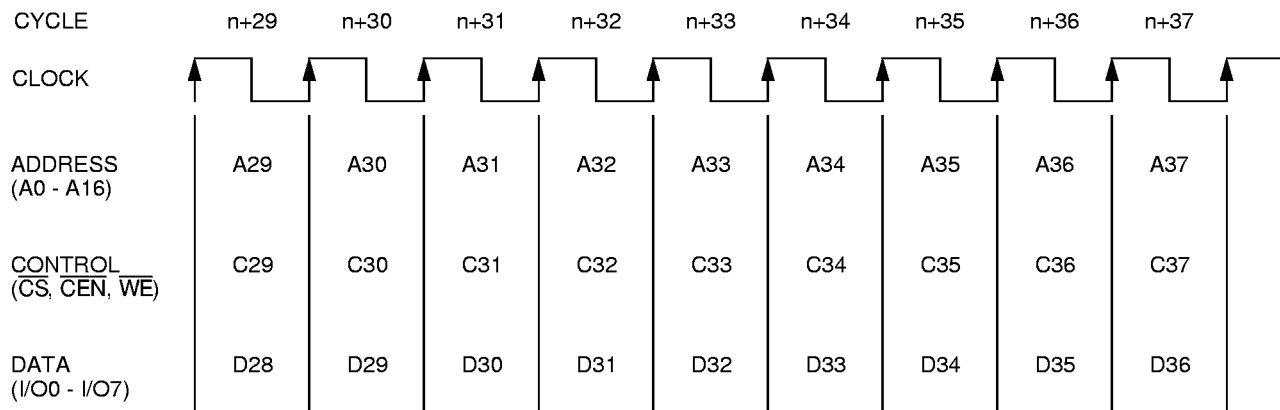
TOP VIEW

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PIN DEFINITIONS⁽¹⁾

Symbol	Pin Function	I/O	Active	Description
A0-A16	Address Inputs	I	N/A	Synchronous Address inputs. The address is registered on every rising edge of CLK if \overline{CEN} and \overline{CS} are both low.
CLK	Clock	I	N/A	The clock input. Except for \overline{OE} , all input and output timing references for the device are with respect to the rising edge of CLK.
\overline{CEN}	Clock Enable	I	LOW	Synchronous clock enable input. When \overline{CEN} is sampled high, the other synchronous inputs are ignored, and outputs remain unchanged. When \overline{CEN} is sampled low, the IDT71V509 operates normally.
\overline{CS}	Chip Select	I	LOW	Synchronous chip select input. When \overline{CS} is sampled low, the device operates normally. When \overline{CS} is sampled high, no read or write operation is initiated, and the I/O bus is tri-stated the next cycle. \overline{CS} is ignored if \overline{CEN} is high at the same rising edge of CLK.
\overline{WE}	Write Enable	I	LOW	Synchronous write enable. If \overline{WE} is sampled low, a write is initiated at the address that is registered at that time. If \overline{WE} is sampled high, a read is initiated at the address that is registered at that time. \overline{WE} is ignored when either \overline{CEN} or \overline{CS} is sampled high.
\overline{OE}	Output Enable	I	LOW	Asynchronous output enable. When \overline{OE} is high, the I/O bus goes high impedance. \overline{OE} must be low to read data from the IDT71V509.
I/O0-I/O7	Data Input/Output	I/O	N/A	Synchronous data input/output (I/O) pins. Both the data input path and data output path are registered and triggered by the rising edge of CLK.
VDD	Power Supply	N/A	N/A	3.3V power supply pins.
VSS	Ground	N/A	N/A	Ground pins.

FUNCTIONAL TIMING DIAGRAM



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TYPICAL OPERATION - \overline{CS} AND \overline{CEN} ARE LOW

Cycle	Address	\overline{WE}	\overline{CS}	\overline{CEN}	\overline{OE}	I/O	Comments
n	A0	H	L	L	?	D-1	?
n+1	A1	L	L	L	L	D0	Data Out
n+2	A2	H	L	L	X	D1	Data In
n+3	A3	L	L	L	L	D2	Data Out
n+4	A4	H	L	L	X	D3	Data In
n+5	A5	L	L	L	L	D4	Data Out
n+6	A6	H	L	L	X	D5	Data In
n+7	A7	L	L	L	L	D6	Data Out
n+8	A8	H	L	L	X	D7	Data In
n+9	A9	L	L	L	L	D8	Data Out
n+10	A10	H	L	L	X	D9	Data In
n+11	A11	H	L	L	L	D10	Data Out
n+12	A12	L	L	L	L	D11	Data Out
n+13	A13	L	L	L	X	D12	Data In
n+14	A14	H	L	L	X	D13	Data In
n+15	A15	H	L	L	L	D14	Data Out
n+16	A16	H	L	L	L	D15	Data Out
n+17	A17	L	L	L	L	D16	Data Out
n+18	A18	L	L	L	X	D17	Data In
n+19	A19	L	L	L	X	D18	Data In
n+20	A20	H	L	L	X	D19	Data In
n+21	A21	H	L	L	L	D20	Data Out

READ OPERATION

Cycle	Address	\overline{WE}	\overline{CS}	\overline{CEN}	\overline{OE}	I/O	Comments
n	A0	H	L	L	X	X	Address and Control meet setup
n+1	X	X	X	X	L	D0	Contents of Address A0 Read Out

H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance

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WRITE OPERATION

Cycle	Address	\overline{WE}	\overline{CS}	\overline{CEN}	\overline{OE}	I/O	Comments
n	A0	L	L	L	X	X	Address and Control meet setup
n+1	X	X	X	L	X	D0	New Data Drives SRAM Inputs

H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance

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READ OPERATION WITH CLOCK ENABLE USED

Cycle	Address	\overline{WE}	\overline{CS}	\overline{CEN}	\overline{OE}	I/O	Comments
n	A0	H	L	L	X	X	Address and Control meet setup
n+1	X	X	X	H	L	D0	Contents of Address A0 Read Out
n+2	A2	H	L	L	L	D0	Contents of Address A0 Read Out
n+3	X	X	X	H	L	D2	Contents of Address A2 Read Out
n+4	X	X	X	H	L	D2	Contents of Address A2 Read Out
n+5	A5	H	L	L	L	D2	Contents of Address A2 Read Out
n+6	A6	H	L	L	L	D5	Contents of Address A5 Read Out
n+7	A7	?	L	L	L	D6	Contents of Address A6 Read Out

H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance

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WRITE OPERATION WITH CLOCK ENABLE USED

Cycle	Address	\overline{WE}	\overline{CS}	\overline{CEN}	\overline{OE}	I/O	Comments
n	A0	L	L	L	X	X	Address and Control meet setup
n+1	X	X	X	H	X	X	Clock Ignored at n+1 to n+2 Low-to-High
n+2	A2	L	L	L	X	D0	New Data Drives SRAM Inputs
n+3	X	X	X	H	X	X	Clock Ignored at n+3 to n+4 Low-to-High
n+4	X	X	X	H	X	X	Clock Ignored at n+4 to n+5 Low-to-High
n+5	A5	L	L	L	X	D2	New Data Drives SRAM Inputs
n+6	A6	L	L	L	X	D5	New Data Drives SRAM Inputs
n+7	A7	?	L	L	X	D6	New Data Drives SRAM Inputs

H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance

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READ OPERATION WITH CHIP SELECT USED

Cycle	Address	\overline{WE}	\overline{CS}	\overline{CEN}	\overline{OE}	I/O	Comments
n	X	X	H	L	X	?	Deselected
n+1	X	X	H	L	X	Z	Deselected
n+2	A2	H	L	L	X	Z	Address and Control meet setup
n+3	X	X	H	L	L	D2	Deselected, Contents of Address A2 Read Out
n+4	A4	H	L	L	X	Z	Address and Control meet setup
n+5	X	X	H	L	L	D4	Deselected, Contents of Address A4 Read Out
n+6	X	X	H	L	X	Z	Deselected
n+7	A7	H	L	L	X	Z	Address and Control meet setup
n+8	X	X	H	L	L	D7	Deselected, Contents of Address A7 Read Out
n+9	X	X	H	L	X	Z	Deselected

H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance

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WRITE OPERATION WITH CHIP SELECT USED

Cycle	Address	\overline{WE}	\overline{CS}	\overline{CEN}	\overline{OE}	I/O	Comments
n	X	X	H	L	X	?	Deselected
n+1	X	X	H	L	X	Z	Deselected
n+2	A2	L	L	L	X	Z	Address and Control meet setup
n+3	X	X	H	L	X	D2	Deselected, New Data Drives SRAM Inputs
n+4	A4	L	L	L	X	Z	Address and Control meet setup
n+5	X	X	H	L	X	D4	Deselected, New Data Drives SRAM Inputs
n+6	X	X	H	L	X	Z	Deselected
n+7	A7	L	L	L	X	Z	Address and Control meet setup
n+8	X	X	X	L	X	D7	Deselected, New Data Drives SRAM Inputs
n+9	X	X	X	L	X	Z	Deselected

H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance

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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Com'l.	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to V _{DD} +0.5	V
T _A	Operating Temperature	0 to +70	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	°C
T _{STG}	Storage Temperature	-55 to +125	°C
P _T	Power Dissipation	1.0	W
I _{OUT}	DC Output Current	50	mA

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{DD} and Input terminals only.
- I/O terminals.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{DD}	Supply Voltage	3.135	3.3	3.465	V
V _{SS}	Supply Voltage	0	0	0	V
V _{IH}	Input High Voltage - Inputs	2.0	—	4.6	V
V _{IH}	Input High Voltage - I/O	2.0	—	V _{DD} +0.3	V
V _{IL}	Input Low Voltage	-0.3 ⁽¹⁾	—	0.8	V

NOTE:

- V_{IL} (min.) = -1.5V for pulse width less than 5 ns, once per cycle.

CAPACITANCE

(T_A = +25°C, f = 1.0MHz, SOJ package)

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 3dV	6	pF
C _{I/O}	I/O Capacitance	V _{OUT} = 3dV	7	pF

NOTE:

- This parameter is guaranteed by device characterization, but not production tested.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{DD} = 3.3V ±5%)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I _{LI}	Input Leakage Current	V _{DD} = Max., V _{IN} = 0V to V _{DD}	—	5	μA
I _{LO}	Output Leakage Current	$\overline{CS} \geq V_{IH}$, V _{OUT} = 0V to V _{DD} , V _{DD} = Max.	—	5	μA
V _{OL}	Output Low Voltage	I _{OL} = 5 mA, V _{DD} = Min.	—	0.4	V
V _{OH}	Output High Voltage	I _{OH} = -5 mA, V _{DD} = Min.	2.4	—	V

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE⁽¹⁾ (V_{DD} = 3.3V ±5%, V_{HD} = V_{DD} - 0.2V, V_{LD} = 0.2V)

Symbol	Parameter	Test Condition	71V509S66	71V509S50	Unit
I _{DD}	Operating Power Supply Current	$\overline{CS} \leq V_{IL}$, Outputs Open, V _{DD} = Max., V _{IN} ≥ V _{IH} or ≤ V _{IL} , f = f _{MAX} ⁽²⁾	150	120	mA
I _{SB}	Standby Power Supply Current	$\overline{CS} \geq V_{IH}$, Outputs Open, V _{DD} = Max., V _{IN} ≥ V _{IH} or ≤ V _{IL} , f = f _{MAX} ⁽²⁾	50	45	mA
I _{SB1}	Full Standby Power Supply Current	$\overline{CS} \geq V_{HD}$, Outputs Open, V _{DD} = Max., V _{IN} ≥ V _{HD} or ≤ V _{LD} , f = 0 ⁽²⁾	25	25	mA

NOTES:

- All values are maximum guaranteed values.
- At f = f_{MAX}, address inputs are switching at 1/t_{CYC} and CLK is cycling at 1/t_{CYC}; f=0 means no input signals are changing.

AC ELECTRICAL CHARACTERISTICS

(VDD = 3.3V ±5%, TA = 0 to 70°C)

Symbol	Parameter	IDT71V509S66		IDT71V509S50		Unit
		Min.	Max.	Min.	Max.	
Clock Parameters						
fMAX	Clock Frequency	—	66	—	50	MHz
tCYC	Clock Cycle Time	15	—	20	—	ns
tCH	Clock High Pulse Width	5	—	6	—	ns
tCL	Clock Low Pulse Width	5	—	6	—	ns
Output Parameters						
tCD	Clock High to Valid Data	—	9	—	10	ns
tCDC	Clock High to Data Change	2	—	2	—	ns
tCLZ ⁽¹⁾	Clock High to Output Active	2	—	2	—	ns
tCHZ ⁽¹⁾	Clock High to Data High-Z	2	5	2	6	ns
tOE	Output Enable Access Time	—	6	—	7	ns
tOLZ ⁽¹⁾	Output Enable Low to Data Active	0	—	0	—	ns
tOHZ ⁽¹⁾	Output Enable High to Data High-Z	—	5	—	6	ns
Set Up Times						
tSE	Clock Enable Setup Time	2	—	2.5	—	ns
tSA	Address Setup Time	2	—	2.5	—	ns
tSD	Data In Setup Time	2	—	2.5	—	ns
tSW	Write Enable Setup Time	2	—	2.5	—	ns
tSC	Chip Select Setup Time	2	—	2.5	—	ns
Hold Times						
tHE	Clock Enable Hold Time	1	—	1	—	ns
tHA	Address Hold Time	2.5	—	2.5	—	ns
tHD	Data In Hold Time	1	—	1	—	ns
tHW	Write Enable Hold Time	1	—	1	—	ns
tHC	Chip Select Hold Time	1	—	1	—	ns

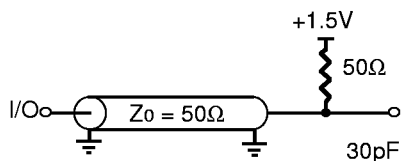
NOTES:

1. Transition is measured ±200mV from steady-state.

AC TEST CONDITIONS

Input Pulse Levels	0 to 3V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

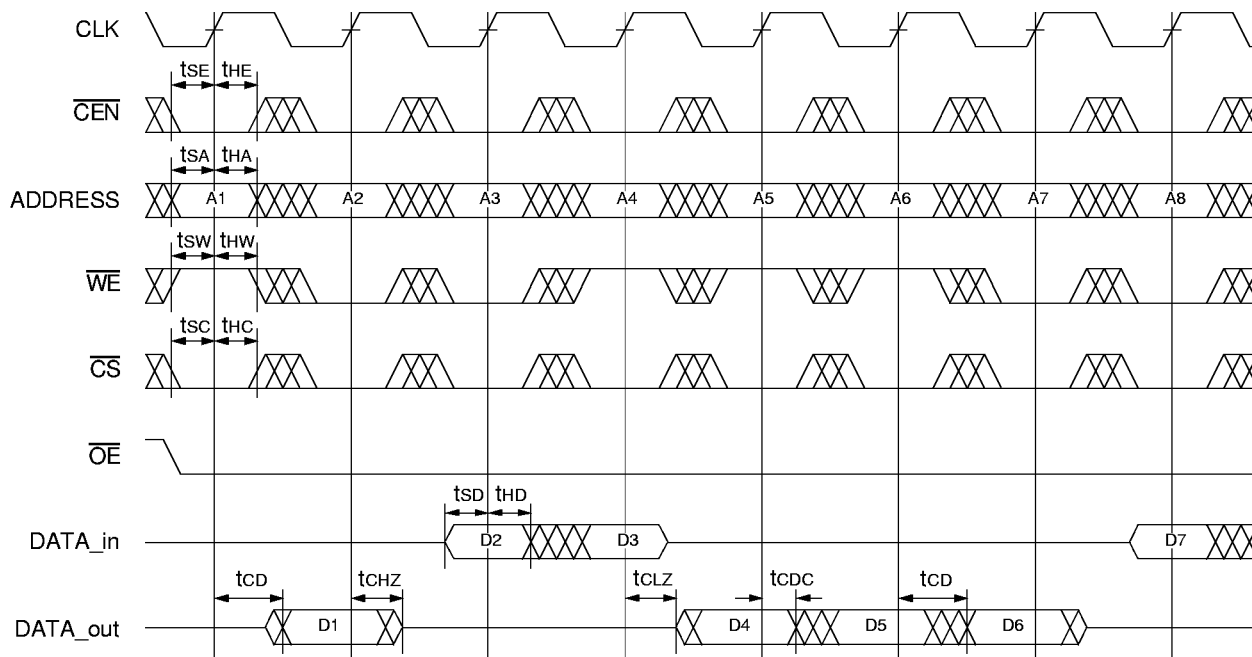
AC TEST LOADS



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Figure 1. AC Test Load

TIMING WAVEFORM OF READ AND WRITE CYCLES⁽¹⁾

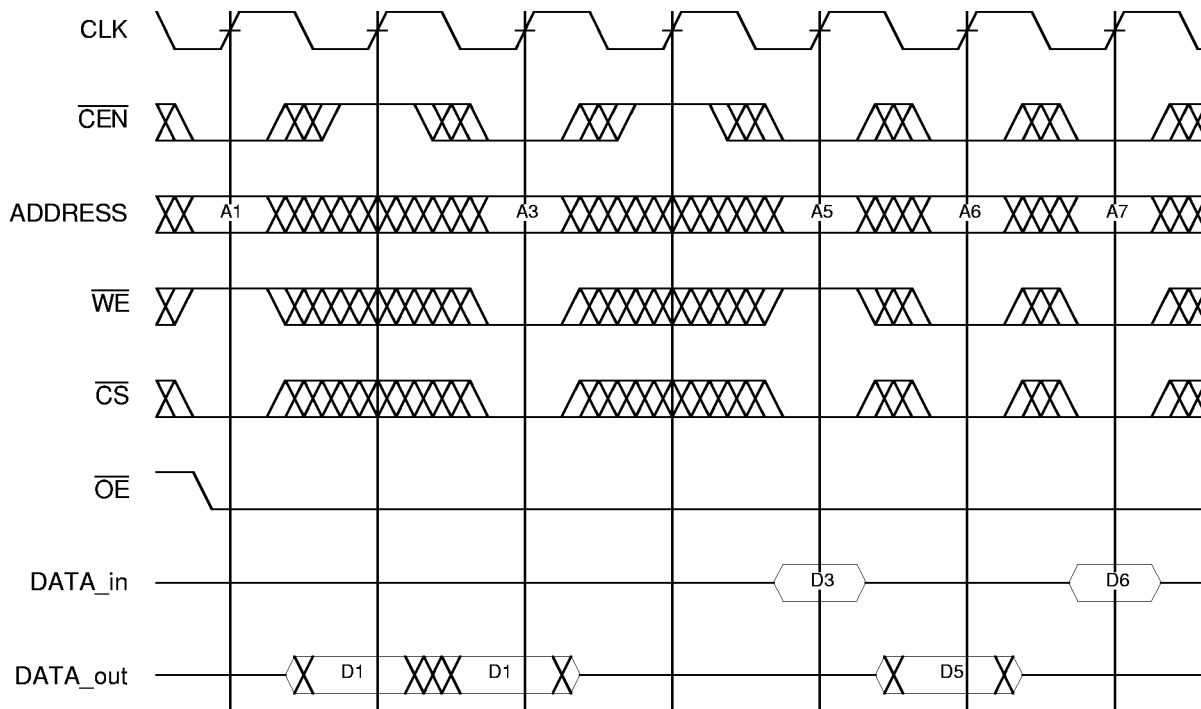


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NOTES:

1. Dx represents the data for address Ax.
2. DATA_in and DATA_out together represent I/O(7:0).

TIMING WAVEFORM OF $\overline{\text{CEN}}$ OPERATION⁽¹⁾

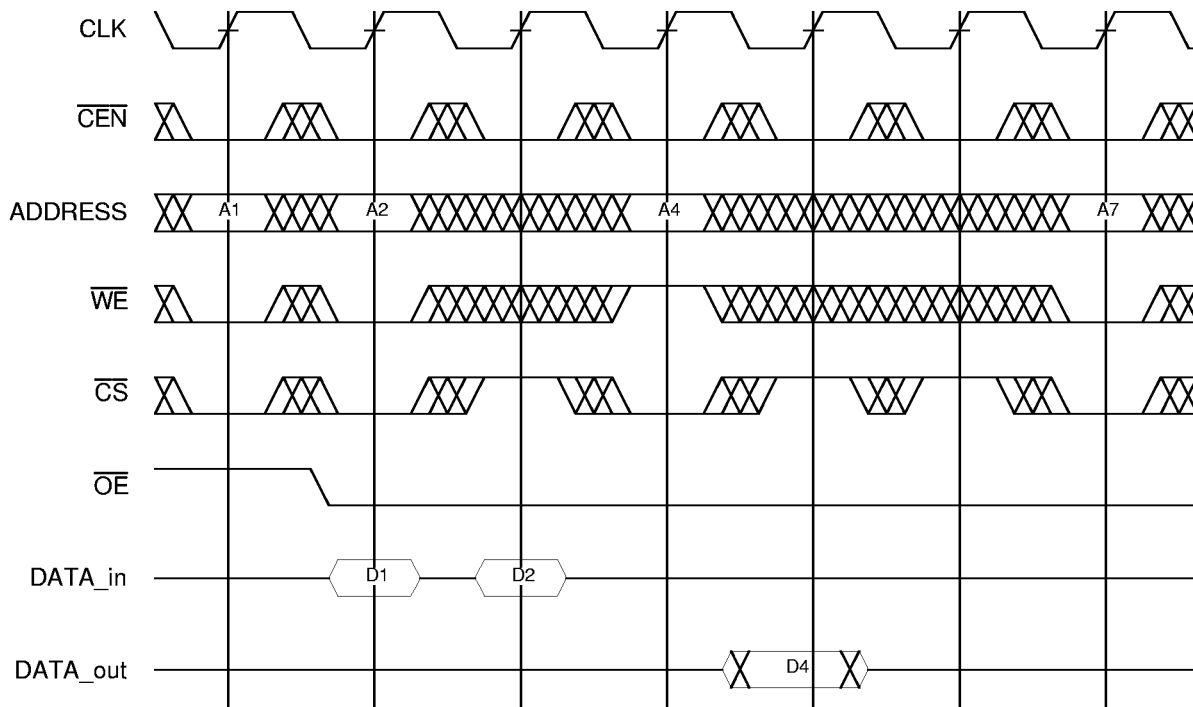


3618 drw 06

NOTES:

1. Dx represents the data for address Ax.
2. DATA_in and DATA_out together represent I/O(7:0).

TIMING WAVEFORM OF \overline{CS} OPERATION⁽¹⁾

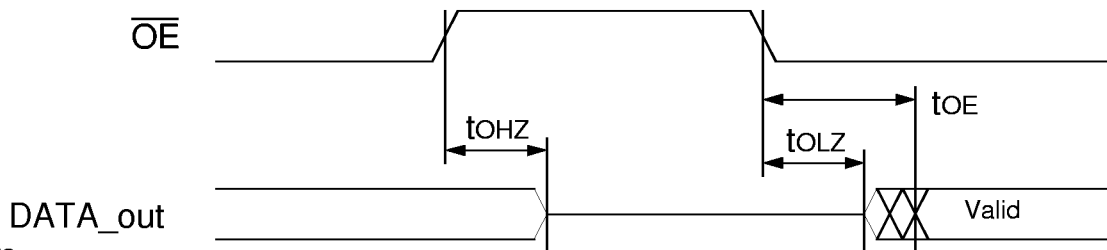


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NOTES:

1. Dx represents the data for address Ax.
2. DATA_in and DATA_out together represent I/O(7:0).

TIMING WAVEFORM OF \overline{OE} OPERATION



NOTES:

1. A read operation is assumed to be in progress.

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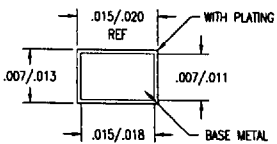
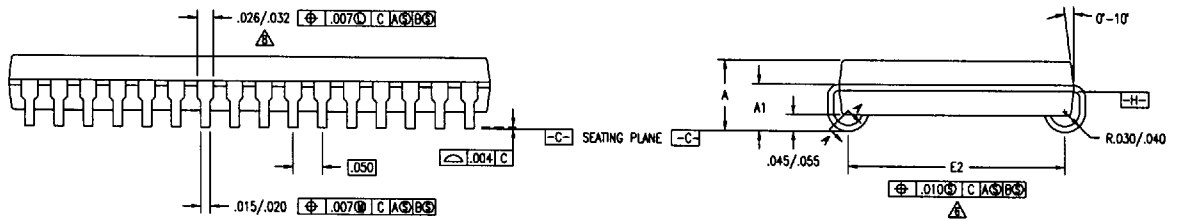
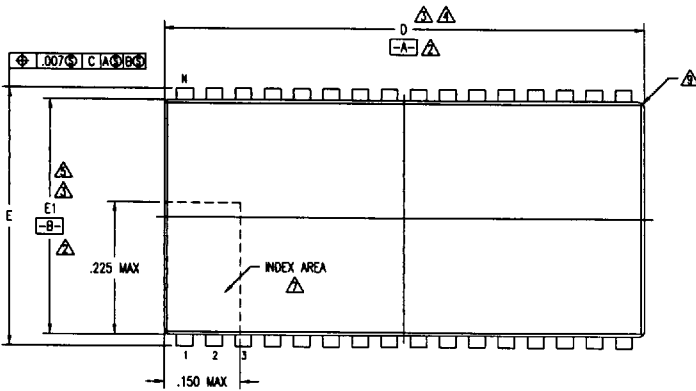
ORDERING INFORMATION

IDT	71V509	S	X	Y	
	Device Type	Power	Speed	Package	
				Y	} Small Outline J-Bend, 44 pin (SO44-1)
				50 66	
					} Clock Frequency in Megahertz

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PACKAGE DIAGRAM OUTLINES
SOJ (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
20287	00	INITIAL RELEASE	04/11/91	A. KATZ
21863	01	ADD 28 LD	01/24/92	T. VU
27321	02	ADD A2 DIM	11/14/94	T. VU
27645	03	REDRAW TO JEDEC FORMAT	03/15/95	T. VU
27945	04	ADD 44 LD	06/25/95	



SECTION A-A

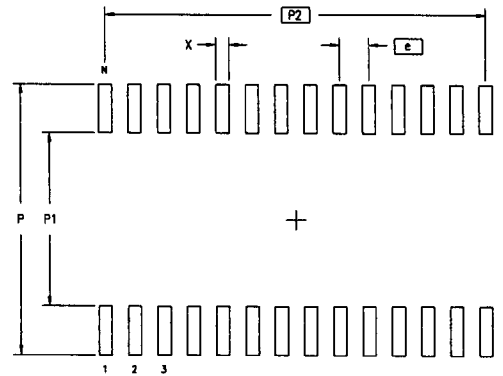
TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2975 Stonder Way, Santa Clara, CA 95054 PHONE: (408) 727-8118 FAX: (408) 492-8674 TMC 910-338-2070	
DECIMAL	ANGULAR	±	
XX#	XX#		
XXX#	XXX#		
XXXX#	XXXX#		
APPROVALS	DATE	TITLE PB PACKAGE OUTLINE	
DRAWN	02/15/96	.400" BODY WIDTH SOJ	
CHECKED		.050" PITCH	
SIZE	DRAWING No.	PSC-4033	REV 04
C			
DO NOT SCALE DRAWING			

PACKAGE DIAGRAM OUTLINES
SOJ (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
20267	00	INITIAL RELEASE	04/11/91	A. KATZ
21863	01	ADD 28 LD	01/24/92	T. WU
27321	02	ADD A2 DIM	11/14/94	T. WU
27645	03	REDRAW TO JEDEC FORMAT	03/15/95	T. WU
27945	04	ADD 44 LD	06/25/95	

SYMBOL	JEDEC # S028-6				JEDEC # S032-3				JEDEC # S044-1			
	JEDEC VARIATION			NOTE	JEDEC VARIATION			NOTE	JEDEC VARIATION			NOTE
	AA	MIN	NOM		MAX	AB	MIN		NOM	MAX	AE	
A	.131	.138	.145		.131	.138	.145		.131	.138	.145	
A1	.082	-	-		.082	-	-		.082	-	-	
D	.720	.725	.730	3,4	.820	.825	.830	3,4	1.120	1.125	1.130	3,4
E	.435	.440	.445		.435	.440	.445		.435	.440	.445	
E1	.395	.400	.405	3,5	.395	.400	.405	3,5	.395	.400	.405	3,5
E2	.360	.370	.380	6	.360	.370	.380	6	.360	.370	.380	6
N	28				32				44			

LAND PATTERN DIMENSIONS



NOTES:

- ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
- DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **-H-**
- DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE **-H-**
- DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 PER SIDE
- DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 PER SIDE
- DIMENSION E2 TO BE DETERMINED AT SEATING PLANE **-C-** CONTACT POINT
- DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
- LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .005 IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION
- EXACT SHAPE OF EACH CORNER IS OPTIONAL
- ALL DIMENSIONS ARE IN INCHES
- THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-061, VARIATION AA, AB & AE

	MIN	MAX	MIN	MAX	MIN	MAX
P	.458	.466	.458	.466	.458	.466
P1	.290	.294	.290	.294	.290	.294
P2	.650 BSC		.750 BSC		1.050 BSC	
X	.018	.026	.018	.026	.018	.026
e	.050 BSC		.050 BSC		.050 BSC	
N	28		32		44	

TOLERANCES UNLESS SPECIFIED		INTEGRATED DEVICE TECHNOLOGY, INC.	
DECIMAL	ANGULAR	2975 Stender Way, Santa Clara, CA 95054	
XXX±	±	PHONE: (408) 727-8118	
XXXX±		FAX: (408) 482-8874	
XXXX±		TEL: 910-338-2070	
APPROVALS	DATE	TITLE	
DRAWN Ad	02/15/98	PB PACKAGE OUTLINE	
CHECKED		.400" BODY WIDTH SOJ	
		.050" PITCH	
		SIZE	REV
		C	04
DO NOT SCALE DRAWING			