VTC Inc.
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# VM65020

## DIGITAL PRML CHANNEL ENCODE/DECODE PROCESSOR

960801

**PRELIMINARY**

August,1996



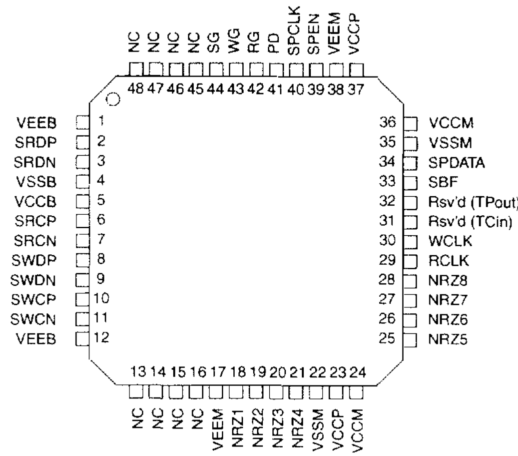
### FEATURES

- Channel clock divider
- 4-bit Nibble and 8-bit Byte wide Bi-directional NRZ interfaces
- Optional WCLK input strobe of NRZ data
- 8-bit wide Scrambler and Descrambler, with Pseudo Random Number Generator
- 8/9 (0, 4, 4) Encoder and Decoder
- Parallel-to-Serial and Serial-to-Parallel converters
- SYNC Byte Detector, programmable, dual byte ("or" type)
- Serial Control Register port
- 4-bit Nibble and 8-bit Byte Direct Test Write and Read

### DESCRIPTION

The VM65020 is a PolarMOS2i integrated circuit that provides parallel-to-serial and serial-to-parallel conversion of data between the disk controller and the analog PRML channel chip, VM65014. In read mode this circuit performs sync byte detection, read clock synchronization, data word framing, 9/8 (0, 4, 4) *decoding, descrambling, and byte-wide or nibble-wide NRZ interfacing*. In write mode this circuit takes in byte-wide or nibble-wide NRZ information (consisting of zero-level VCO sync field, sync byte 1, spacer, sync byte 2, and user data), scrambles, 8/9 (0, 4, 4) encodes, and serializes it out to VTC's VM65014. This device can handle NRZ channel data rates in excess of 180Mbits/sec, or 22.5 Mbytes/sec.

### CONNECTION DIAGRAM




48-pin Thin Quad Flat Pack

### ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage:
- $V_{CC}$ .................... –0.3V to +7V

Input Voltages:
- Digital Input Voltage $V_{IN}$ .................. –0.3V to ($V_{CC}$+0.3V)
- Analog Input Voltage $V_{IN}$ .................. –0.3V to ($V_{CC}$+0.3V)

Storage Temperature $T_{stg}$ .................... –65° to 150°C

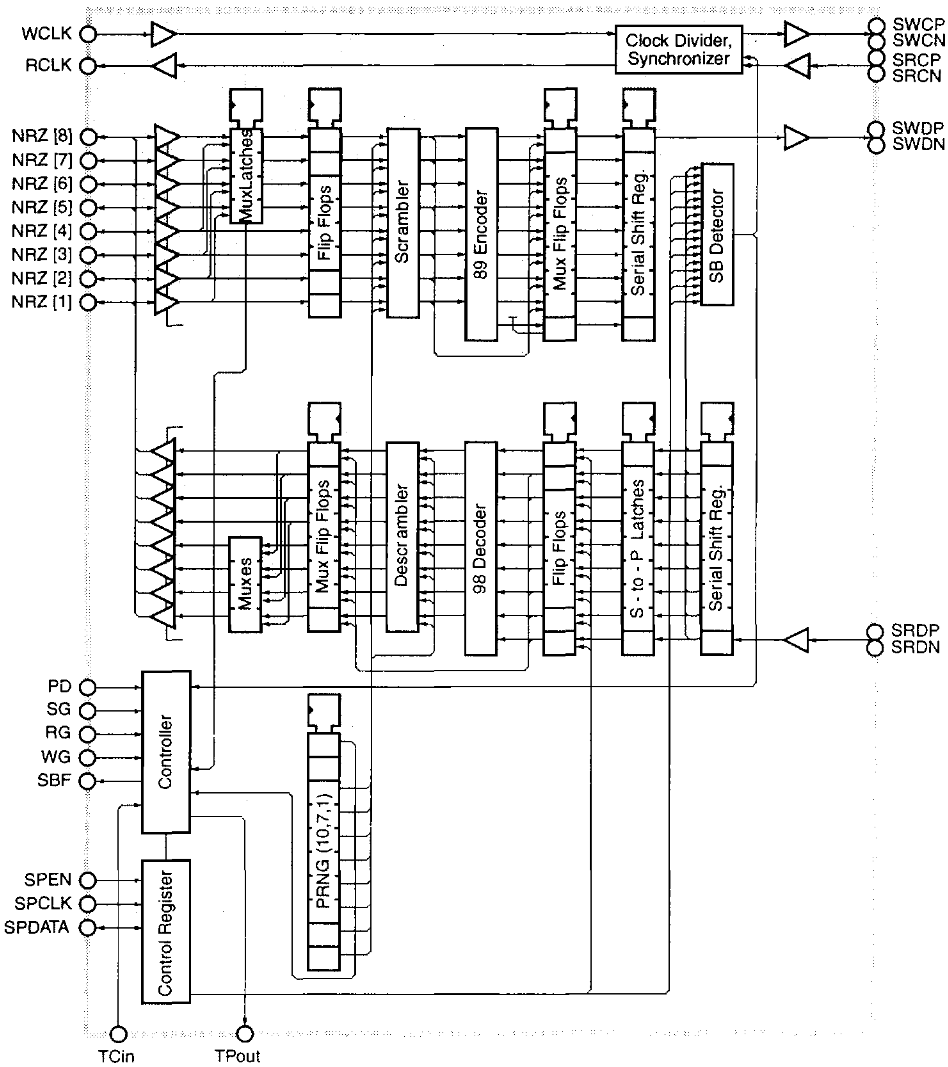
Junction Temperature $T_J$ .................... 150°C

### RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
- $V_{CC}$ .................... +5V ± 10%

Ambient Temperature $T_A$ (still air) .................... 0°C to 70°C

## BLOCK DIAGRAM




## BLOCK-BY-BLOCK FUNCTIONAL DESCRIPTIONS

Descriptions of the logical blocks are presented beginning on page 60.

## MODES OF OPERATION

Descriptions of the Write, Read, Idle, Power Down, Direct Test Write, and Direct Test Read modes are presented on the following pages.

## WRITE MODE

Write Mode (WM) is the set of operations where 8-bit byte wide, or 4-bit nibble wide, parallel information is taken in from the disk controller and passed on to the VM65014 in serial form. The information passed consists of three portions. The first is known as the VCO Sync Field, the second as the SYNC Bytes, and the third as the User Data Field.

In write mode the NRZ clock, RCLK, is $1/9^{th}$ the frequency of the channel clock for byte mode, and twice that for nibble mode. The channel clock is produced by the frequency synthesizer in the VM65014.

Write mode normally begins with the Write Gate (WG) going high (SG and RG both low). Several options for strobing the NRZ data being written into the VM65020 are available to the user. The NRZ data can be strobed in using the RCLK, either edge of which can be selected to accommodate for phase delays either in the controller chip or in the NRZ interconnect lines. The NRZ data can also be strobed in using the WCLK input's rising edge.

The first *N* number of NRZ bytes will be used for writing the VCO Sync Field. During these cycles, the NRZ pins must be driven low by the disk controller (i.e. $00_H$ input to the NRZ pins). This results in about 9x(*N*+2) Channel cycles of 1's being sent to the VM65014 for precoding to '11001100...', which is the actual VCO sync field written to the disk. The VM65020 *assumes* that the first two NRZ bytes are $00_H$, *which allows the user to be 'late' in driving the NRZ lines low at the start of a write mode operation. The length of the* VCO Sync Field is left up to the user and can be any length (greater than two bytes). The end of the VCO Sync Field, and thus the first Sync Byte, is determined by the detection of any non-zero pattern on the MSB bits of the NRZ byte (i.e., when NRZ bits 5, 6, 7, or 8 go non-zero). This applies to both Byte mode and Nibble mode, where the leading nibble is MSB and the trailing nibble is LSB of the whole 8-bit word.

Following the *N* number of NRZ byte cycles where the VCO Sync Field is written, there are three NRZ bytes for the writing of the SYNC Bytes. Here the two 8-bit SYNC Byte words from the disk controller, and the 8-bit spacer word between them, are encoded into 9-bit words that are then serially shifted to the VM65014 for writing to the disk at nine times the NRZ byte rate.

After these three NRZ bytes for SYNC Byte, the NRZ lines begin to send user data to the VM65020. The 8-bit user data is first scrambled with a pseudo random number stream, then it is encoded into 9-bit words, which in turn are serially shifted to the VM65014 for writing to the disk. The writing of user data continues until the end of the write mode when WG goes low.

It should be noted that it takes three NRZ byte cycles to pass the NRZ byte input information on through the VM65020, out the VM65014, and on to the Preamp. Therefore, at the end of the write mode, three additional NRZ bytes are needed to flush the final user data word on out to the Preamp.

*The following diagrams show the various portions of the NRZ signal during the normal write mode of operation.*

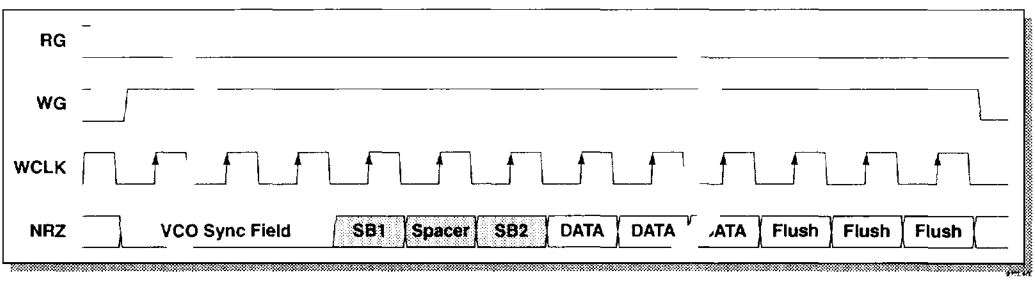



**Diagram 1a Write Mode of Operation (Byte-Wide)**

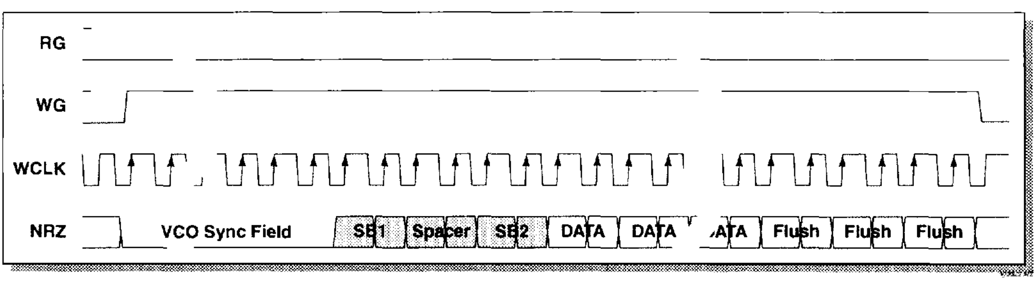



**Diagram 1b Write Mode of Operation (Nibble-Wide)**

## READ MODE

Read Mode (RM) is the set of operations where serial information is taken in from the VM65014 and passed to the disk controller in 8-bit byte wide, of 4-bit nibble, parallel form. The information received from the VM65014 consists of three portions. The first is known as the VCO Sync Field, the second as the SYNC Bytes, and the third as the User Data Field.

In read mode the NRZ clock, RCLK, is 1/9$^{th}$ the frequency of the channel clock for byte mode, and twice that for nibble mode. The channel clock is produced by the timing recovery circuit in the VM65014.

Read mode begins with the Read Gate (RG) going high (SG and WG both low). Once in read mode WG can go high but will be ignored by the VM65020. Before the end of the read mode WG should go low prior to RG being dropped. This will prevent an immediate read mode to write mode switch. The NRZ data being read will be strobed out of the VM65020 using the falling edge of RCLK, which is generated within the device.

For the duration of the read mode the VM65020 is given control of the NRZ bus. At the start of the read mode, the NRZ output drivers change from their normal high impedance state to driving the NRZ output lines low.

The serial bit stream is scanned for either of the two 9-bit SYNC Byte words. The serial bit stream will start out consisting of the VCO Sync Field and then followed by the two 9-bit SYNC Byte words separated by a 9-bit spacer word, which in turn are followed by the User Data field.There is no time limit of the search for the SYNC Byte words. The search will continue throughout the Read Mode until SYNC Byte(s) is found. Acknowledging the failure to detect the SYNC Byte during the proper portion of the Read Mode is left up to the Controller chip.

Note that is quite possible to find a SYNC Byte pattern anywhere along the serial bit stream within the user data portion as all possible SYNC Byte words are legal 8/9 (0, 4, 4) code words.

If the VM65020 successfully detects either of the 9-bit SYNC Byte words, the RCLK is synchronized for NRZ word framing. Nine bit sections of the serial bit stream are captured in parallel, starting with the first nine bits of the User Data which follows the second SYNC Byte word. Each 9-bit user data word is decoded into an 8-bit word. These words are then descrambled with the same pseudo random number stream that was used to scramble them during an earlier write operation. These descrambled words are then driven out the NRZ pins. The reading of user data continues until the end of the read mode when RG goes low.

The user has the option to precede the User Data with the SYNC Byte pattern. This is the pattern stored in the control register and is equal to the second of the two SYNC Byte words. This pattern is decoded into an 8-bit word prior to being driven out the NRZ pins.

The non-zero NRZ data patterns are strobed out of the VM65020 on the falling edge of RCLK. The first non-zero data pattern, be it User Data or the SYNC Byte Pattern, corresponds with the SYNC Byte Flag (SBF) going low, also on the falling edge of RCLK.

The following diagrams show the various portions of the NRZ signal during the normal read mode of operation.

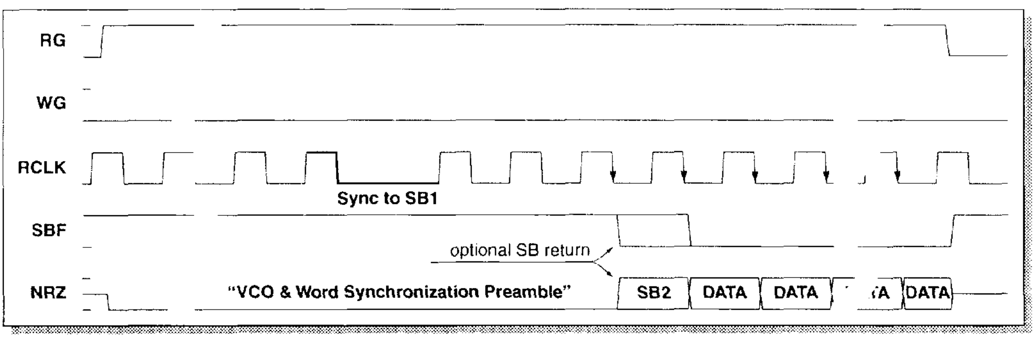



**Diagram 2a Read Mode of Operation (Byte-Wide)**

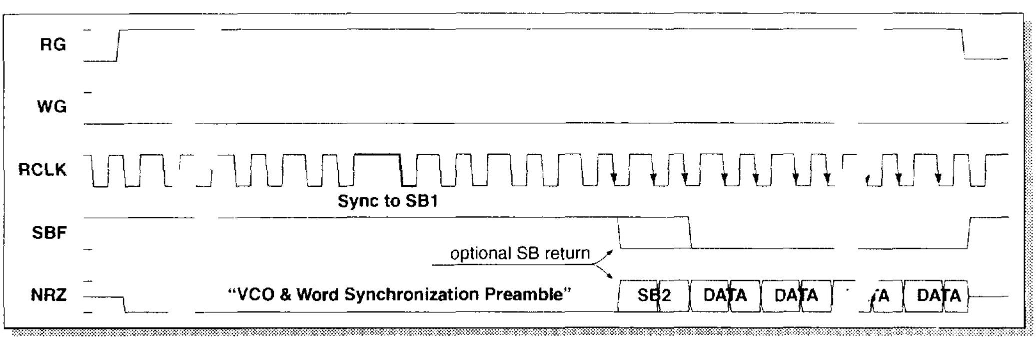



**Diagram 2b Read Mode of Operation (Nibble-Wide)**





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## IDE MODE

Idle Mode (IM) in the VM65020 is considered to be the absence of either a write mode or a read mode. It is the case whenever WG and RG are both low, or whenever Servo Gate (SG) is high. During an idle mode none of the VM65020 circuitry is powered down; everything remains powered up and ready to respond to the next read or write mode operation. During idle mode the serial channel clock continues to be divided down to create the parallel NRZ clock known as RCLK.

Once in idle mode based on SG being high, WG and/or RG can go high but will be ignored by the VM65020. Before the end of such an idle mode WG and RG should go low prior to directing either a write mode or a read mode. Failure to bring WG and RG low before bringing SG low will result in entering a read or write mode upon the dropping of SG, which is legal for the VM65020 as SG being high is an idle mode condition. (This is not the case for the VM65014.)

## POWER DOWN MODE

Power Down Mode (PDM) is the condition where all CML circuitry[1] is powered down, the RCLK idled, and the CMOS TTL input and output pins (except for the Serial Control Register Port) are disabled. This condition will be controlled by either a single control register bit (SLP) or the power down (PD) input pin.

## DIRECT TEST WRITE MODE

Direct Test Write Mode (DTWM) is the set of operations where 8-bit wide parallel information is taken in from the disk controller *and sent directly to the VM65014 in serial form. This mode is a* system test mode determined by the setting of a single control register bit.

In the direct test write mode the NRZ clock, RCLK, is 1/8$^{th}$ the frequency of the channel clock. This is because the 8-bit wide NRZ data is not encoded into 9-bit words prior to being converted into a serial form.

Direct test write mode begins with the Write Gate (WG) going high (SG and RG both low). Several options for strobing the NRZ data being written into the VM65020 are available to the user. The NRZ data can be strobed in using the RCLK, either edge of which can be selected to accommodate for phase delays either in the controller chip or in the NRZ interconnect lines. The NRZ data can also be strobed in using the WCLK input's rising edge.

The first *N* number of NRZ bytes will be used for writing the VCO Sync Field. During these cycles, the NRZ pins must be driven low by the disk controller (i.e. $00_H$ input to the NRZ pins). This results in about 8x(*N*+2) Channel cycles of 1's being sent to the VM65014 for precoding to '11001100...', which is the actual VCO sync field written to the disk. The VM65020 *assumes* that the first two NRZ bytes are $00_H$, which allows the user to be 'late' in driving the NRZ lines low at the start of a write mode operation. The length of the VCO Sync Field is left up to the user and can be any length (greater than two bytes). The end of the VCO Sync Field, and thus the first Sync Byte, is determined by the detection of any non-zero pattern on the MSB bits of the NRZ byte (i.e., when NRZ bits 5, 6, 7, or 8 go non-zero). This applies *to both Byte mode and Nibble mode, where the leading nibble is* MSB and the trailing nibble is LSB of the whole 8-bit word.

Following the *N* number of NRZ byte cycles where the VCO Sync Field is written, there are three NRZ cycles for the writing of the SYNC Bytes. Here the two 8-bit SYNC Byte words from the disk controller, and the 8-bit spacer word between them, are neither scrambled nor encoded into 9-bit words. Rather, they are directly converted into a serial form which is serially shifted to the VM65014 for writing to the disk at eight times the NRZ cycle rate.

After these three NRZ cycles of Sync Byte writing, the NRZ lines begin to send user data to the VM65020. This data is also neither scrambled nor encoded into 9-bit words, but simply converted into a serial form which is serially shifted to the VM65014. Direct test writing continues until the end of the write mode when WG goes low.

It should be noted that it takes three NRZ byte cycles to pass the NRZ byte input information on through the VM65020, out the VM65014, and on to the Preamp. Therefore, at the end of the write mode, three additional NRZ bytes are needed to flush the final user data word on out to the Preamp.

Diagrams for the direct test write mode of operation look identical to those for the normal write operation as shown earlier.

## DIRECT TEST READ MODE

Direct Test Read Mode (DTRM) is the set of operations where serial information is taken in from the VM65014 and sent directly to the disk controller in 8-bit wide parallel form. This mode is a system test mode determined by the setting of a single control register bit.

In the direct test read mode the NRZ clock, RCLK, is 1/8$^{th}$ the frequency of the channel clock. This is because the 8-bit wide NRZ data is not decoded from 9-bit words after being converted from serial form. Rather, 8-bit segments of the serial bit stream are being captured in parallel.

Direct test read mode begins with the Read Gate (RG) going high (SG and WG both low). Once in read mode WG can go high but will be ignored by the VM65020. Before the end of the read mode WG should go low prior to RG being dropped. This will prevent a direct read mode to write mode switch. The NRZ data being read will be strobed out of the VM65020 using the falling edge of RCLK, which is generated within the device.

For the duration of the direct test read mode the VM65020 is given control of the NRZ bus. At the start of the read mode, the NRZ output drivers change from their normal high impedance state to driving the NRZ output lines low.

The serial bit stream is scanned for either of the two 9-bit SYNC Byte words. The serial bit stream will start out consisting of the VCO Sync Field and then followed by the two 8-bit SYNC Byte words separated by a 8-bit spacer word, which in turn are followed by the User Data field. There is no time limit of the search for the SYNC Byte words. The search will continue throughout the Direct Test Read Mode until SYNC Byte(s) is found. Acknowledging the failure to detect the SYNC Byte during the proper portion of the Read Mode is left up to the Controller chip.

Note that in Direct Test modes only 8-bit words are written, but 9-bit SYNC Byte words are still being scanned-for. In order to accommodate this, the last bit of the VCO Sync Field, a '1', will be included with the first 8-bit SYNC Byte word to make up the

READ CHANNEL CIRCUITS

[1] CML (Current Mode Logic) circuitry consists of the Parallel-to-Serial, Serial-to-Parallel, SYNC Byte Detector, Channel clock divider, and associated circuitry.

required nine bits. And similarly, the last bit of the 8-bit spacer word, which here must be a '0', will be included with the second 8-bit SYNC Byte word to make up the required nine bits.

Note also that is possible to find a SYNC Byte pattern anywhere along the serial bit stream within the user data portion.

If the VM65020 successfully detects either of the 9-bit SYNC Byte words, the RCLK is synchronized for NRZ word framing. Eight-bit sections of the serial bit stream are captured in parallel, starting with the first eight bits of the User Data which follows the second SYNC Byte word. Each 8-bit user data word bypasses the decoder and descrambler. These 8-bit words are then driven out the NRZ pins. The reading of user data continues until the end of the read mode when RG goes low.

The non-zero NRZ data patterns are strobed out of the VM65020 on the falling edge of RCLK. The first non-zero data pattern corresponds with the SYNC Byte Flag (SBF) going low, also on the falling edge of RCLK.

The user has the option to require *both* SYNC Byte words to be detected prior to reading out direct test data. This option tightens up the error tolerance and is used to verify zero bit errors in the SYNC Byte region.

The user has the option to forego SYNC Byte detection and framing. In this option RCLK is not synchronized to anything and the serial bit stream is simply captured in sequential eight bit sections and passed out to the NRZ pins. This is intended as a 'last resort' option when the serial bit stream is so corrupted that SYNC Byte words can not be detected for use in framing.

Diagrams for the direct read mode of operation look identical to those for the normal read operation as shown earlier.



## FUNCTIONAL BLOCKS

- 8-bit Bidirectional NRZ interface
- 4-bit Bidirectional NRZ Interface
- 8-bit wide Scrambler / Descrambler, with PRNG
- 8/9 (0, 4, 4) Encoder / Decoder
- Parallel-to-Serial and Serial-to-Parallel converters
- SYNC Byte Detector, programmable
- Channel clock divider
- Mode Controller and Sequencers, programmable
- Serial Control Register port

## 8-BIT (BYTE-WIDE) BIDIRECTIONAL NRZ INTERFACE

The 8-bit NRZ interface is a set of eight bidirectional pins that provide the ability to interface with a byte-wide disk controller. Each pin has a TTL level input detector and a tristate TTL level output driver. The input detector is disabled during sleep mode. The output driver is put into high impedance when not driving the NRZ line. These pins, when not driving data out of the VM65020, must, like all CMOS inputs, be driven by external sources.

In write mode, the NRZ data can be latched-in on the rising edge of WCLK or either edge of RCLK. These choices are determined by the setting of two control register bits. The length of the VCO Sync Field is left up to the user. Internal circuitry ignores the first two NRZ bytes, assuming them to be zero. This allows for a possible late driving of the NRZ bus with respect to the rising edge of WG. The end of the VCO Sync Field, and the start of the SYNC Byte section, is determined by the first non-zero byte strobed into the VM65020. NRZ[8] through NRZ[5] are used for non-zero detection. NRZ[4] through NRZ[1] are not monitored by the non-zero detector circuitry. Thus the MSB half of the first SYNC Byte *must* be non-zero, while the LSB half can be all zero.

In read mode, the NRZ data is driven out on the falling edge of RCLK. When RG goes high, the NRZ interface will drive low until either SYNC byte has been detected. The first non-zero data driven out on the NRZ pins will be either the first User Data word or else the SYNC Byte pattern. The user has the option to precede the User Data with the SYNC Byte pattern.

## 4-BIT (NIBBLE-WIDE) BIDIRECTIONAL NRZ INTERFACE

The operation of the 4-bit NRZ interface is much the same as that of the 8-bit interface. The main difference being that only the pins NRZ[4] through NRZ[1] are used, with NRZ[8] through NRZ[5] being tied off by the user. Eight-bit words are still used but they are broken into two 4-bit nibbles. The first nibble is the MSB half and the second nibble is the LSB half. Within the VM65020 the two 4-bit halves are concatenated into a full 8-bit word. During Nibble operations the RCLK is run at twice the frequency as the internal byte clock, thus maintaining equivalent byte speed operation.

## 8-BIT WIDE SCRAMBLER / DESCRAMBLER, WITH PRNG

The Scrambler and Descrambler circuits, which are used to randomize repetitive user data, half-add each bit of an 8-bit Pseudo Random Number (PRN) to each bit of the 8-bit user data. The half-adding is done through the use of eight XNOR gates. The same PRN is half-added during write and again dur-



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*ing read, resulting in the original user data being returned.* The PRN comes from a shared Pseudo Random Number Generator (PRNG) which itself is based upon the $X^{10} + X^3 + 1$ polynomial.

At the beginning of write mode the PRNG is initialized to all 0's. The PRNG then generates a PRN of continuous $00_H$ until it is set with the $FF_H$ seed. This continuous $00_H$ PRN in turn allows the scrambler to act as inverting buffers on the NRZ's VCO Sync Field during write mode. This causes the continuous $00_H$ being detected on the NRZ inputs to be inverted into continuous $FF_H$ before entering the Encoder. At the end of the VCO Sync Field the PRNG is set to all 1's. This allows for a maximum run length PRN pattern as well as allowing the scrambler to act as a noninverting buffer on the NRZ's SYNC Bytes and Spacer byte. At the end of the three Sync Byte cycles, the PRNG is enabled into a free-running condition, where PRN's are generated and half-added to the User Data, until the end of the write mode.

At the beginning of read mode the PRNG is initialized to all 1's. Following the successful detection of a Sync Byte, the PRNG is enabled into a free-running condition, where PRN's are generated and half-added to the User Data before being passing on to the NRZ output drivers, until the end of the read mode.

During Idle, Sleep, or Direct Test modes the PRNG's clock is disabled to save power. During normal Write or Read modes the PRNG's clock is enabled. The user has the option to not scramble and descramble the User Data by not generating PRN's with the PRNG. When this option is chosen, the PRNG remains set at all 1's throughout the User Data fields, and the scrambler and descrambler circuitries simply buffer the User Data in both the write path and the read path.

### 8/9 (0, 4, 4) ENCODER / DECODER

In order to provide for good partial response maximum likelihood (PRML) signaling and detection in the recording channel, a Run Length Limited (RLL) code of parameters (0, 4, 4) is being provided.

As 8-bit data words are being provided for recording, the simplest (0, 4, 4) RLL code for 8-bit words is to use a set of qualified 9-bit code words. There are 279 qualified 9-bit code words (out of the 512 possible 9-bit words). Only 256 of these are required to encode the 8-bit data word. This is known as an 8/9 code.

Circuitry has been designed to provide for both encoding and decoding the 8-bit data words. The code-word to data-word assignments have been made to minimize both logic delay and chip area; the 256 codewords out of the 279 valid codewords were chosen so as to be able to realize encoder and decoder logic circuitry in the simplest and fastest means possible. A maximum of five gate delays through the encoder and through the decoder have been realized.

### PARALLEL-TO-SERIAL AND SERIAL-TO-PARALLEL CONVERTERS

One of the main features of the VM65020 is the parallel to serial conversion of 8-bit parallel NRZ data into a high speed serial bit stream, and the serial to parallel conversion of high speed serial data back to 8-bit parallel NRZ data. In write operations a 9-bit word is loaded in parallel onto the high speed serial write data bit stream every ninth channel clock cycle (every eighth in direct test) and then shifted out the SWD pins. In read *operations nine bits of the high speed read data bit stream are captured in parallel every ninth channel clock cycle (every eighth* in direct test) and then passed toward the NRZ pins.

The coordination of these transfers is timing-critical. In write operations, the transfer takes place as a parallel load of a serial shift register for a single channel clock cycle during the second half of the internal NRZ write clock period. This allows the parallel data plenty of time to have settled prior to its parallel loading into the serial shift register of the high speed write data bit stream.

In read operations, the transfer only takes place following a successful SYNC Byte word detection so that the RCLK will have been synchronized with the user data word boundaries. Once synchronization of the clock has been achieved, the user data is captured in 9-bit segments once every ninth cycle and made available to the decoder, descrambler, and NRZ output pins. In direct test the user data is captured in 8-bit segments once every eighth cycle and bypasses the decoder and descrambler on its way to the NRZ output pins.

### SYNC BYTE DETECTOR, PROGRAMMABLE

Detection of a SYNC Byte word in read mode is used to set the framing of the user data field into user data words that can then be passed on to the disk controller. The VCO Sync field, which precedes the SYNC Byte words, is searched at the beginning of read mode by the SYNC Byte detector circuitry. It is looking for either of the two SYNC Byte words to come along in the serial data stream so that the proper data word framing, or boundaries, can be determined and set.

In normal operation, the SYNC Byte words are two 9-bit words separated by a 9-bit spacer word, while in direct test operation they are the combination of 8-bit SYNC Byte words and the last bit of the VCO Sync Field, '1', for SB1 and the last bit of the 8-bit spacer word, '0', for SB2. The 9-bit SYNC Byte pattern for which to search is stored in the control register. This pattern is for the second SYNC Byte word, SB2, while the pattern for SB1 is the bit-by-bit inverse of SB2.



Upon detecting either SB1 or SB2 in the serial bit stream, a synchronization signal is passed on to the channel clock divider circuitry so that the divided clock can be adjusted for framing the user data word boundaries. Also, a blocking signal is set that stops the detector circuitry from continuing to search for and detecting subsequent patterns that also match the SYNC Byte patterns. In addition, a SYNC Byte Flag is set and eventually driven out on the SBF pin.

If the SYNC Byte detector circuitry fails to detect either SYNC Byte pattern as it passes through in the serial data stream, possibly due to a corrupted bit stream, the search is allowed to continue until the end of the read mode during which a possible false detection of user data patterns as the SYNC Byte words might occur. Acknowledging the failure to detect the SYNC Byte during the proper portion of the Read Mode is left up to the Controller chip.

The user has the option of requiring patterns SB1 and SB2 to both be detected prior to the passing of user data words to the disk controller. This is so the user can require tighter error tolerances during the SYNC Byte zone (i.e. that both SYNC Bytes must be error free, rather than just one).

The user also has the option to forego SYNC Byte detection and framing altogether. In this option the serial bit stream is not *searched for the SB1 and SB2 patterns. And thus the RCLK is* not synchronized to anything and the serial bit stream is simply captured in sequential eight bit sections and passed out to the NRZ pins. This is intended as a 'last resort' option when the serial bit stream is so corrupted that SYNC Byte words can not be detected for use in framing.

### CHANNEL CLOCK DIVIDER

The base (or channel rate) clock for the write or read operations comes from the frequency synthesizer (or timing recovery) in the VM65014. This clock enters the VM65020 on the Serial Read Clock (SRC) pins and is used to strobe Serial Read Data (SRD) from the VM65014 into the VM65020. The maximum frequency for this clock is beyond 202.5MHz (which is 9/8 x 180Mbit/sec, where 180Mbit/sec is the NRZ bit rate or frequency). This same clock is echoed by the VM65020 during write mode operations as the Serial Write Clock (SWC) to strobe Serial Write Data (SWD) out of the VM65020 and into the VM65014.

The minimum pulse width (high or low) for RCLK in byte mode is four channel rate clock periods, regardless of whether the chip is in normal operational mode or direct test mode, or whether RCLK is free running or synchronizing up to the SYNC Byte words. In Direct Test (÷ 8) both high and low pulses of RCLK are four channel rate clock periods. In normal operation (÷ 9) the high pulse remains at four while the low pulse is expanded out to five channel rate clock periods.

For nibble mode the minimum pulse width (high or low) for RCLK in byte mode is two channel rate clock periods. This, too, is regardless of whether the chip is in normal operational mode or direct test mode, or whether RCLK is free running or synchronizing up to the SYNC Byte words. In Direct Test both high and low pulses of RCLK are two channel rate clock periods. In normal operation the low pulses remain at two while the high pulses alternate between two and three channel rate clock periods. Thus the normal nibble clock period alternates between four and five channel clock periods just like the normal byte clock pulses alternate between four high and five low.

The NRZ read clock, RCLK, is used to strobe parallel NRZ data out of the VM65020 to the disk controller on the falling edge. This same clock is used to strobe parallel NRZ data into the VM65020. Either edge of the RCLK output can be selected and used to accommodate for phase delays either in the controller chip or in the NRZ interconnect lines. Also, an 'echo' of the RCLK output, supplied back to the WCLK input, can be used to strobe NRZ data in using the WCLK input's rising edge.

When synchronization occurs at a SYNC Byte word, either the low or the high pulse of one RCLK period is expanded per the diagrams below. Short pulse glitches during synchronization are thus not allowed to happen. See RCLK Synchronization Cases (Byte-Wide)below and "RCLK Synchronization Cases (Nibble-Wide)" on page 63.

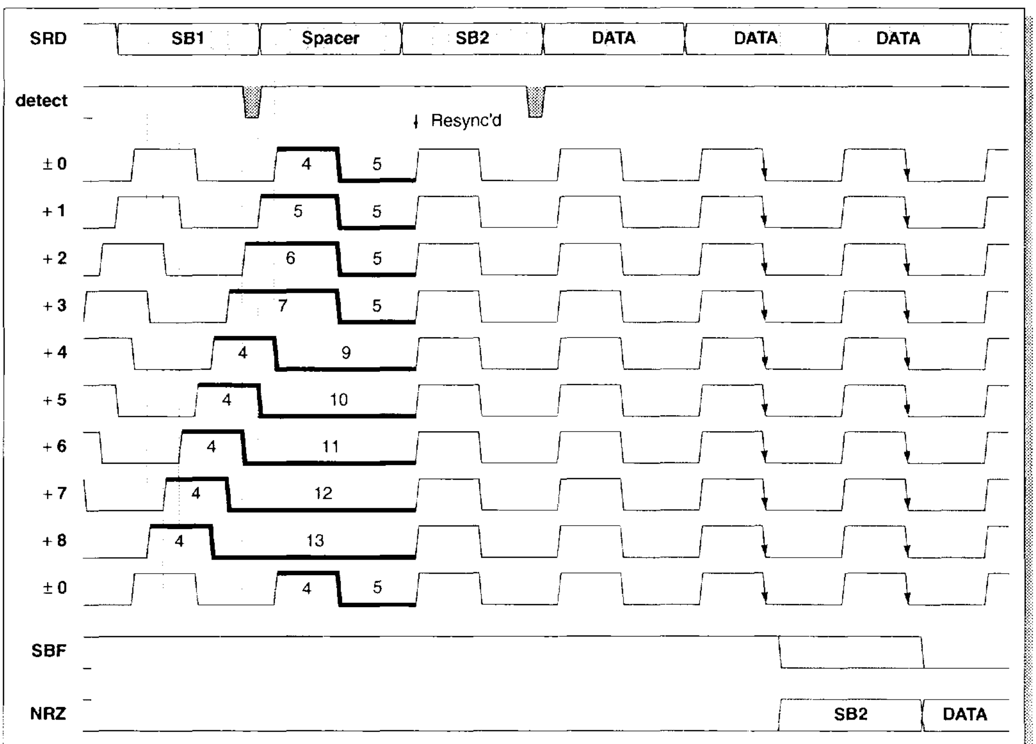


**Diagram 3a RCLK Synchronization Cases (Byte-Wide)**

READ CHANNEL CIRCUITS

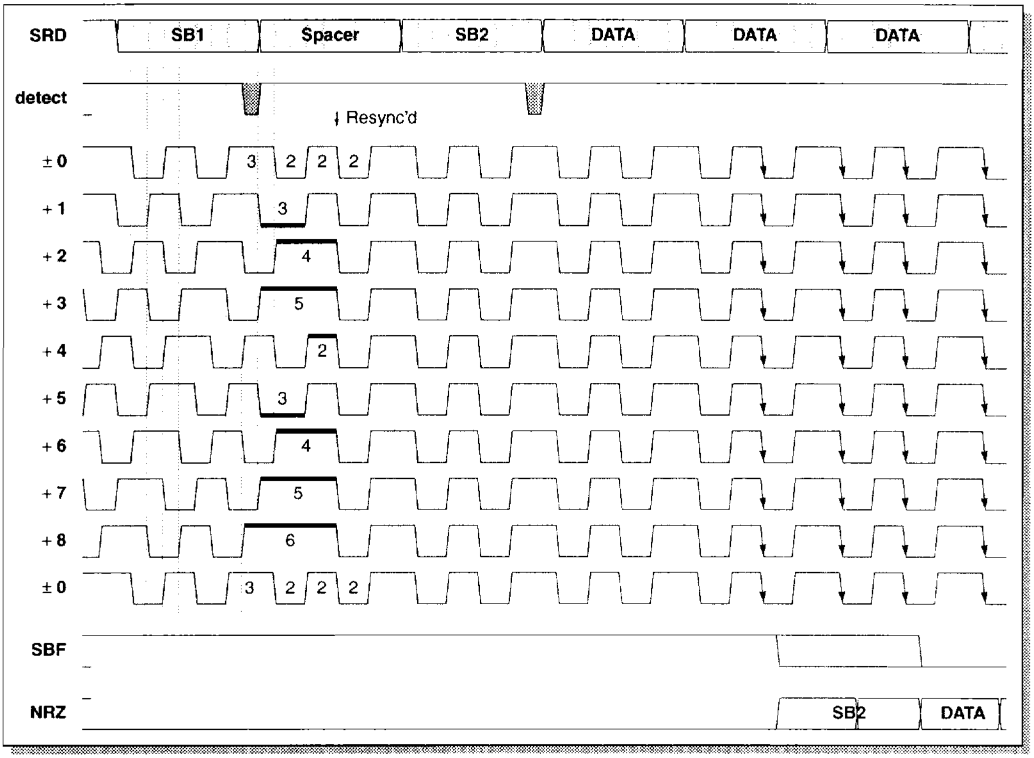


**Diagram 3b RCLK Synchronization Cases (Nibble-Wide)**

The channel clock divider circuitry consists of a 4-bit counter that rolls over after either eight or nine clock cycles, depending on the setting of the DT bit in the serial control register. The roll over, or clearing, of the counter is based on the established count length or on the detection of a SYNC Byte word. When a SYNC Byte word is detected, the counter is cleared regardless of where it is in the count. The RCLK is created through the use of a synchronous set/reset flip-flop with setting and resetting based on various decoded count values of the counter. The use of this flip-flop is what allows the elimination of any clock glitches during synchronization. The clearing of the counter due to the detection of a SYNC Byte words may cause either a second reset to follow an earlier reset resulting in an extended low pulse, or a second set to follow an earlier set resulting in an extended high pulse. There is no case where either pulse would be shortened due to synchronization.

The clock divider circuitry also creates the pulses used to control the parallel-to-serial and the serial-to-parallel transfers of data. These pulses are framed up with the incoming NRZ data words (with the first non-zero word) for write operations, and with the SYNC byte words for read operations.

## WCLK INPUT

The WCLK input provides an optional input strobe for parallel NRZ data being written into the VM65020. The rising edge of this input is used as the strobing edge. The Control Register bit EXT is used to select the WCLK option. The signal sent to the WCLK input must be a copy, or echo, of the RCLK output. An externally- generated signal replicating the RCLK frequency is not acceptable. The RCLK output itself may be tied back into the WCLK input, but a more common practice is for the RCLK output to drive into a controller chip, used there to strobe out NRZ data, and then sent back to the VM65020, along with the NRZ data, as the WCLK signal.

## TCIN INPUT

In order to synchronize testing of the VM65020, the Clock DIvider circuitry needs to be initialized to a known starting point and then released. The Control Register bit VTC2 can be used for this purpose. But this requires writing this bit twice. An alternate method is provided via the TCin input pin. A '1' on TCin initializes the clock divider, and a falling edge releases it to respond to SRC clock pulses.

## MODE CONTROLLER AND SEQUENCE CONTROLLERS

Four signal pins and three control register bits guide and determine the main operations of the VM65020. The pins are Servo Gate (SG), Read Gate (RG), Write Gate (WG), and Power Down (PD). The control register bits are Direct Test Mode (DTM), No Scramble (NOPR), and Sleep (SLP).

SG=X RG=X WG=X PD=X SLP bit =1

- Power Down Mode [PDM]
  - CML logic[2] off
  - NRZ, SG, RG, WG inputs disabled
  - NRZ outputs tristated

⇒ Can exit this PDM only by changing SLP bit to '0'.
This should be done with SG=0, RG=0, & WG=0, i.e. into Idle Mode

SG=X RG=X WG=X PD=1 SLP bit =0

- Power Down Mode [PDM]
  - CML logic off
  - NRZ, SG, RG, WG inputs disabled
  - NRZ outputs tristated

⇒ Should exit PDM only with SG=0, RG=0, & WG=0, i.e. into Idle Mode

SG=0 RG=0 WG=0 PD=0 SLP bit =0

- Idle Mode [IM]
  - CML logic on
  - Sequencers initialized but disabled, i.e. not running
  - PRNG initialized but disabled, i.e. not running
  - NRZ inputs disabled
  - NRZ outputs tristated

SG=1 RG=X WG=X PD=0 SLP bit =0

- Servo Mode [SM](SM ≡ IM for the VM65020)
  - CML logic on
  - Sequencers initialized but disabled, i.e. not running
  - PRNG initialized but disabled, i.e. not running
  - NRZ inputs disabled
  - NRZ outputs tristated
  - ⇒Should exit SM only with RG=0, & WG=0, i.e. into Idle Mode

SG=0 RG=1 WG=X PD=0 SLP bit =0

- Read Mode [RM]
  - CML logic on
  - NRZ outputs enabled, initially driving low
  - PRNG ready and waiting for enable upon SBF, uses RCLK
  - NRZ inputs disabled
  - ⇒Should exit RM only with SG=0, & WG=0, i.e. into Idle Mode
  - ⇒Should enter RM only with SG=0, & WG=0, i.e. from Idle Mode

SG=0 RG=0 WG=1 PD=0 SLP bit =0

- Write Mode [WM]
  - CML logic on
  - PRNG ready and waiting for enable upon NZD, uses internal WCLK (RCLK ↑ or RCLK ↓ )
  - NRZ inputs enabled
  - NRZ outputs tristated

⇒ Should exit WM only with SG=0, & RG=0, i.e. into Idle Mode
⇒ Should enter WM only with SG=0, & RG=0, i.e. from Idle Mode

[2] CML (Current Mode Logic) circuitry consists of the Parallel-to-Serial, Serial-to-Parallel, SYNC Byte Detector, Channel clock divider, and associated circuitry.



 

As seen above, the Sleep bit (SLP), when set to a '1', has the effect of overriding the four controlling pins. On the other hand, the No Scramble (NOPR), and Direct Test Mode (DTM) bits only modify the performance and operations within the various modes.

In byte operations (NIB=0) whenever DTM=0 the clock divider circuitry divides the serial channel clock, SRC, frequency by nine to create RCLK. And whenever DTM=1 the division is changed to eight.

Whenever DTM=1, the PRNG circuitry is disabled, regardless of the value of NOPR. Whenever DTM=0, the enabling of the PRNG is dependent upon the value of NOPR, with NOPR=1 providing a disable and NOPR=0 providing an enable.

The following diagram shows, in state diagram form, the three operational modes of the VM65020. These modes are Idle / Servo mode, Read mode, and Write mode. Note that Idle and Servo modes are one and the same for the VM65020. This is not the case for the analog PRML channel chip, VM65014. Also shown are the transitions between these modes. The usual and intended transitions are shown with the heavy arrows and control settings in bold. Other possible valid but less standard transitions are shown with dotted arrows.

These transitions are set via the hierarchy: SG overrides RG which overrides WG. These inputs are, by nature, all asynchronous. But there is a relationship between WG input, NRZ input, and the active clock write strobe edge, be it WCLK, RCLK rising, or RCLK falling. The first two input write clock edges following WG rising, or whichever signal put the chip into Write mode, are the two NRZ inputs that are ignored and assumed to be zero, whereas the third clock edge actually strobes in the NRZ inputs that are first checked for non-zero patterns.

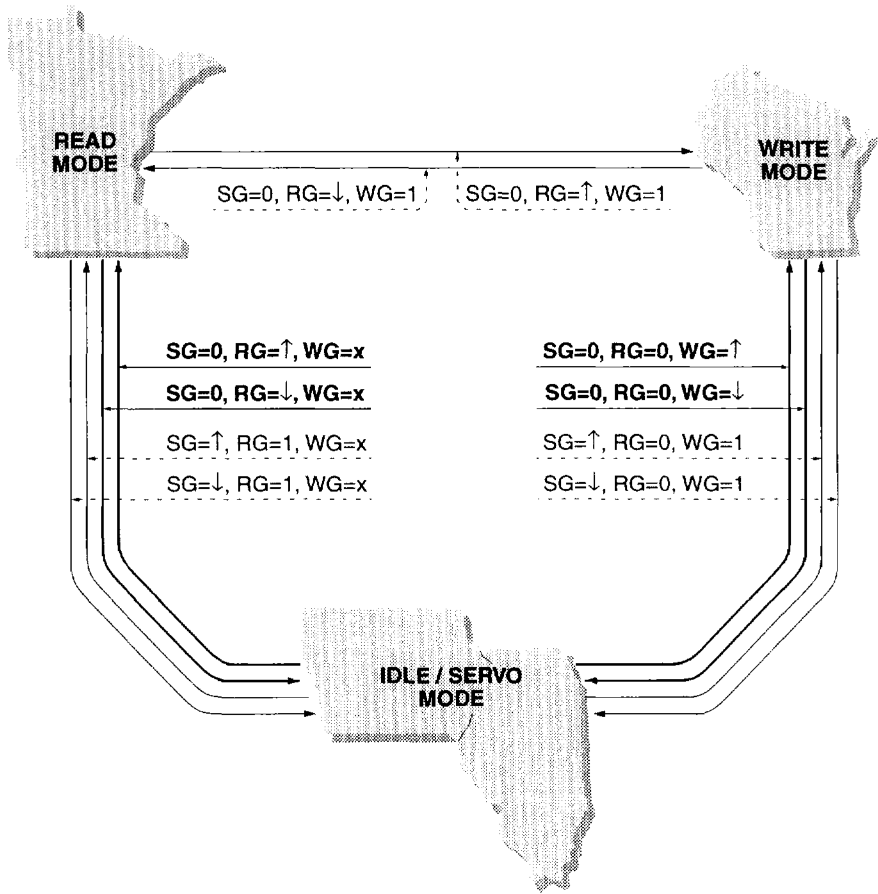


**Diagram 4 State Diagram of Mode Transitions**

## SERIAL CONTROL REGISTER

Control of the chip is performed through a serial digital interface and a two-word, 12-bit wide register file. Control information is stored in the register file and used directly as digital control lines. The interface consists of three CMOS-level signals for input/output data, clock, and enable. Upon asserting SPEN, the serial port is enabled and ready for input on SPDATA and SPCLK. The SPDATA line provides the read/write, address and data information.

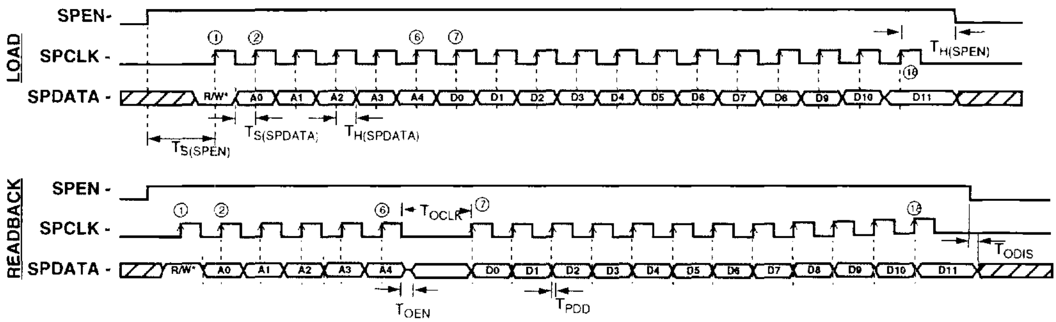


**Diagram 5 Serial Port Write and Readback Operations**

A serial port, consisting of a serial clock pin SPCLK, a serial data pin SPDATA, and a serial enable pin SPEN, allows the programming of internal control registers which control the operation of the VM65020. The data is organized into two 12-bit registers addressed with a 5-bit address. Upon assertion of the SPEN pin, data is transferred into the chip (or out of the chip for a readback) on the SPDATA pin synchronously with the SPCLK pin. The serial data transfer sequence is as follows:

- 1 R/W bit
- 5 Address bits
- 12 Data bits

For either the case of loading the bits or reading them back, the R/W and five address bits must be loaded into the chip. If the R/W bit is a '0', then a load takes place and the 12 data bits corresponding to the 5-bit address are immediately serially loaded into the chip. On the falling edge of the SPEN signal, the 12 data registers are latched into the appropriate register for storage. If the R/W bit is a '1' then a readback takes place. After the five address bits are loaded, followed by a longer $6^{th}$ clock pulse, the SPDATA signal is driven by the VM65020 and the 12 bits in the register corresponding to the five address bits are serially shifted out of the chip on the rising edges of SPCLK. The falling edge of the SPEN signal disables the VM65020's SPDATA output driver.

The assignments for the two 12-bit control registers in the VM65020 are shown in Table 1.

| ADDRESS | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $10000_B$ | VTC3 | VTC2 | SB9 | SB8 | SB7 | SB6 | SB5 | SB4 | SB3 | SB2 | SB1 | VTC1 |
| $10001_B$ | DTM | NONE | BOTH | rsrv'd | rsrv'd | rsrv'd | EXT | SBRT | EDGE | NOPR | NIB | SLP |

**Table 1 Control Register Bit Assignments**

The various Control Register bits are defined as below.

- VTC1 — VTC internal test control: 4x Output Current (when = '1') [3]
- VTC2 — VTC internal test control: Initialize Clock Maker Circuitry (when = '1') [3]
- VTC3 — VTC internal test point monitor: PRN10( = '0') or NZD (='1')
- SB[9:1] — SYNC Byte #2 Pattern, 9-bit encoded format
- SLP — Sleep (='1') or Awake (='0') mode [Power Up or Power Down]
- NIB — Nibble (='1') or Byte (='0') mode [8-bit or 4-bit NRZ Interface]
- NOPR — PRNG Not Running (='1') or Running (='0') [to not Scramble or to Scramble]
- EDGE — RCLK ↓ edge (='1') or RCLK ↑ edge (='0') used for NRZ Input Strobe
- SBRT — SYNC Byte #2 Pattern Returned (='1') or Not Returned (='0') prior to User Data
- EXT — External WCLK ↑ edge (='1') or internal RCLK (='0') used for NRZ Input Strobe
- BOTH — Both (='1') or Either (='0') Sync Byte(s) must be found
- NONE — RG (='1') or Sync Byte(s) (='0') used for Readback Framing
- DTM — Direct Test mode (='1') or Normal mode(='0') mode [8-bit Clear or 9-bit Encoded]
- rsrv'd — VTC Reserved Control Bit [3]

[3] User must set and leave this bit low, bit = '0'

## INPUT, OUTPUT, AND SUPPLY PINS

There are a number of different input and output buffers used on this chip. There are CMOS TTL inputs, outputs, and bidirectionals, and special Current Mode differential inputs and outputs. A table showing the various pin types is provided in Table 2 below.

| PIN TYPE | PIN NAME | # | INFORMATION |
|---|---|---|---|
| Power Supplies | VCCM | 24, 36 | CMOS 5.0V Logic Supply |
| | VCCP | 23, 37 | CMOS 5.0V Tub Supply |
| | VCCB | 5 | Bipolar 5.0V Logic Supply |
| Ground Supplies | VSSM | 22, 35 | CMOS 0.0V Logic Supply |
| | VSSB | 4 | Bipolar 0.0V Logic Supply |
| | VEEM | 17, 38 | CMOS 0.0V Substrate Supply |
| | VEEB | 1, 12 | Bipolar 0.0V Substrate Supply |
| CMOS TTL Inputs | PD | 41 | Power Down |
| | SG | 44 | Servo Mode Gate |
| | RG | 42 | Read Mode Gate |
| | WG | 43 | Write Mode Gate |
| | WCLK | 30 | NRZ Write Clock |
| | SPEN | 39 | Serial Control Register Port Enable |
| | SPCLK | 40 | Serial Control Register Port Clock |
| CMOS TTL Outputs | RCLK | 29 | NRZ Read Clock |
| | SBF | 33 | SYNC Byte Flag |
| CMOS TTL Bidirectionals | NRZ[8:1] | 28-25<br>21-18 | NRZ Parallel Read/Write Data<br>( For Nibble NRZ[4:1] are used & NRZ[8:5] are tied off ) |
| | SPDATA | 34 | Serial Control Register Port Read/Write Data |
| Current Mode Differential Inputs | SRCP / N | 6 / 7 | Serial Read Clock (pos & neg) |
| | SRDP / N | 2 / 3 | Serial Read Data (pos & neg) |
| Current Mode Differential Outputs | SWCP / N | 10 / 11 | Serial Write Clock (pos & neg) |
| | SWDP / N | 8 / 9 | Serial Write Data (pos & neg) |

| | | | |
|---|---|---|---|
| VTC Reserved Pins [ CMOS TTL inputs and/or outputs ] | reserved | 31 | TCin: Test Control input - Initialize Clockmaker |
| | reserved | 32 | TPout: Test Point monitor output - NZD or PRN10 |

**Table 2 Pin Type Groupings**

READ CHANNEL CIRCUITS

## PIN / FUNCTION LIST AND DESCRIPTION

| ## | NAME | DESCRIPTION | | ## | NAME | DESCRIPTION |
|---|---|---|---|---|---|---|
| 1 | VEEB | 0.0V Bipolar Substrate | | 25 | NRZ5 | $5^{th}$ bit NRZ Data |
| 2 | SRDP | Serial Read Data (pos) | | 26 | NRZ6 | $6^{th}$ bit NRZ Data |
| 3 | SRDN | Serial Read Data (neg) | | 27 | NRZ7 | $7^{th}$ bit NRZ Data |
| 4 | VSSB | 0.0V Bipolar Supply | | 28 | NRZ8 | $8^{th}$ bit NRZ Data |
| 5 | VCCB | 5.0V Bipolar Supply | | 29 | RCLK | NRZ Read Clock |
| 6 | SRCP | Serial Read Clock (pos) | | 30 | WCLK | NRZ Write Clock |
| 7 | SRCN | Serial Read Clock (neg) | | 31 | reserved | control test point [a] |
| 8 | SWDP | Serial Write Data (pos) | | 32 | reserved | monitor test point [b] |
| 9 | SWDN | Serial Write Data (neg) | | 33 | SBF | Sync Byte Flag |
| 10 | SWCP | Serial Write Clock (pos) | | 34 | SPDATA | Serial Port Data |
| 11 | SWCN | Serial Write Clock (neg) | | 35 | VSSM | 0.0V CMOS Supply |
| 12 | VEEB | 0.0V Bipolar Substrate | | 36 | VCCM | 5.0V CMOS Supply |
| 13 | nc | no connect | | 37 | VCCP | 5.0V CMOS Tub |
| 14 | nc | no connect | | 38 | VEEM | 0.0V CMOS Substrate |
| 15 | nc | no connect | | 39 | SPEN | Serial Port Enable |
| 16 | nc | no connect | | 40 | SPCLK | Serial Port Clock |
| 17 | VEEM | 0.0V CMOS Substrate | | 41 | PD | Power Down |
| 18 | NRZ1 | $1^{st}$ bit NRZ Data | | 42 | RG | Read Gate |
| 19 | NRZ2 | $2^{nd}$ bit NRZ Data | | 43 | WG | Write Gate |
| 20 | NRZ3 | $3^{rd}$ bit NRZ Data | | 44 | SG | Servo Gate |
| 21 | NRZ4 | $4^{th}$ bit NRZ Data | | 45 | nc | no connect |
| 22 | VSSM | 0.0V CMOS Supply | | 46 | nc | no connect |
| 23 | VCCP | 5.0V CMOS Tub | | 47 | nc | no connect |
| 24 | VCCM | 5.0V CMOS Supply | | 48 | nc | no connect |

a. User to tie this pin Low
b. User to "no connect" this pin

## ELECTRICAL PARAMETERS

AC and DC CHARACTERISTICS: Recommended operating conditions apply unless otherwise specified

| PARAMETER | SYM | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Power Supply Current | $I_{CC}$ | Read Mode, Data Rate=140Mbps | | | <TBD> | mA |
| | | Read Mode, Data Rate=180Mbps | | | <TBD> | mA |
| | | Write Mode, Data Rate=140Mbps | | | <TBD> | mA |
| | | Write Mode, Data Rate=180Mbps | | | <TBD> | mA |
| | | Idle Mode, Data Rate=140Mbps | | | <TBD> | mA |
| | | Idle Mode, Data Rate=180Mbps | | | <TBD> | mA |
| | | Powerdown Mode | | | <TBD> | mA |

## LOGICAL SIGNALS; TTL DIGITAL PINS

| PARAMETER | SYM | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Input High Voltage | $V_{IH}$ | | 2.0 | | $V_{CC} + 0.3$ | V |
| Input Low Voltage | $V_{IL}$ | | –0.3 | | 0.8 | V |
| Input Leakage Current | $I_{IL}$ | $V_{IL} = 0.8V$ | | | ±10 | µA |
| | $I_{IH}$ | $V_{IH} = 2.0V$ | | | ±10 | µA |
| Output High Voltage | $V_{OH}$ | $I_{OH} = 4mA$ | 2.7 | | | V |
| Output Low Voltage | $V_{OL}$ | $I_{OL} = 4mA$ | | | 0.5 | V |
| Output Leakage Current | $I_{OZ}$ | Output Disabled | | | ±10 | µA |
| Input Capacitance | $C_{IN}$ | CMOS Input only pins | | | 10 | pF |
| Output Capacitance | $C_{OUT}$ | CMOS Output or Bidirectional pins | | | 10 | pF |

## TIMING PARAMETERS

AC CHARACTERISTICS: Recommended operating conditions apply unless otherwise specified

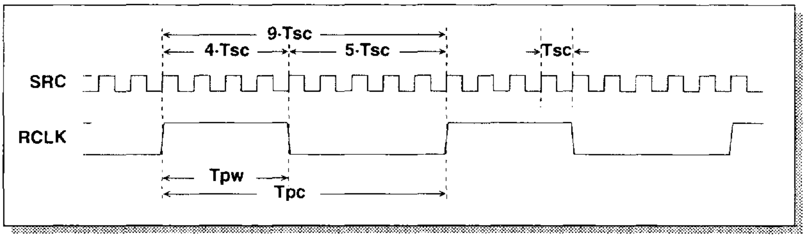


Diagram 6a Byte-Wide RCLK with respect to SRC, Normal

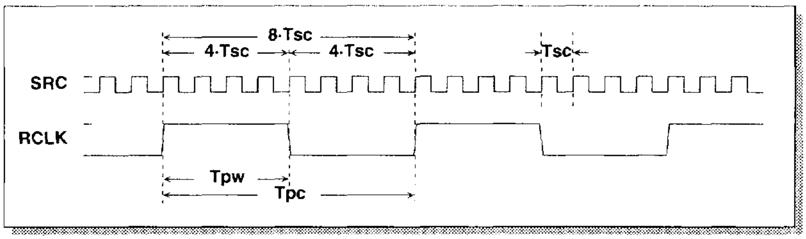


Diagram 6b Byte-Wide RCLK with respect to SRC, Direct Test

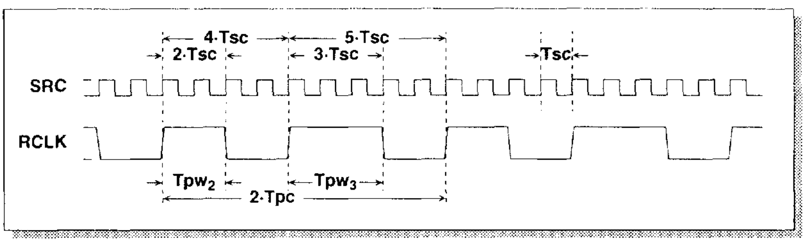


Diagram 6c Nibble-Wide RCLK with respect to SRC, Normal

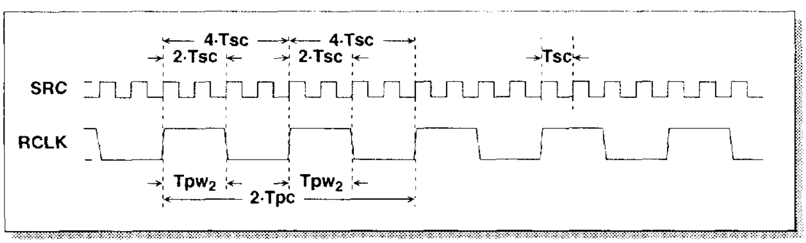


Diagram 6d Nibble-Wide RCLK with respect to SRC, Direct Test

| PARAMETER | SYM | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Channel Clock Frequency | $f_{chclk}$ (max) | Data Rate=140Mbit/s | 157.5 | | | MHz |
| | | Data Rate=180Mbit/s | 202.5 | | | MHz |
| Parallel Read Clock Frequency | $f_{RCLK}$ (max) | Control Reg Bit DTM=0; Byte-wide | 17.5 | $1/9 \cdot f_{chclk}$ | | MHz |
| | | Control Reg Bit DTM=1; Byte-wide | 19.7 | $1/8 \cdot f_{chclk}$ | | MHz |
| Serial Channel Clock Period | $T_{SC}$ (min) | Data Rate=140Mbit/s | | | 6.35 | ns |
| | | Data Rate=180Mbit/s | | | 4.94 | ns |
| Parallel Read Clock Pulse Width | TPW | at 1.5V points; $C_L \leq 15pF$ | $4 \cdot T_{SC} - x$ | | $4 \cdot T_{SC} + x$ | ns |
| | TPW2 | at 1.5V points; $C_L \leq 15pF$ | $2 \cdot T_{SC} - x$ | | $2 \cdot T_{SC} + x$ | ns |
| | TPW3 | at 1.5V points; $C_L \leq 15pF$ | $3 \cdot T_{SC} - x$ | | $3 \cdot T_{SC} + x$ | ns |
| Parallel Read Clock Period | $T_{PC}$ | Byte-wide, Normal Operation | $9 \cdot T_{SC}$ | $9 \cdot T_{SC}$ | $9 \cdot T_{SC}$ | ns |
| | | Byte-wide, Direct Test | $8 \cdot T_{SC}$ | $8 \cdot T_{SC}$ | $8 \cdot T_{SC}$ | ns |
| | $2 \cdot T_{PC}$ | Nibble-wide, Normal Operation | $9 \cdot T_{SC}$ | $9 \cdot T_{SC}$ | $9 \cdot T_{SC}$ | ns |
| | | Nibble-wide, Direct Test | $8 \cdot T_{SC}$ | $8 \cdot T_{SC}$ | $8 \cdot T_{SC}$ | ns |
| Control Signal rise and fall times | $t_{CS}$ | 20% to 80% | | | < 10 > | ns |
| Recovery time Powerdown to fully functional | $t_{REC}$ | | | | <TBD> | ns |

READ CHANNEL CIRCUITS

**PARALLEL WRITE**

Pins: WG, WCLK or RCLK, NRZ[8:1] or NRZ[4:1]

**Timing Diagrams:**

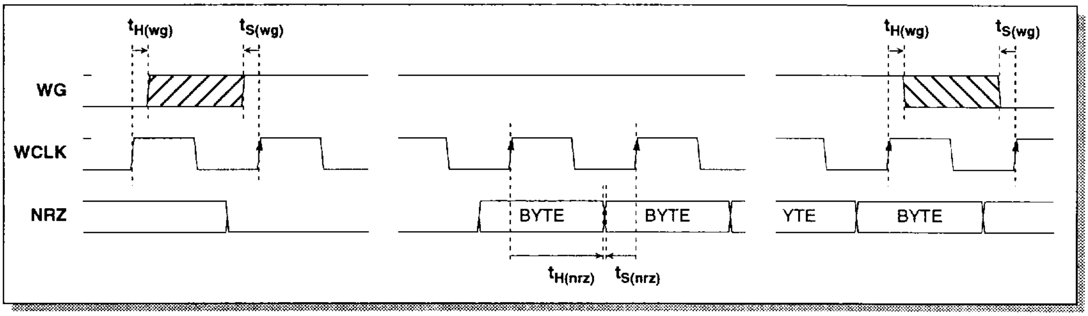


**Diagram 7a Parallel Write Timing: WCLK, Byte-Wide**

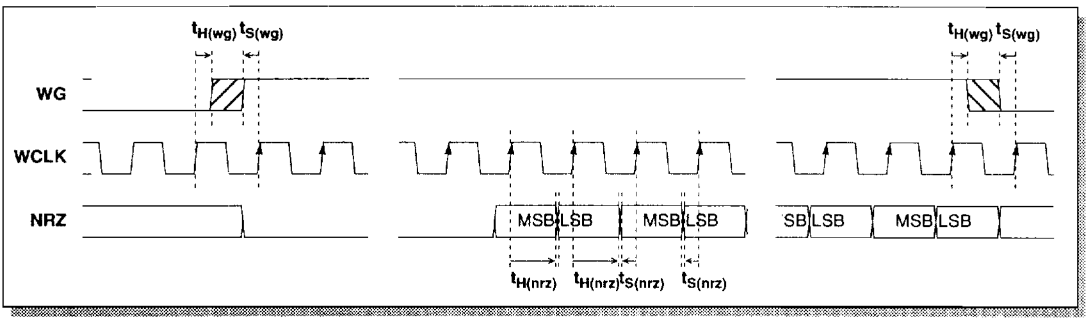


**Diagram 7b Parallel Write Timing: WCLK, Nibble-Wide**

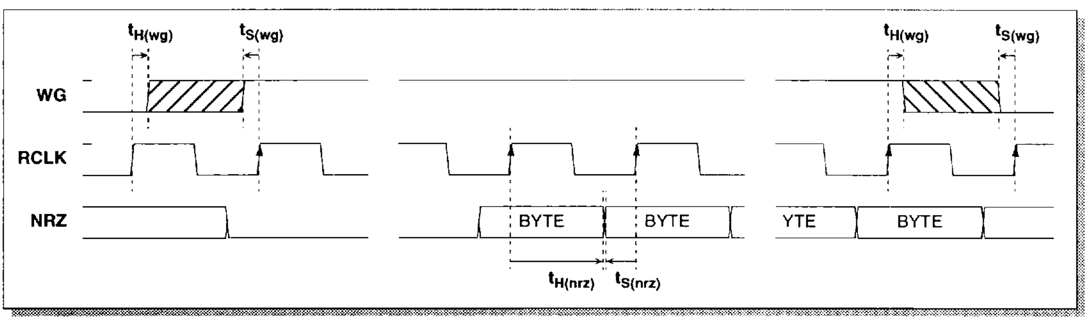


**Diagram 7c Parallel Write Timing: RCLK Rising Edge, Byte-Wide**

READ CHANNEL CIRCUITS

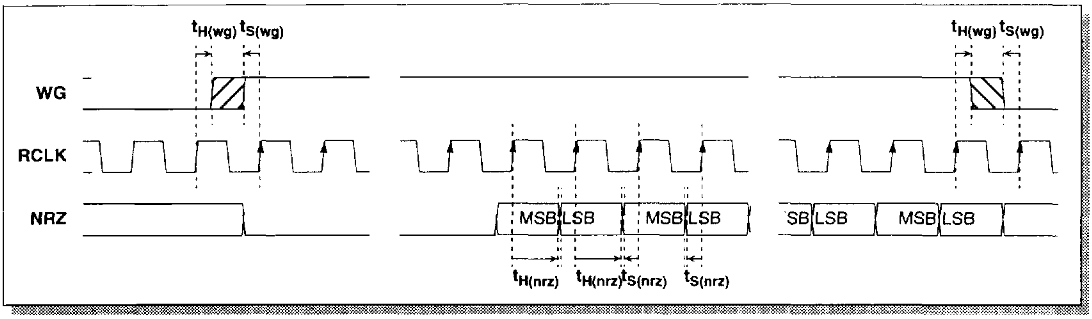


**Diagram 7d Parallel Write Timing: RCLK Rising Edge, Nibble-Wide**

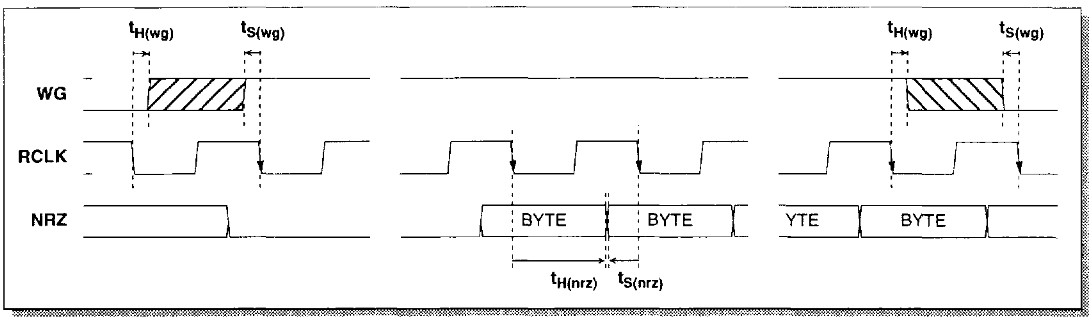


**Diagram 7e Parallel Write Timing: RCLK Falling Edge, Byte-Wide**

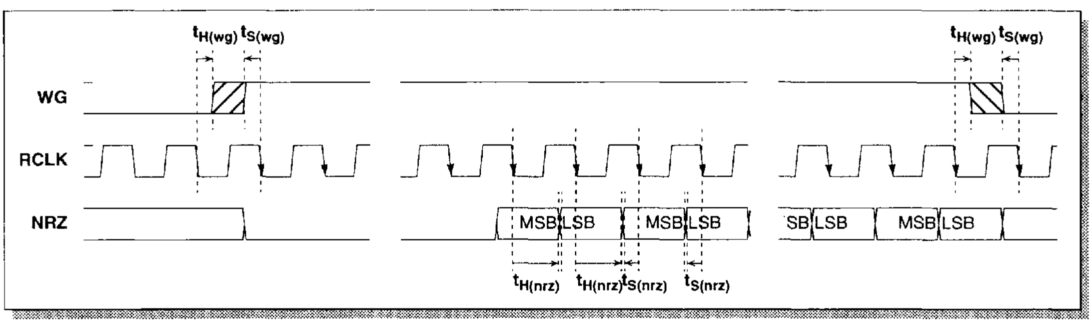


**Diagram 7f Parallel Write Timing: RCLK Falling Edge, Nibble-Wide**

| PARAMETER | SYM | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| WG Hold Time | $t_{H(wg)}$ | w.r.t. WCLK; at 1.5V points | <TBD> | | | ns |
| | | w.r.t. RCLK; at 1.5V points | <TBD> | | | ns |
| WG Setup Time | $t_{S(wg)}$ | w.r.t. WCLK; at 1.5V points | <TBD> | | | ns |
| | | w.r.t. RCLK; at 1.5V points | <TBD> | | | ns |
| NRZ Hold Time | $t_{H(nrz)}$ | w.r.t. WCLK; at 1.5V points | <TBD> | | | ns |
| | | w.r.t. RCLK; at 1.5V points | <TBD> | | | ns |
| NRZ Setup Time | $t_{S(nrz)}$ | w.r.t. WCLK; at 1.5V points | <TBD> | | | ns |
| | | w.r.t. RCLK; at 1.5V points | <TBD> | | | ns |
| $\overline{WM}$ time prior to WM | $t_{\overline{WM}}$ | $\overline{WM}$ = Idle mode or Read mode | <TBD> | | | ns |

## PARALLEL READ

Pins: RG, RCLK, SBF, NRZ[8:1] or NRZ[4:1]

**Timing Diagrams:**

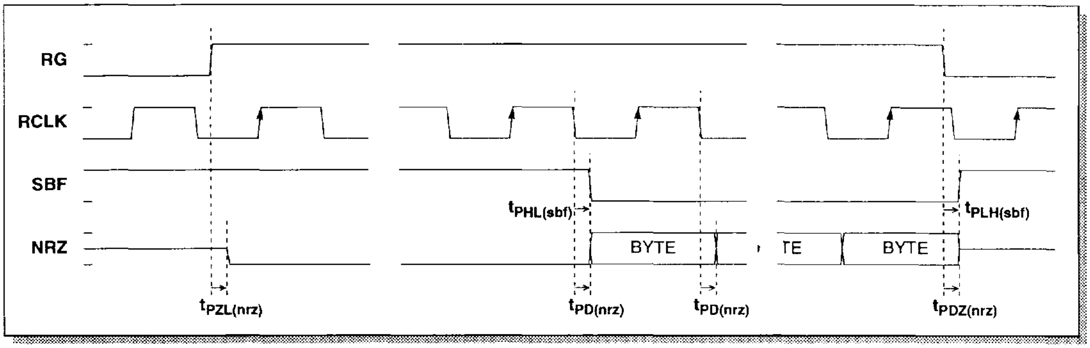


**Diagram 8a Parallel Read Timing: Byte-Wide**

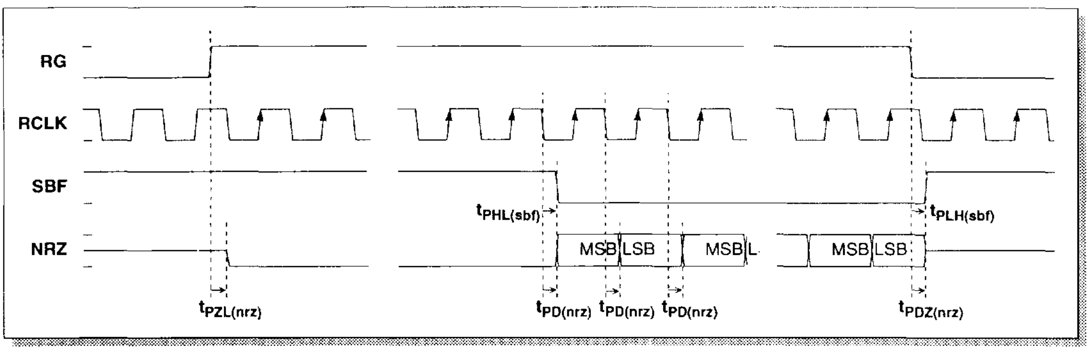


**Diagram 8b Parallel Read Timing: Nibble-Wide**

| PARAMETER | SYM | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| RCLK to SBF falling | $t_{PHL(sbf)}$ | measured at 1.5V points; $C_L \leq 15pF$ | | | <TBD> | ns |
| RG to SBF rising | $t_{PLH(sbf)}$ | measured at 1.5V points; $C_L \leq 15pF$ | | | <TBD> | ns |
| RG to NRZ enabled | $t_{PZL(nrz)}$ | measured at 1.5V points; $C_L \leq 15pF$ | | | <TBD> | ns |
| RCLK to NRZ change | $t_{PD(nrz)}$ | measured at 1.5V points; $C_L \leq 15pF$ | | | <TBD> | ns |
| RG to NRZ disabled | $t_{PDZ(nrz)}$ | measured at 1.5V points; $C_L \leq 15pF$ | | | <TBD> | ns |
| $\overline{RM}$ time prior to RM | t $\overline{RM}$ | $\overline{RM}$ = Idle mode or Write mode | <TBD> | | | ns |

## SERIAL PORT WRITE AND READ

Pins: SPEN, SPCLK, SPDATA

(See Timing Diagram 5 on page 66))

| PARAMETER | SYM | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| SPCLK Period | T | | < 50 > | | | ns |
| SPCLK High | $t_{high}$ | | < 15 > | | | ns |
| SPCLK Low | $t_{low}$ | | < 15 > | | | ns |
| SPCLK Low Time | $t_{OCLK}$ | Readback $6^{th}$ clock cycle | < 30 > | | | ns |
| SPEN Low Time | $t_{low}$ | Between Serial Port operations | < 50 > | | | ns |
| SPEN Setup Time | $t_{S(spen)}$ | | < 40 > | | | ns |
| SPEN Hold Time | $t_{H(spen)}$ | | < 50 > | | | ns |
| SPCLK to SPDATA | $t_{PD}$ | with respect to SPCLK $\uparrow$ | | | < 10 > | ns |
| SPDATA Setup Time | $t_{S(spdata)}$ | | < 5 > | | | ns |
| SPDATA Hold Time | $t_{H(spdata)}$ | | < 5 > | | | ns |
| SPDATA Enable | $t_{OEN}$ | | < 5 > | | | ns |
| SPDATA Disable | $t_{ODIS}$ | | | | < 30 > | ns |





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