

Notice: These are not a final specification. Some parametric limits are subject to change.

T-52-33-21

**DESCRIPTION**

M33245GS (M32/CCM) is a cache controller/memory for M32 family microprocessors (M33210GS-20, M33220GS-20, M33230GS-20).

It improves the MPU's average memory access time.

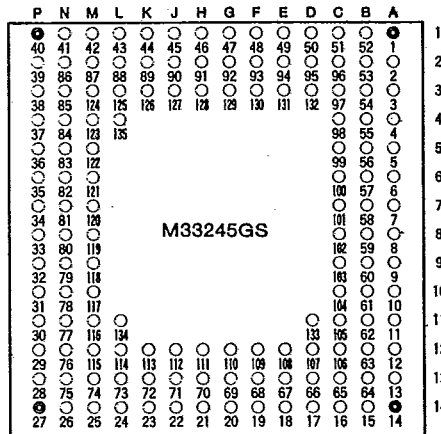
**FEATURES**

- 16kB real address external cache
- No wait reads possible when the cache is hit
- Fast 4 words burst read when the cache is missed
- Fully synchronous operation with M32 family processors
- Internal address comparator allows multiple usage
- Division into data cache and instruction cache
- Coherency maintained by address monitor
- Purge and freeze functions in way units
- Write-through main memory replace
- 4-way set associative cache
- LRU (Least Recently Used) replace control
- Each line consists of 4 words (16 bytes) and a validity bit
- Package : 135 pin PGA

**APPLICATION**

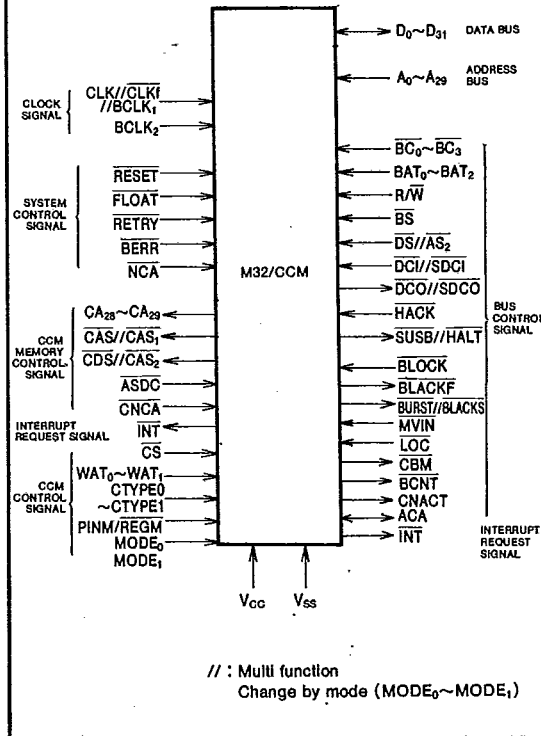
High performance cache memory system

**PIN CONFIGURATION (BOTTOM VIEW)**



Outline 135S8

**PIN FUNCTION**



Note. G<sub>MICRO</sub>™ is a trademark of the G-MICRO group for the TRON specification microprocessors.

CMOS CACHE CONTROLLER/MEMORY (M32/CCM)

BLOCK DIAGRAM

