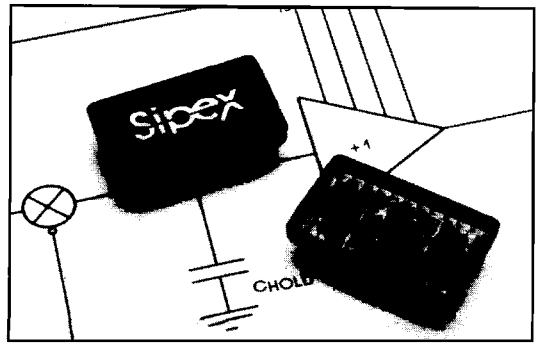
ULTRA HIGH SPEED 16-BIT ACCURATE, TRACK & HOLD AMPLIFIER

FEATURES

- 350 ηsec Acquisition Time to .005% for 20V step
  250 ηsec Acquisition Time to .005% for 10V step
- -94 dB Feedthrough Rejection Ratio (20V step)
- Low Aperture Uncertainty of 75 ρsec rms
- Excellent Linearity: ±.0005% for ±5V range
  ±.001% for ±10V range
- Low droop rate: 1V/sec
- Low distortion: -90 dB (5V p-p @ 100 kHz)
  -88 dB (20V p-p @ 10 kHz)



DESCRIPTION

The SP9760 is an ultra fast 16 bit linear sample-and-hold, featuring an acquisition time of 250 ηsec and 350 ηsec for 20V and 10V signal step respectively. The ultimate combination of speed, accuracy and stability is evidenced by low aperture uncertainty of 75 ρsec rms, 16 bit linearity, 30 MHz small signal bandwidth and maximum pedestal of ±1mV. Two proprietary Dielectric-Isolation-based ASICs are utilized in the design of the SP9760 to achieve true 16 bit performance at specified conversion rates.

The SP9760 accepts bipolar ±10V input signal, dissipates 825 mW and is available in the 24 pin dual-in-line package. The superior attributes of the SP9760 make it an ideal candidate to use in conjunction with a high speed14 to 16 bit ADC's in multiplexed data acquisition applications such as audio digitizing, ATE, industrial data acquisition and signal processing such as magnetic resonance imaging and radar.

Two temperature ranges are available. The SP9760C is guaranteed over a case temperature of 0°C to +70°C; the SP9760B is MIL-STD-883C screened over a temperature range of -55°C to +125°C.

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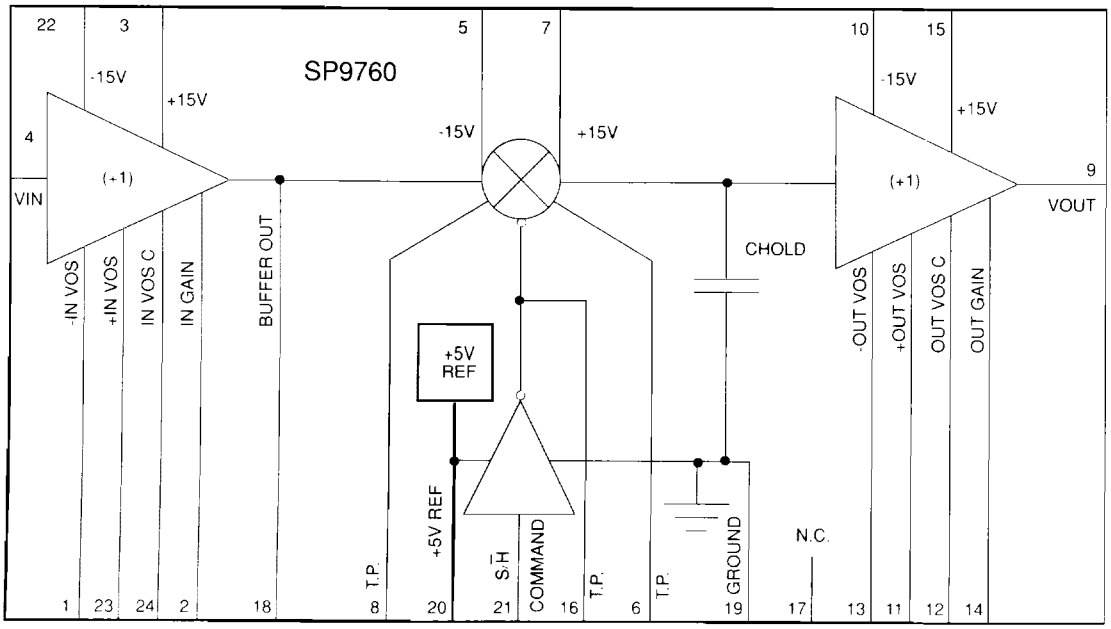
FUNCTIONAL DIAGRAM



SPECIFICATIONS

	SP9760C 0°C to 70°C			SP9760B (PRELIMINARY) -55°C to +125°C			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
ANALOG INPUT							
Input Voltage	±10			±10			V
Input Bias Current		100			100		pA
Input Impedance		100			100		MΩ
DIGITAL INPUT							
Logic "0"	0		0.8	0		0.8	V
Logic "1"	2.0		5.0	2.0		5.0	V
ANALOG OUTPUT							
Voltage	±10			±10			V
Current		20			20		mA
Impedance		.1			.1		Ω
Capacitive Load[1]							
SAMPLE MODE DC TRANSFER CHARACTERISTICS							
Offset Error		±1	±5		±5	±20	mV
Offset Drift		±20			±50	±200	µV/°C
Gain		+1			+1		
Gain Error		±.03	±.1		±.05	±.2	%FSR
Gain Drift		±2	±20		±2	±20	ppm/°C
Linearity							
20V Range		.001	.002		.001	.002	%FSR
10V Range		.0005			.0005		%FSR
SAMPLE MODE DYNAMICS							
Frequency Response							
Small Signal (-3 dB)		30			20		MHz
Full Power (20V p-p)		2			1		MHz
(10V p-p)		4			2		MHz
Slew Rate	75	120		40	60		V/µsec
Acquisition Time							
±20V Step to .0015%		350	500		600	700	nsec
±10V Step to .0015%		250			450		nsec
±5V Step to .01%		200			375		nsec
Distortion							
5V p-p @ 100 kHz		-90			-80		dB
20V p-p @ 10 kHz		-88			-78		dB
HOLD MODE DYNAMICS							
Pedestal Offset Error		±0.2	±1.0		±2	±5	mV
Pedestal Offset Drift		±30			±20	±50	µV/°C
Pedestal Gain Error		±.002			±.005	±.01	%FSR
Pedestal Linearity		±.0005	±.002		±.0005	±.002	%FSR
Droop Rate		±1	±100		±150	±1000	µV/µS
Feedthrough Rejection[2, 5]		-103	-90		-103	-90	dB
Dielectric Absorption[2]		.0005			.001		%FSR
Aperture Delay		30			30		nsec
Aperture Uncertainty		75			75		ps RMS
Sample to Hold Settling[3]		150			150		nsec
Noise[4]		300			300		µV RMS

SPECIFICATIONS

	SP9760C 0°C to 70°C			SP9760B (PRELIMINARY) -55°C to +125°C			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
POWER REQUIREMENTS							
Nominal Voltage							
$+V_S$		+15			+15		V
$-V_S$		-15			-15		V
Supply Current							
$+V_S$		31			31		mA
$-V_S$		24			24		mA
Power Dissipation		825			825		mW
Power Supply Rejection		100			100		µV/V
TEMPERATURE RANGE							
Operating		0 to +70			-55 to +125		°C
Storage		-40 to +85			-65 to +150		°C
ABSOLUTE MAXIMUM RATINGS							
$\pm V_S$			16			16	V
Analog Input	$-V_S$		$+V_S$	$-V_S$		$+V_S$	V
Digital Input	-1		+6	-1		+6	V
Junction Temp			150				°C
Θ_{JC}			30.3				°C/Watt

NOTES

1. $C_{load} < {}^{Iload}/_{(\partial V_{out}/\partial I_{out})}$. See recommendations on capacitive loading.
2. ±20V Step
3. To ±0.005%
4. DC to 30 MHz
5. Feedthrough rejection tested at 25°C.

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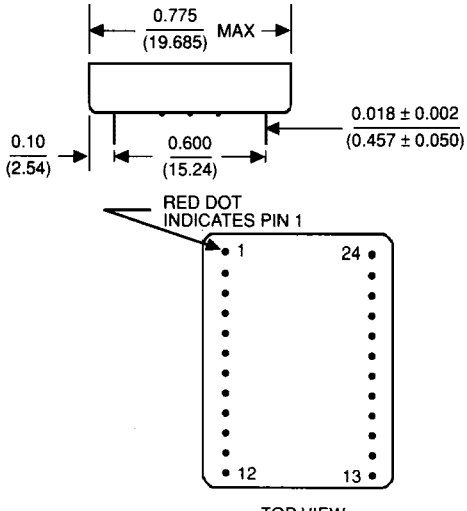
PIN ASSIGNMENTS

PIN	FUNCTION
1	-In V_{os}
2	In Gain
3	+15V
4	V_{in}
5	-15V
6	TP
7	+15V
8	TP
9	V_{out}
10	-15V
11	+Out V_{os}
12	Out V_{os} C
13	-Out V_{os}
14	Out Gain
15	+15V
16	TP
17	NC
18	Buffer Out
19	Ground
20	+5V Ref
21	S/$\overline{H}$ In
22	-15V
23	+In V_{os}
24	In V_{os} C

ORDERING INFORMATION

MODEL	TEMPERATURE RANGE	DESCRIPTION
SP9760C	0°C to 70°C	—
SP9760B	-55°C to +125°C	MIL-STD-883

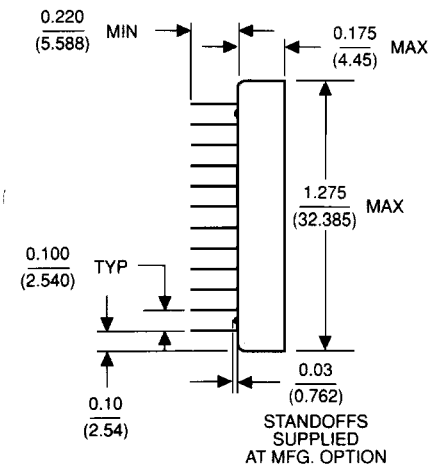
PACKAGE OUTLINE



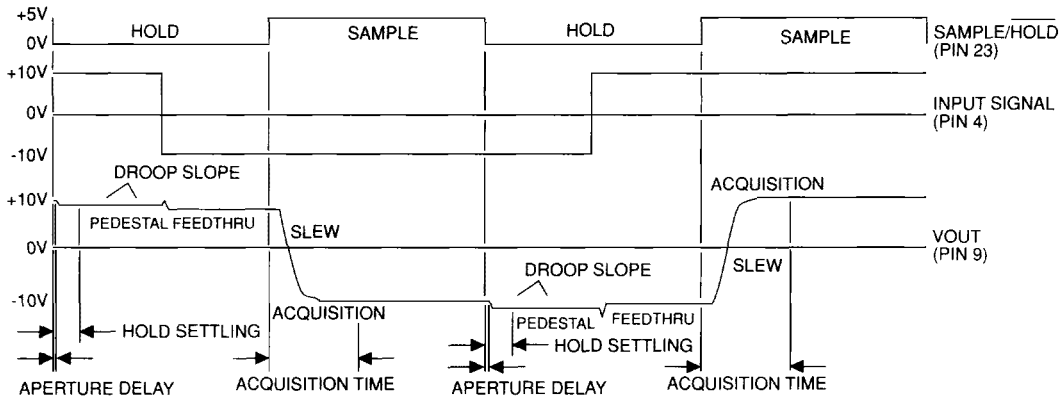
TOP VIEW

FUNCTIONAL PIN DESCRIPTIONS

Pins 1, 23, 24	Input Offset Trim: Trim pot connection for external offset trim of input buffer.
Pins 11, 12, 13	Output Offset Trim: Trim pot connection for external offset trim of output buffer.
Pin 2	Input Gain Trim: Trim pot wiper connection for external gain trim of input buffer.
Pin 14	Output Gain Trim: Trim pot wiper connection for external gain trim of output buffer.
Pin 4	Analog Input: High impedance signal input to first buffer.
Pin 9	Analog Output: Low impedance output of S/H amplifier.
Pin 21	S/$\overline{H}$ In: Logic control of sample mode (high) and hold mode (low).
Pin 20	+5V Ref Out: Internal reference generated with 78L05.
Pin 19	GND: Only ground pin.
Pin 3	+15V Input Supply: Input buffer positive supply.
Pin 22	-15V Input Supply: Input buffer negative supply.
Pin 15	+15V Output Supply: Output buffer positive supply.
Pin 10	-15V Output Supply: Output buffer negative supply.
Pin 7	+15V Gate Drive Supply: Analog switch positive supply.
Pin 5	-15V Gate Drive Supply: Analog switch negative supply.
Pin 18	Buffer Out: Output of input buffer.
Pin 16	TP: Factory test point.
Pin 8	TP: Factory test point.
Pin 6	TP: Factory test point.
Pin 17	No Connect.



TIMING DIAGRAM



TIMING

The timing diagram illustrates the critical timing points for the SP9760. This is illustrated by sending the SP9760 into hold and back to sample on both positive and negative going signals. The key points on the timing diagram are defined below.

Aperture Delay - the difference in time between when the hold signal is given and the SHA holds the input signal.

Hold Settling - the time it takes the SHA to settle to the held signal.

Pedestal - the difference in voltage between sample and hold for the same input voltage.

Droop Rate - the rate at which the held signal changes (droops) due to leakage of charge off the hold capacitor.

Feedthru - the extent to which a signal on the input of the SHA, during hold mode, will change the signal being held.

Slew Rate - the rate at which the sample and hold amplifier changes to the new signal being sampled.

Acquisition Time - the time it takes the sample-and-hold to settle and fully acquire a new signal. This time is dependent on input voltage change and accuracy required.

SUPPLY BYPASSING

Power supply bypassing is necessary to prevent oscillation with the SP9760 in all circuits. Low inductance ceramic disc capacitors with the shortest practical lead lengths must be connected from each supply lead (within 1/4" to 1/2" of the device package) to a ground plane. Capacitors should be 0.1 μF in parallel (for each supply pin) with a 10 μF solid tantalum capacitor for each supply voltage.

RECOMMENDED LAYOUT PRECAUTIONS

RF/video printed circuit board layout rules should be followed when using the SP9760 since it will provide power gain to frequencies over 30 MHz. Ground planes are recommended and power supplies should be decoupled at each device with low inductance capacitors.

The optional gain adjust pots and the offset adjust pots should be mounted within one inch of the SP9760. An etch guard ring should be laid around the gain and offset adjust circuitry and tied to the output of each buffer to prevent dynamic deterioration from stray capacitance. (See Figure 1.)

GAIN AND OFFSET ADJUSTMENTS

In most system applications there will be no need to adjust the gain and offset of the SP9760 separately. The system gain and offset adjustments should be used instead. However, it is not recommended that the gain and offset adjustment pots connected to the SP9760 be used to compensate system gain and offset errors.

Figure 1 shows the recommended gain and offset adjustment circuit. The gain and offset adjustments should be repeated for each buffer.

IMPORTANT: The lead length on the gain and offset adjustment circuit should be kept short (within one inch) to avoid oscillation or deterioration of dynamic performance.

The DVM must have both inputs floating. A hand held DVM with 100 μV or finer resolution may be used for this measurement.

For very critical adjustments a 5 minute warmup is recommended for the SP9760.

GAIN ADJUSTMENT

The gain adjustment should be done before the offset adjustment to avoid the effect that the gain pot has on the offset voltage.

The gain adjustment also affects the output resistance of the SP9760 buffers. The output resistance will be closest to zero ohms when the gain is closest to one.

The gain pot is adjusted in sample mode while plus full scale and minus full scale voltages (as defined by the user's system) are applied to the SP9760 by an external voltage source or by the previous stage in the system. This applied voltage needs to be only 10% accurate because the floating DVM is measuring gain error directly. The

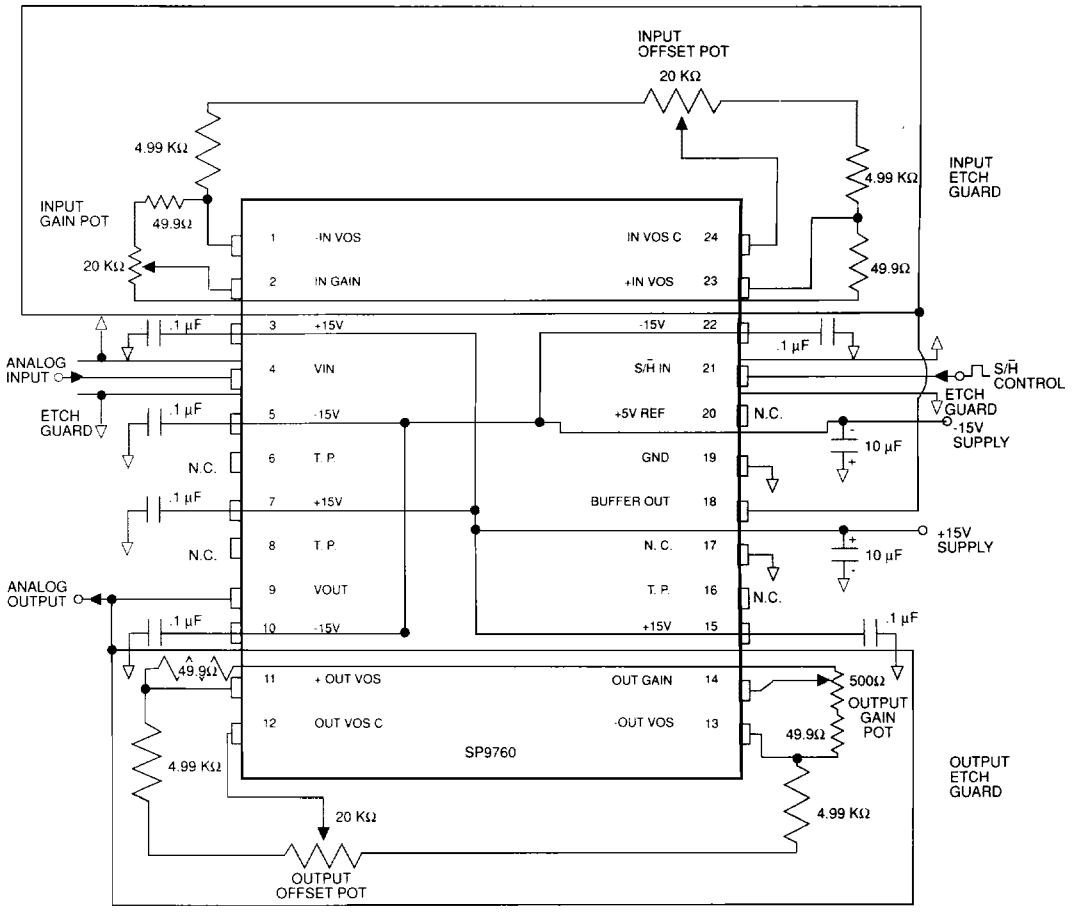


FIGURE 1
SUGGESTED TOPOLOGY AND RELATIVE PLACEMENT OF COMPONENTS

gain error has been compensated when the floating DVM reads the same value for plus full scale and minus full scale input voltages. The input voltage applied to the SP9760 can be a manually controlled DC voltage or a slow 2 to 10 second period full scale square wave.

OFFSET ADJUSTMENT

After the gain has been adjusted, the remaining error is eliminated by the offset adjustment. The input voltage applied to the SP9760 should be zero volts. The offset pot is adjusted until the floating DVM reads zero volts.

CAPACITIVE LOADING

Two considerations must be taken into account when driving capacitive loads. These are frequency stability and charge current magnitude.

For some values of load capacitance (>50 pf) it may be necessary to isolate the capacitive load with a resistor from 1Ω to 10Ω to reduce ringing or oscillation tendency. The desired step response can be obtained with the right resistor value for each application. (See Figure 2.)

The charge current magnitude must be controlled not to exceed the maximum rated output current for the SP9760. If the maximum output current is exceeded, the output stage will saturate during a transient and will take longer to recover.

The charge current into the capacitor is established by

$$I_{C\ load} = C_{load} \times \frac{dv}{dt}$$

The charge current can be limited by controlling the slew rate of the signals driving the SP9760, by reducing the amount of capacitive loading or by adding resistance in series with the capacitive load.

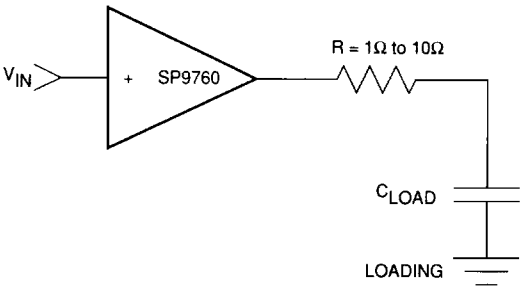


FIGURE 2
CAPACITIVE LOADING

APPLICATIONS

The SP9760 is suited for data acquisition and signal processing applications with high speed 14 and 16-bit analog-to-digital converters. In figure 3 the SP9760 is connected to an SP9588 14-bit 2 µsec analog-to-digital converter. The figure shows everything required for these two parts to work together, in a 0 to +10V unipolar mode. As can be seen in graph 1 with an input signal of 120 kHz at 0 dB the signal-to-noise + distortion ratio is 70 dB.

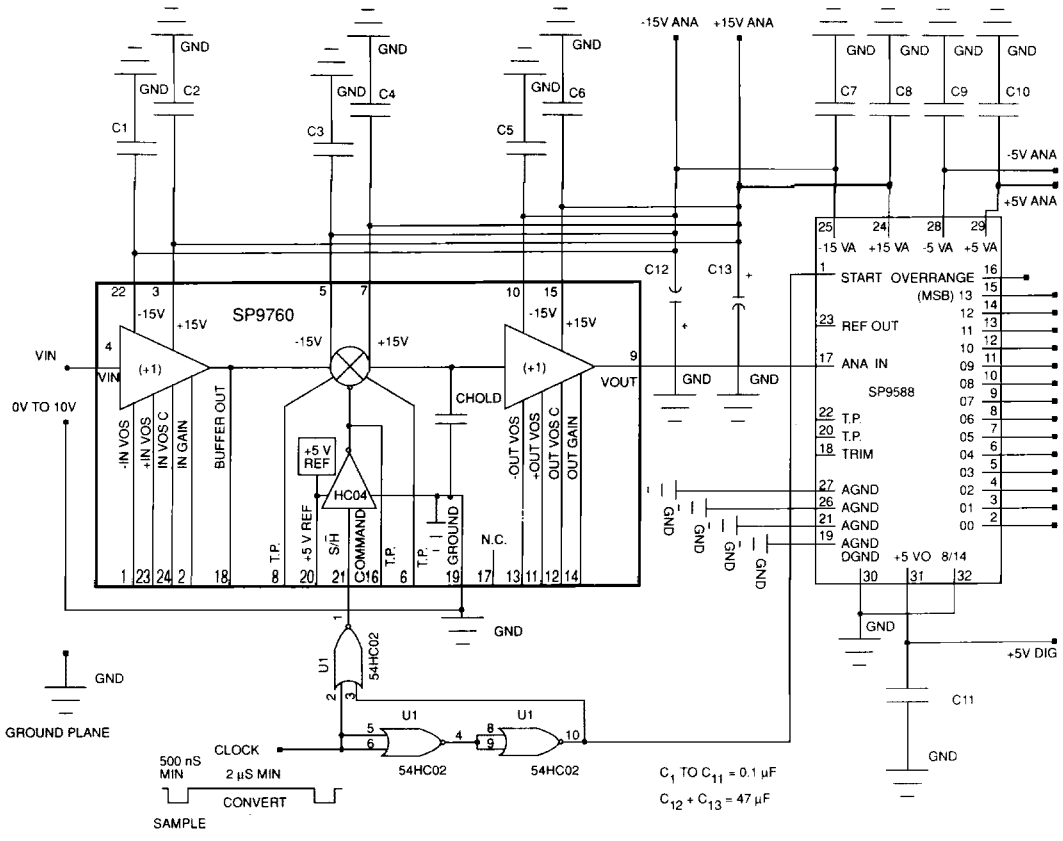


FIGURE 3
0V TO 10V UNIPOLAR DATA ACQUISITION SYSTEM

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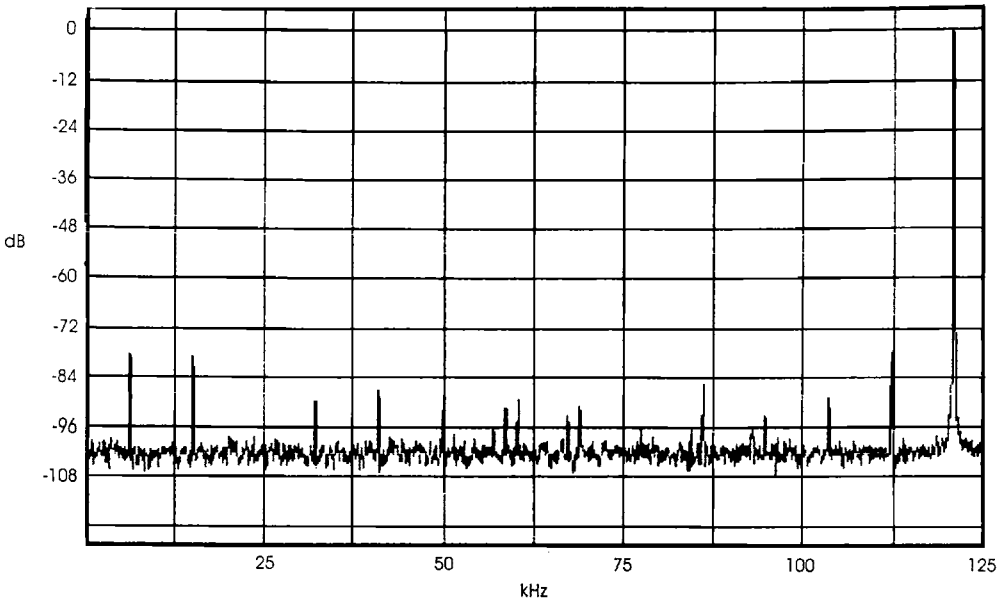
Sampling Rate = 250 kHz
Input Frequency = 120 kHz
Input Amplitude = 10 Volts p-p (0 dB)
Noise Floor < -100 dB
Maximum Harmonic < -72 dB



SIGNAL-TO-NOISE + DISTORTION RATIO
SINAD = 69.36 dB

Graph 1

The SP9760 and SP9588 can be used in the bipolar mode and be AC coupled for AC signal processing applications. In figure 4 the complete schematic is given for ±5V input range and AC coupling.

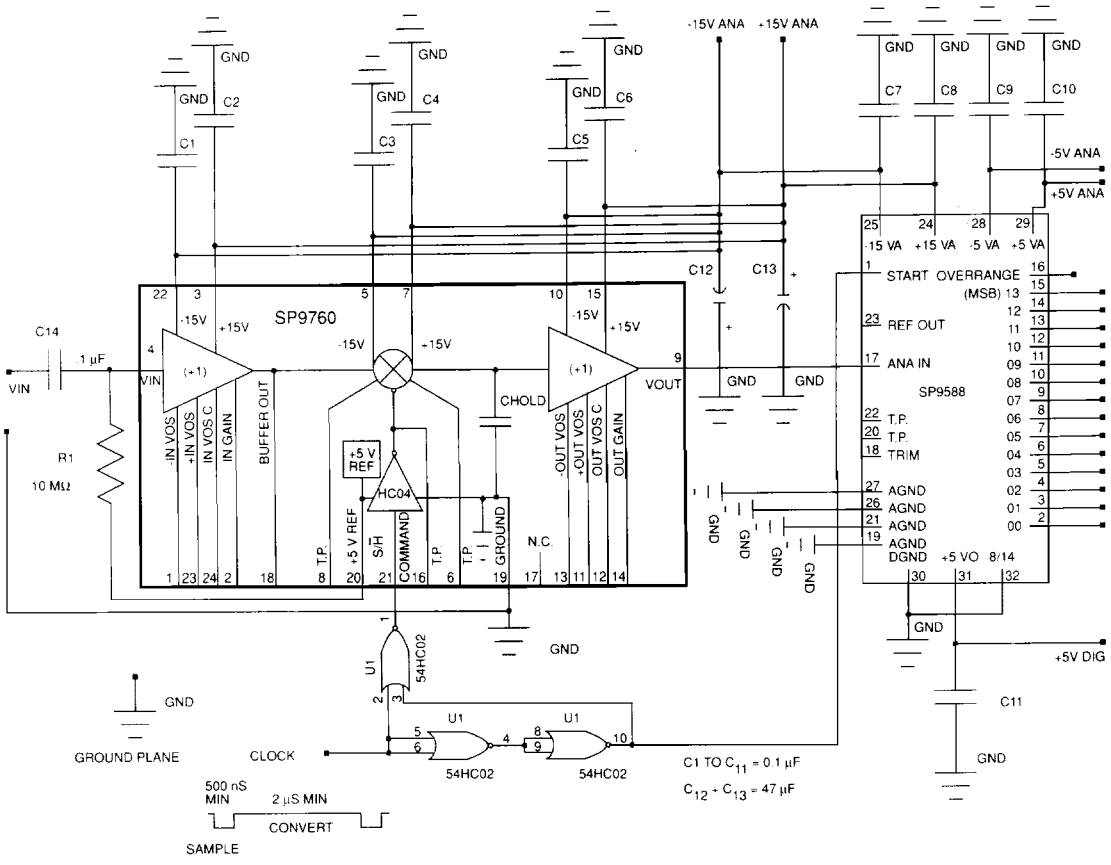


FIGURE 4
-5V TO +5V AC COUPLED BIPOLAR DATA ACQUISITION SYSTEM

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The SP9760 and SP9588 can be used in conjunction with a multiplexer for multi-channel data acquisition systems. The configuration seen in figure 5 will handle eight input channels providing a total throughput of 100 kHz per channel.

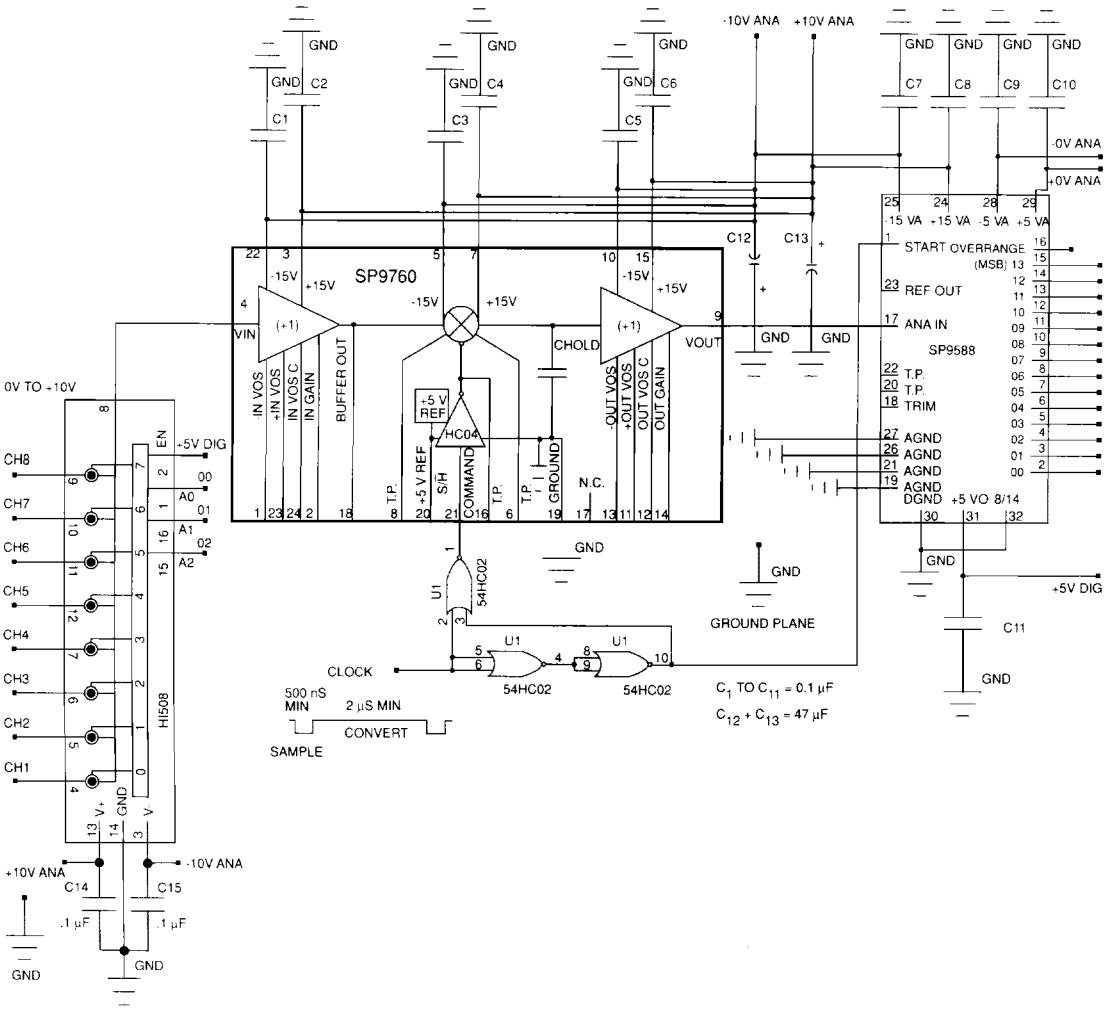

FIGURE 5
0V TO +10V UNIPOLAR DATA ACQUISITION SYSTEM WITH 8 CHANNELS AND 100 KHz THROUGHPUT

The internal buffer amplifier on the SP9760 can be used to implement a multi-order anti-aliasing filter for signal processing applications. (See Figure 6.) The formula for calculating the frequency and Q of the filter are:

$$F_o = \frac{1}{2\pi\sqrt{R_1 R_2 C_{14} C_{15}}}$$

$$\frac{1}{Q} = \sqrt{\frac{R_1 C_{15}}{R_2 C_{14}}} + \sqrt{\frac{R_2 C_{15}}{R_1 C_{15}}}$$

in this case F_O = 100 kHz Q = .5
$R_1 = R_2 = 1k\Omega$ $C_{14} = C_{15}$ = 1600 pF

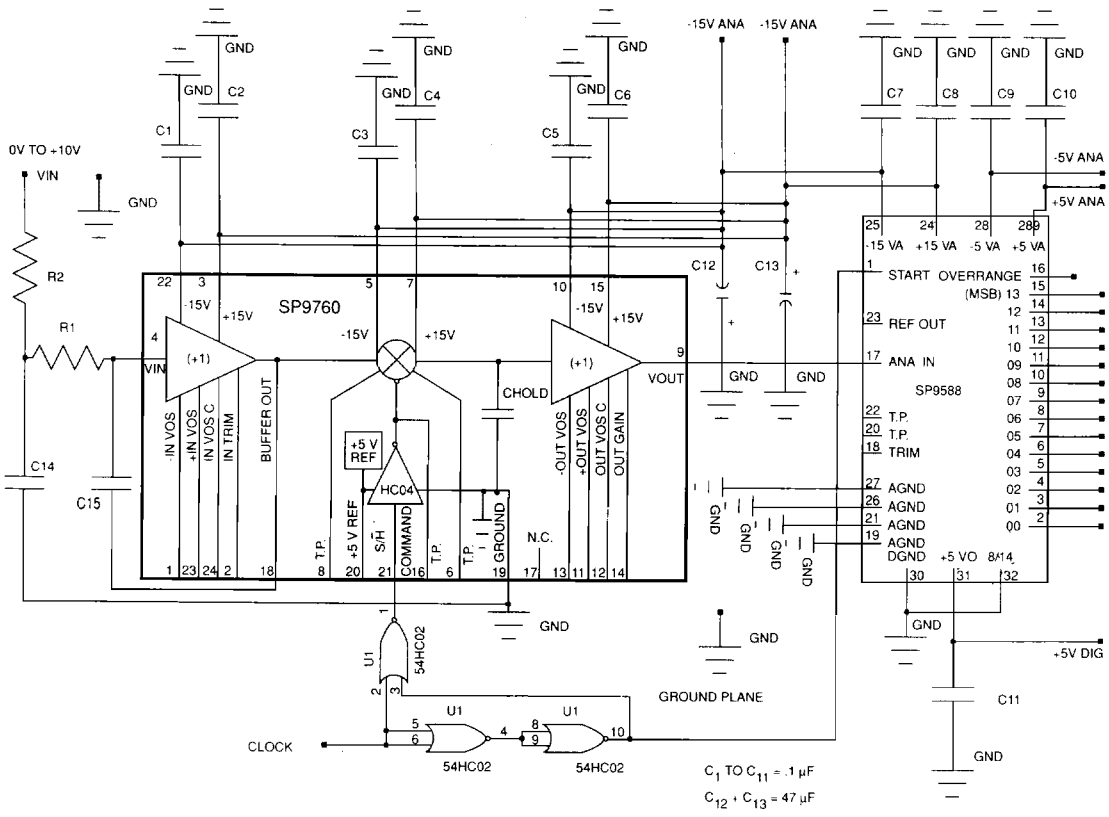

FIGURE 6
0V TO +10V UNIPOLAR DATA ACQUISITION SYSTEM WITH SECOND ORDER ANTI-ALIASING FILTER

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