ICs for Communications

2.5 Gbit/s, 3.3 V Transimpedance Amplifier

FOA1251B1, FOA1252B1 Device Version 1.0

High Gain 3.3 V Transimpedance Amplifier with Postamplifier for Tele- and Datacom Receiver Applications

Advance Datasheet 10June1999 Document Rev. 1.0

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Related Documentation

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Advance Information

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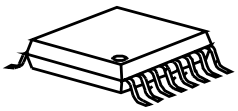
Advance Information

2.5 Gbit/s, 3.3 V Transimpedance Amplifier

FOA1251B1
FOA1252B1

Device Version 1.0 **Bipolar**

1 Overview



P-TSSOP-16-1

1.1 Features

- Nominal data rate: 2.488 Gbit/s.
- Input sensitivity: - 23.0 dBm at BER = 10^{-10}.
- Transimpedance: 27 kΩ.
- High overload: 2.2 mA_{pp} maximum input current.
- Single power supply: + 3.3 V.
- Full ITU-T G957 specification compliance.
- Internal DC-compensation loop increases dynamic range.
- Operation without external components.
- Internal bias generation for PIN-photodiode.
- Internal low-pass filter to improve power supply rejection.
- Operates with PIN-photodiode or APD.
- Monitor output for mirrored photodiode current.
- Additional pair of complementary output pins optimized for TO-packages.
-

1.2 Typical Applications

- Fibre optics data- and telecommmunication systems as e.g. OC48 and STM 16:
  - SDH,
  - SONET,
  - ATM.
- Pre-Amplifier Modules.
- Optical Receiver Modules.
- Digital CATV

Type	Ordering Code	Package
FOA1251B1	Q67000-H????	P-TSSOP-16-1
FOA1252B1	Q67000-H????	Bare die

1.3 General Description

The FOA1251B1, FOA1252B1 is a high performance transimpedance amplifier (TIA) designed for use in data- and telecommunication systems for optical networks:

- SDH STM-16
- SONET OC-48

The FOA1251B1, FOA1252B1 can be used from a single +3.3 V power supply. It offers a transimpedance of typically 27 kΩ over a 3 dB bandwidth of at least 1600 MHz. The sensitivity of the device allows for a limitated output voltage with input currents greater than 10 µA.

The output signal has a typical differential amplitude of 500 mV_{pp}, which facilitates easy interconnection to downstream clock/data recovery and demultiplexer devices. The high output voltage and the built-in limiting function eliminate the need for a limiting amplifier in typical receiver applications.

The FOA1251B1, FOA1252B1 has an on-chip filtered output used for DC biasing of the PIN-diode. If an APD is used as input signal source, an external DC source with higher voltage may be required. Decoupling to the filter terminal of the FOA1251B1, FOA1252B1 is still recommended because this pin serves as stable reference point for the input signal.

The input sensitivity which is measured at BER = 10^{-10} is better than -23 dBm.

A separate monitor signal is available from the FOA1251B1, FOA1252B1. This signal is intended for supervision of the input DC current without intrusion into the sensitive input signal path.

The FOA1251B1, FOA1252B1 can be delivered in a standard TSSOP-16 plastic package for PCB mounting, or as die for integration with the PIN diode into one package. The latter will keep the high impedance interconnection to the PIN diode short, which results in increased bandwidth and a minimized noise-pickup.

1.4 Pin Configuration

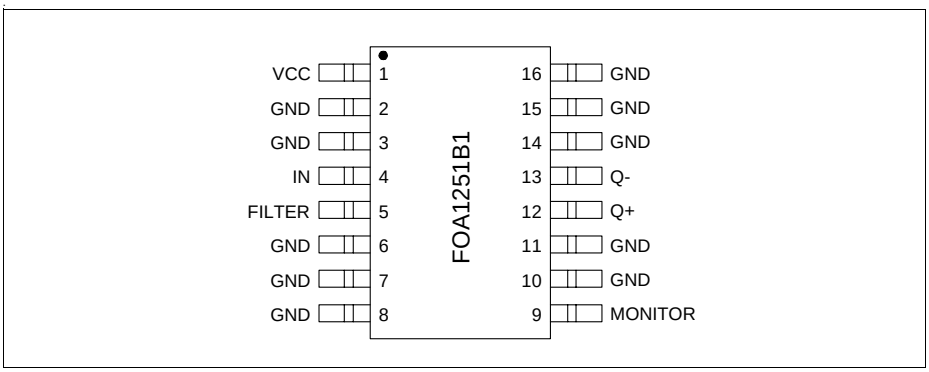


Figure 1-1 P-TSSOP-16 Package Pinout (top view).

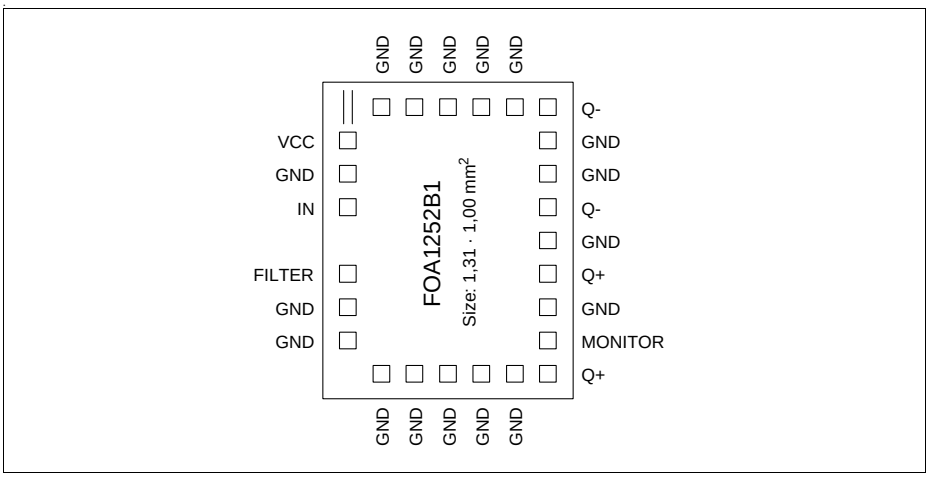


Figure 1-2 Pad Assignment of Bare Die (top view).

1.5 Pin Definitions and Functions

Table 1-1 Pin Definition and Functions

Pin No.	Symbol	I / O	Function
1	VCC	-	Supply voltage
2, 3	GND	-	Ground
4	IN	I	Data input from PIN- or APD-photodiode
5	FILTER	O	Non-inverting data output
6, 7, 8	GND	-	Ground
9	MONITOR	O	Mirrored photodiode current (1), (2)
10, 11	GND	-	Ground
12	Q+	O	Inverting data output
13	Q-	O	Non-inverting data output
14, 15, 16	GND	-	Ground

Notes:

1. Connect pin 9 via resistor (0 ... 2 kΩ) to V_{CC} if used, otherwise pin should be left open.
2. Monitor current is directly proportional to rms-value of input current.

1.6 Functional Block Diagram

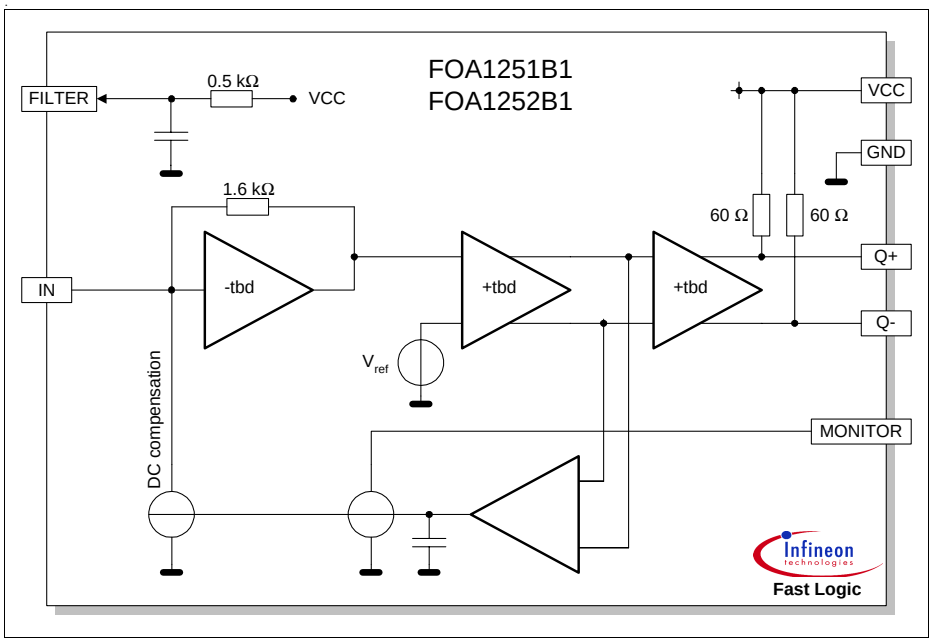


Figure 1-3 Block Diagram of Transimpedance Amplifier with Postamplifer Section.

2 Circuit Description

The single ended input signal from the PIN-diode or APD is fed into an inverting amplifier block with high gain and high bandwidth. An internal feedback stabilizes the overall operation and gives the pre-amplifier block a linear gain and phase up to its bandwidth limit of min. 1.6 GHz for the FOA1252B1. The amplified signal continues to an amplifier stage with differential output. Finally, the signal goes through a post-amplifier before it leaves the device on the Q+ and Q- terminals. The output terminals are both internally terminated with a 60 Ω pull-up resistor to V_{CC}.

An internal voltage reference is connected to the intermediate amplifier block. Hence, the DC content of the differential output from this amplifier stage is proportional to the DC value of the input signal. The DC content is extracted by a separate amplifier and fed back internally to the input amplifier. This internal feedback accomplishes overall DC compensation of the device, so that the output signal at the Q+ and Q- is widely independent of the DC content in the input signal.

The differential output signals Q+ and Q- are internally connected to the positive supply V_{CC} via 60 Ω pull-up resistors. In order to prevent any DC shift problems, the output signals should be AC coupled to the load. Coupling capacitors of approximately 100 nF are suitable values, but may need to be optimized for the specific application. The outputs can be used single or differentially ended; but, it is strongly recommended to use differential operation for best performance. However, if single-ended operation is necessary, the unused output should be terminated with an impedance equal to the load on the pin in use.

The single-ended monitor output signal is a low pass filtered "copy" of the PIN diode current. It can be used for supervision of the state ot the PIN-diode or APD, or it can be left unconnected if not needed.

The occurence of an overload condition is detected at the transimpedance amplifier stage. This early detection feature allows for an active biasing of the circuit, thus avoiding performance losses due to saturation effects.

All device pins should be soldered to the PCB in order to obtain the best possible grounding and thermal drainage of the device.

3 Electrical Characteristics

3.1 Absolute Maximum Ratings (1)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Ambient temperature	T_A	-40	+85	°C	
Supply voltage	V_{CC}	tbd	tbd	V	Refered to GND
Junction temperature	T_j	-40	+125	°C	
Storage temperature	T_S	-40	+125	°C	
Relative ambient humidity			85/85	%/°C	No condensation
ESD integrity	U_{ESD}	1.4		kV	(2), (3)

Notes:

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *HBM according to MIL-Std 883D, method 3015.7 and ESD Ass. Standard EOS/ ESD-5.1-1993.*
3. *The RF pin IN is not ESD protected. The high frequency performance prohibits the use of adequate protective structures. All other pins are ESD protected.*

3.2 Operating Range [1]

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Ambient temperature	T_A	-30		+105	°C	
Data transmission rate			2.488		Gbit/s	
Supply voltage	V_{CC}	3.0		3.6	V	
Supply current	I_{CC}		34	41	mA	
Thermal resistance	Θ_{JA}		140		K/W	(2)
Junction temperature	T_J	-10		+125	°C	

Notes:

1. *In the operating range, the functions given in the circuit description are fulfilled.*
2. *Junction-to-ambient thermal resistance measurement conditions for packaged device FOA1251B1. PCB area: 10 cm × 10 cm × 1.5 mm. Copper area approx. 60 %. Via holes to ground layer underneath the device. All pins soldered.*

3.3 DC Characteristics (1)

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Supply current	I_{CC}		34		mA	
Input voltage	V_{IN}		+0.8		V	
Input current	I_{IN}			2200	µA	
Input current	$I_{IN,CL}$		10		µA	before clipping
Input resistance			tbd			
Output voltage swing	$\Delta V_{OUT,DC}$		0.6		V_{PP}	I_{IN} = 50 µA
Output resistance	R_{OUT}	48	60	72		(2)
Output voltage	$V_{CM,OUT}$		2.7		V	(3)
Bias resistance	R_{BIAS}	400	500	600	Ω	

Notes:

1. *Conditions: T_A = +25 °C, V_{CC} = +3.3 V, $C_{external}$ = 0.85 pF.*
2. *Resistors internally connected to V_{CC} .*
3. *$V_{CM,OUT} = (V_{Q+} - V_{Q-}) / 2$.*

3.4 AC Characteristics [1]

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Input sensitivity	P_{IN}	tbd	-23		dBm	(2)
Optical overload	P_{OVL}		1.5		dBm	(2)
Transimpedance	R_T		27		kΩ	(3)
Bandwidth	$f_{3dB,\ upper}$	1.6	1.8	2.0	GHz	FOA1252B1
Low frequency cutoff	$f_{3dB,\ lower}$		65		kHz	(4)
Output voltage swing	$\Delta V_{OUT,AC}$		500		mV_{PP}	(4), (5)
Power supply rejection ratio	$PSRR$		tbd		dB	(6)
Input current	$I_{IN,CL}$		10		µA	before clipping
Input resistance			tbd			
Output resistance	R_{OUT}	48	60	72		(4)
Output voltage	$V_{CM,OUT}$		2.7		V	(5)
Bias resistance	R_{BIAS}	400	500	600	Ω	

Notes:

1. *Conditions:*
   T_A = +25 °C, V_{CC} = +3.3 V, $C_{external}$ = 0.85 pF
   data rate: 2.488 Gbit/s; data sequence: PRBS, 2^{31}-1; BER = 10^{-10}.
2. *Responsitivity of photodetector: 0.8 A/W.*
   Extinction ratio 9.1 dB; Gating 10^{12} bit.
3. *Differential measurement; input current 5 µA_{pp}.*
4. *AC-coupled outputs via 22 nF into 50 Ω load.*
5. *differential measurement; each output AC-coupled and terminated with 50 Ω.*
6. *Equivalent noise signal on positive power supply rail: sine curve; f < 10 MHz;*
   U < 100 mV_{PP}; refer to application note (figure 5-3)

4 Test Circuits and Results (Preliminary)

4.1 Bit Error Rate Measurements (BER)

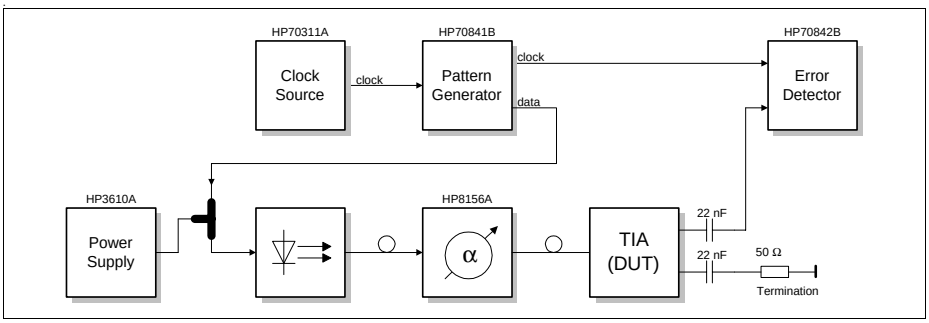


Figure 4-1 BER Measurement Set-Up.

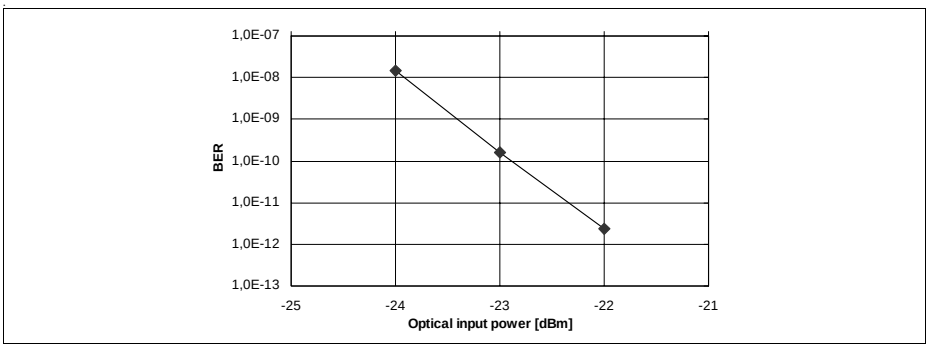


Figure 4-2 Bit Error Rate Results.

4.2 Eye Diagrams (Preliminary)

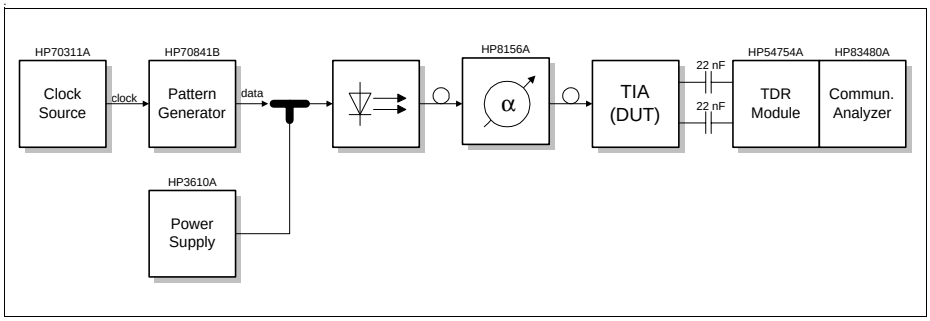


Figure 4-3 Eye Diagram Measurement Set-Up.

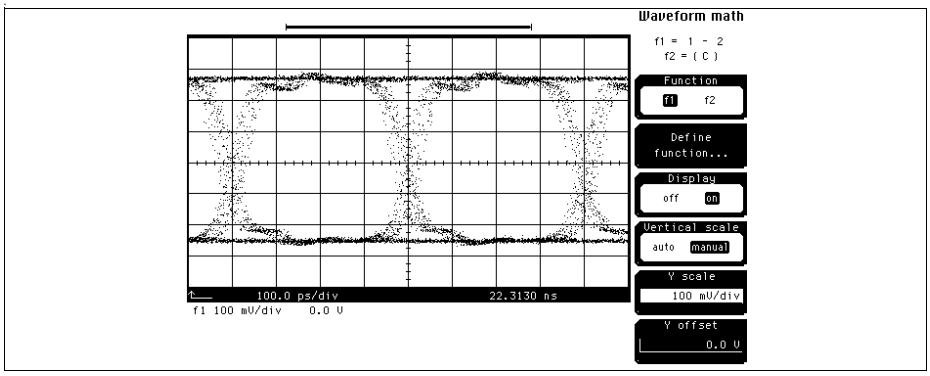


Figure 4-4 Eye Diagrams at Optical input Power +0.9 dBm.

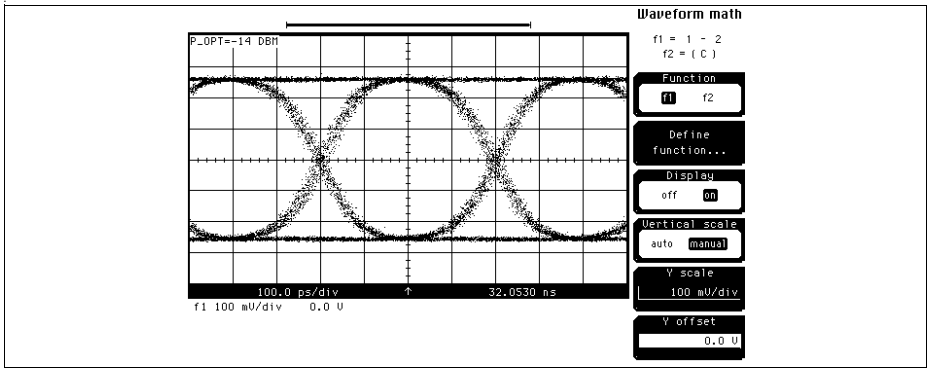


Figure 4-5 Eye Diagrams at Optical input Power -14 dBm.

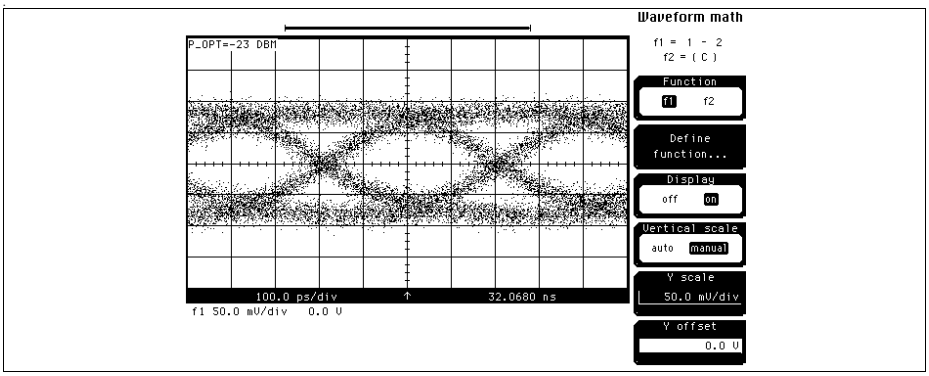


Figure 4-6 Eye Diagrams at Optical input Power -23 dBm.

4.3 Bandwidth and Transimpedance

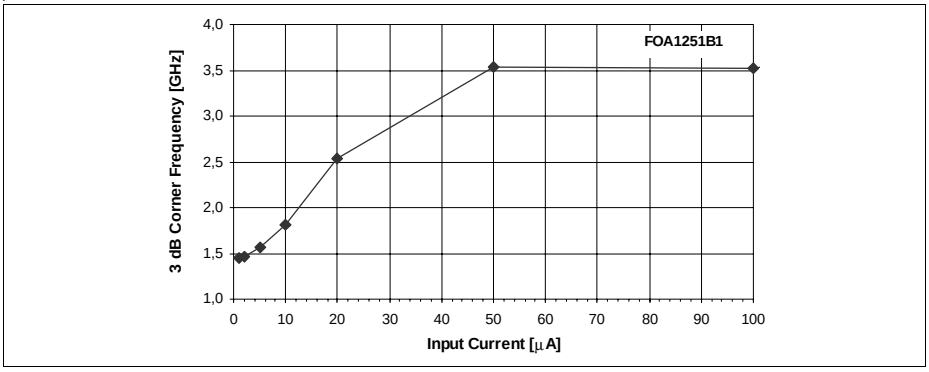


Figure 4-7 Upper Corner Frequency of FOA1251B1 in P-TSSOP-16-1 Package.

Remark:
Upper corner frequency is measured with packaged version. Due to parasitic capacitance and inductance bandwidth is lower compared to bare chip version.

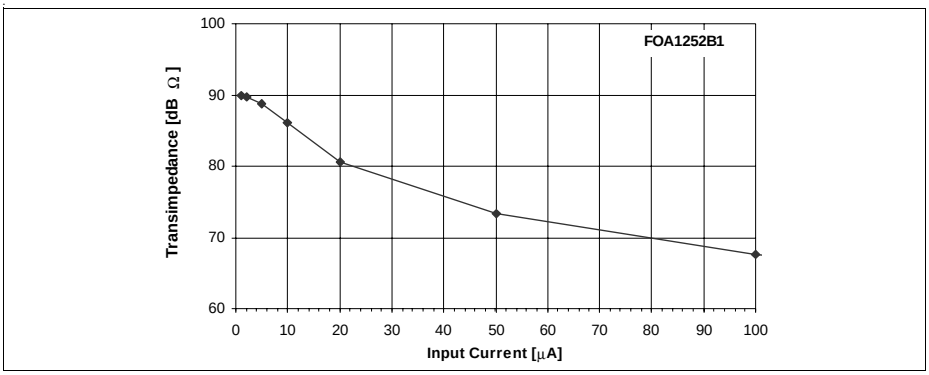


Figure 4-8 Transimpedance versus Input Current of FOA1252B1.

5 Application Notes

5.1 General Information

- The output pins Q_+ and Q_- must be terminated equally to prevent instabilities.
- It is recommended to minimize stray capacitance when connecting photodiode to transimpedance amplifier.
- To improve power supply rejection ratio (PSRR), V_{CC} should be supplied via resistor (4.7 Ω), capacitor (100 nF) to GND, and inductor (BLM11A601, Murata) to V_{CC}-pin. The monitor pin (not used in these application notes) must be left open or connected to V_{CC} via resistor of 0 … 2 kΩ.

5.2 Typical Applications

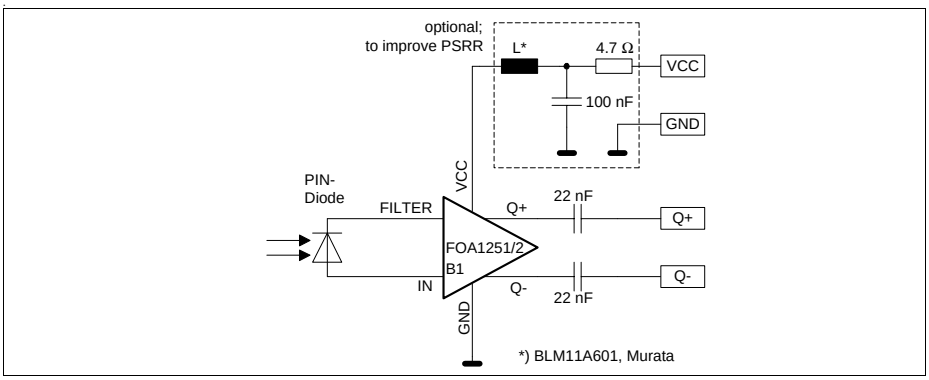


Figure 5-1 PIN-diode connected to Transimpedance Amplifier.

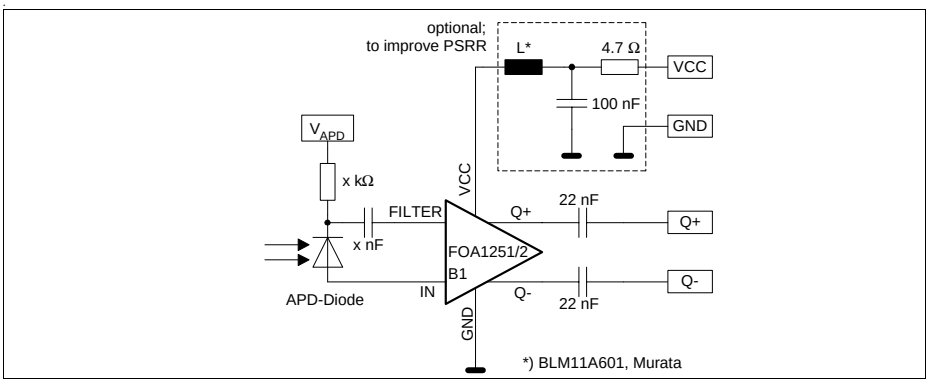


Figure 5-2 PIN-diode connected to Transimpedance Amplifier.

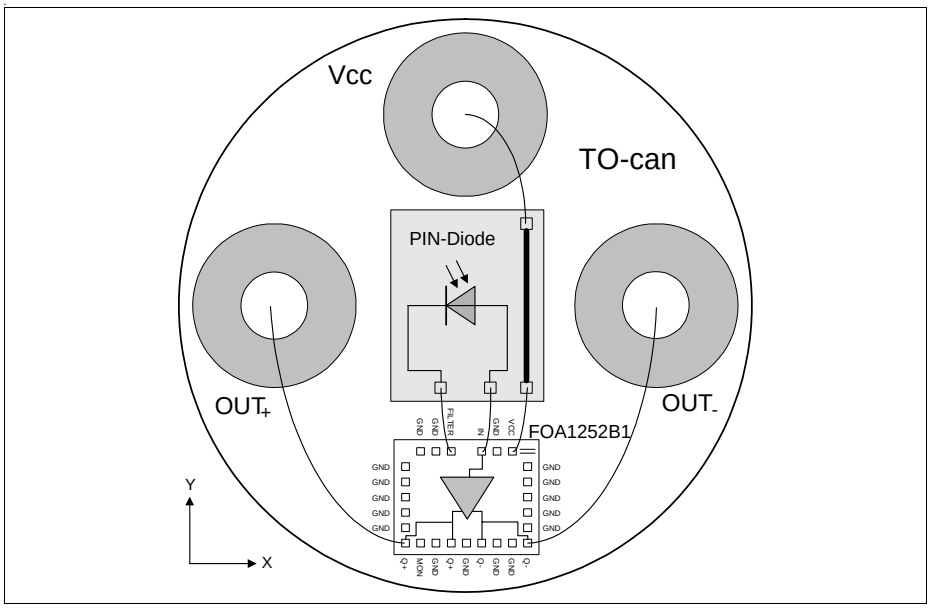


Figure 5-3 Application Example of FOA1252B1 mounted in TO-Module.

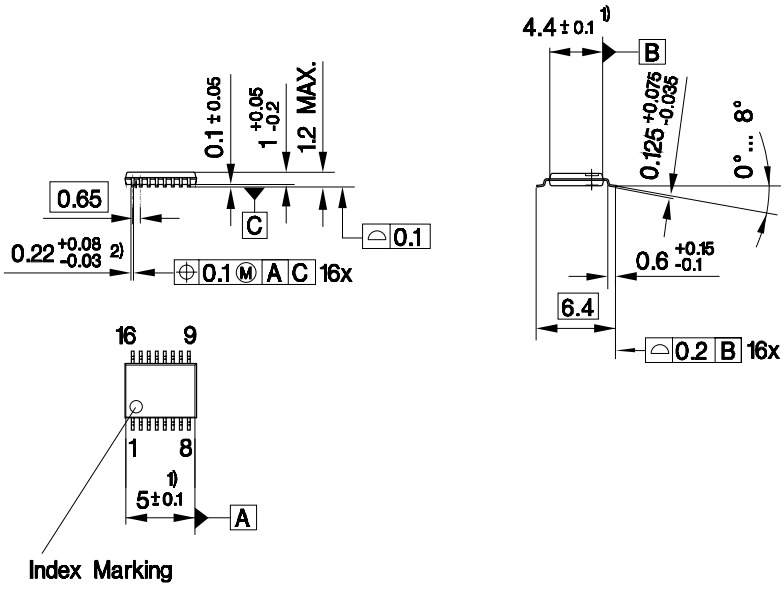
Remarks

- No external components needed.
- The bonding layout as well as the arrangement of transimpedance amplifier and PIN-diode submount is symmetric refered to y-axis. In consequence the electromagnetical fields - induced by output bonding wires - compensate approximately in the middle of the module. Therefore it is required to terminate both outputs with the same load.

6 Package and Bare Die Outlines

6.1 Package Outlines

P-TSSOP-16-1(Plastic Thin Shrink Small Outline Package)



1) Does not include plastic or metal protrusion of 0.15 max. per side

2) Does not include dambar protrusion

Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

6.2 Bare Die Outlines

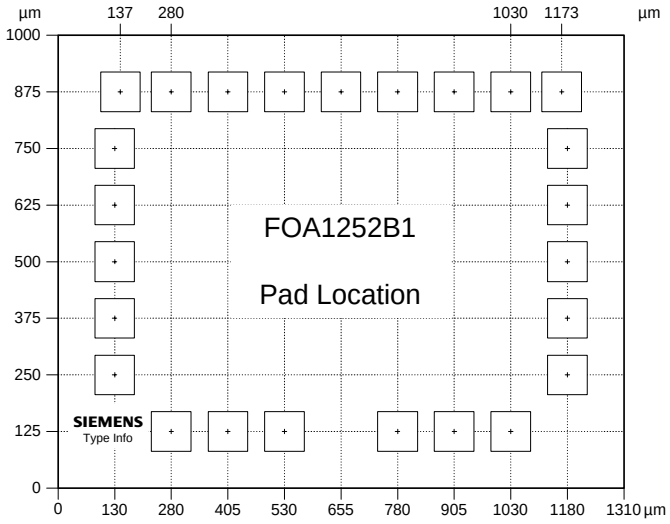


Figure 6-1 Bond Pad Coordinates (top view).

Chip

- Area: 1310 µm x 1000 µm
- Thickness: 280 µm

Pad

- Area: 100 µm x 100 µm
- Material: aluminium

7 Glossary

ATM	Asynchronous Transfer Mode
APD	Avalanche Photodiode
BER	Bit Error Rate
CATV	Cable Television
NRZ	Non Return to Zero
PIN	Positiv-Intrinsic-Negative (doping of photodiode)
PRSB	Pseudo Random Bit Sequence
SDH	Synchronous Digital Hirachie
SONET	Serial Optical Network
TIA	Transimpedance Amplifier

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- Under Preparation -

9 Notes