1x4Mx32bit DRAM Card
2x4Mx32bit DRAM Card
1x4Mx36bit DRAM Card
2x4Mx36bit DRAM Crad

Connector Type

Two-piece 88-pin

MF116M-L17ATXX
MF132M-L17ATXX

MF116M-L27ATXX
MF132M-L27ATXX

DESCRIPTION

These DRAM CARDs are developed based on JEIDA DRAM CARD GUIDELINE Ver. 2. 0.
These cards are made using industry standard 4 M × 4 and 4 M × 1 Dynamic RAM and interface IC' s in TSOP.

FEATURES

- All inputs except $\overline{RAS}$ inputs are buffered.
- Standard card size : 54mm (W) × 85. 6mm (L) × 3. 3mm (T)
- 88pin 2 piece connector type.
- $\overline{RAS}$ only refresh mode, $\overline{CAS}$ before $\overline{RAS}$ refresh mode and Page mode functions are available.
- Extended refresh is available. (128ms/2048cycle)

APPLICATIONS

Main/expansion memory unit for Personal Computer. Laser-Printer, FAX etc.

PRODUCT LIST

Product No.	Item / Type name	Memory capacity	Date Bus width (bits)	Access time (t_{RAC}) (ns)	Connector type	Number of pins	Outline drawing
No. 1	MF116M-L17ATXX	16MB	32 (without parity)	70	Two-piece	88	88P-001
No. 2	MF132M-L17ATXX	32MB					
No. 3	MF116M-L27ATXX	16MB	36 (with parity)				
No. 4	MF132M-L27ATXX	32MB					

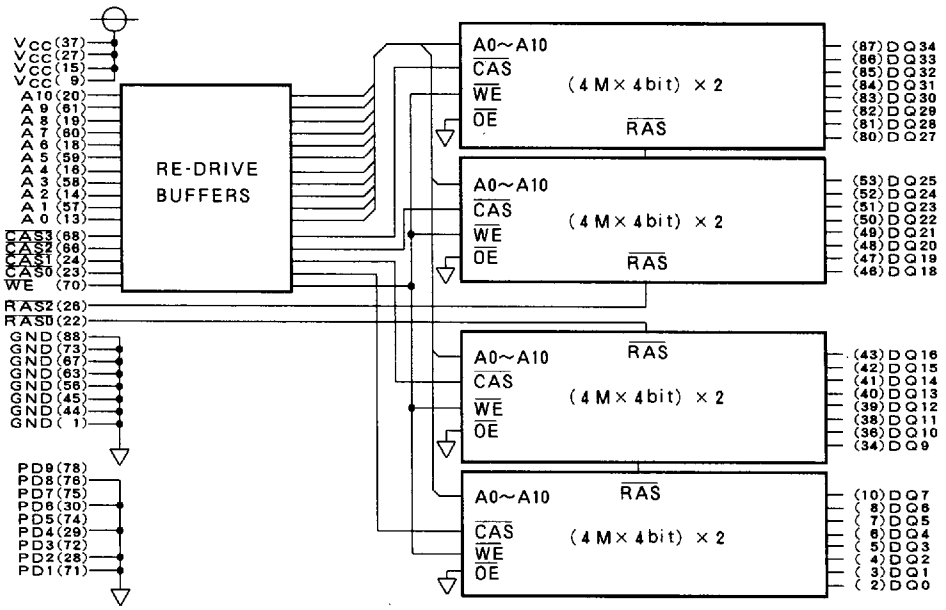
PIN ASSIGNMENT

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	GND	Ground	45	GND	Ground
2	DQ 0	}	46	DQ18	}
3	DQ 1		47	DQ19	
4	DQ 2		48	DQ20	
5	DQ 3	} Data I/O	49	DQ21	} Data I/O
6	DQ 4		50	DQ22	
7	DQ 5		51	DQ23	
8	DQ 6	}	52	DQ24	
9	Vcc	Power supply voltage	53	DQ25	}
10	DQ7	Data I/O	54	DQ26	Data I/O (NC for No. 1, No. 2)
11	NC	No connection	55	NC	No connection
12	DQ 8	Data I/O (NC for No. 1, No. 2)	56	GND	Ground
13	A 0	} Address input	57	A 1	}
14	A 2		58	A 3	
15	Vcc	Power supply voltage	59	A 5	} Address input
16	A 4	Address input	60	A 7	
17	NC	No connection	61	A 9	}
18	A 6	}	62	NC	No connection
19	A 8	} Address input	63	GND	Ground
20	A10	}	64	NC	No connection
21	NC	No connection	65	$\overline{RAS1}$	Row address strobe 1 (NC for No. 1, No. 3)
22	$\overline{RAS0}$	Row address strobe 0	66	$\overline{CAS2}$	Column address strobe 2
23	$\overline{CAS0}$	Column address strobe 0	67	GND	Ground
24	$\overline{CAS1}$	Column address strobe 1	68	$\overline{CAS3}$	Column address strobe 3
25	NC	No connection	69	$\overline{RAS3}$	Row address strobe 3 (NC for No. 1, No. 3)
26	$\overline{RAS2}$	Row address strobe 2	70	$\overline{WE}$	Write enable
27	Vcc	Power supply voltage	71	PD 1	Presence detect 1
28	PD 2	Presence detect 2	72	PD 3	Presence detect 3
29	PD 4	Presence detect 4	73	GND	Ground
30	PD 6	Presence detect 6	74	PD 5	Presence detect 5
31	NC	} No connection	75	PD 7	Presence detect 7
32	NC	}	76	PD 8	Presence detect 8
33	DQ17	Data I/O (NC for No. 1, No. 2)	77	NC	No connection
34	DQ 9	Data I/O	78	PD 9	Presence detect 9
35	NC	No connection	79	DQ35	Data I/O (NC for No. 1, No. 2)
36	DQ10	Data I/O	80	DQ27	}
37	Vcc	Power supply voltage	81	DQ28	
38	DQ11	}	82	DQ29	
39	DQ12		83	DQ30	
40	DQ13	} Data I/O	84	DQ31	} Data I/O
41	DQ14		85	DQ32	
42	DQ15		86	DQ33	
43	DQ16	}	87	DQ34	}
44	GND	Ground	88	GND	Ground

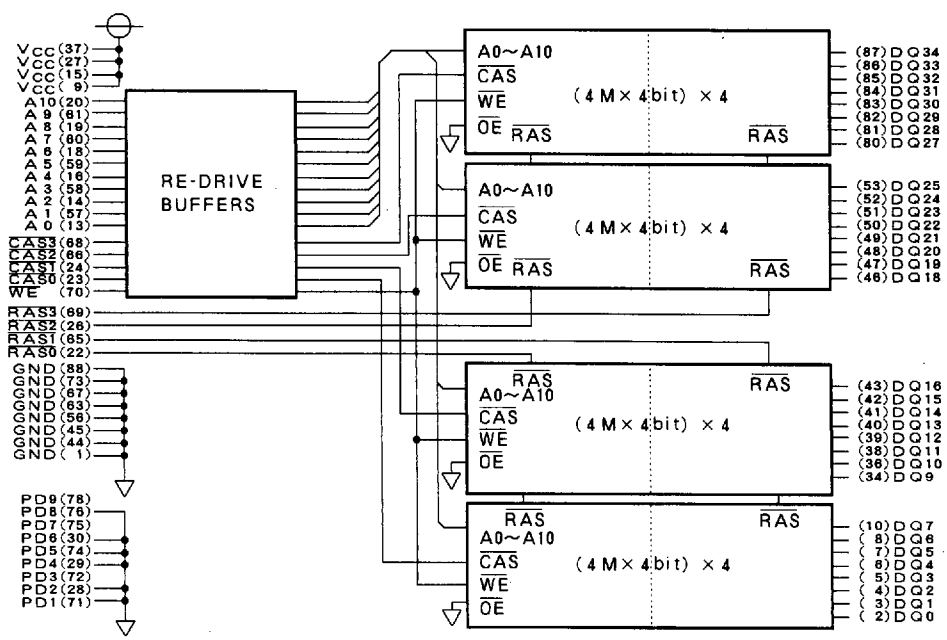
PD Pin Table

Product No.	PD 1	PD 2	PD 3	PD 4	PD 5	PD 6	PD 7	PD 8	PD 9
No. 1	GND	GND	NC	GND	NC	GND	NC	GND	NC
No. 2	GND	GND	NC	GND	GND	GND	NC	GND	NC
No. 3	GND	GND	NC	GND	NC	GND	NC	GND	NC
No. 4	GND	GND	NC	GND	GND	GND	NC	GND	NC

BLOCK DIAGRAM (No.1)



BLOCK DIAGRAM (No.2)



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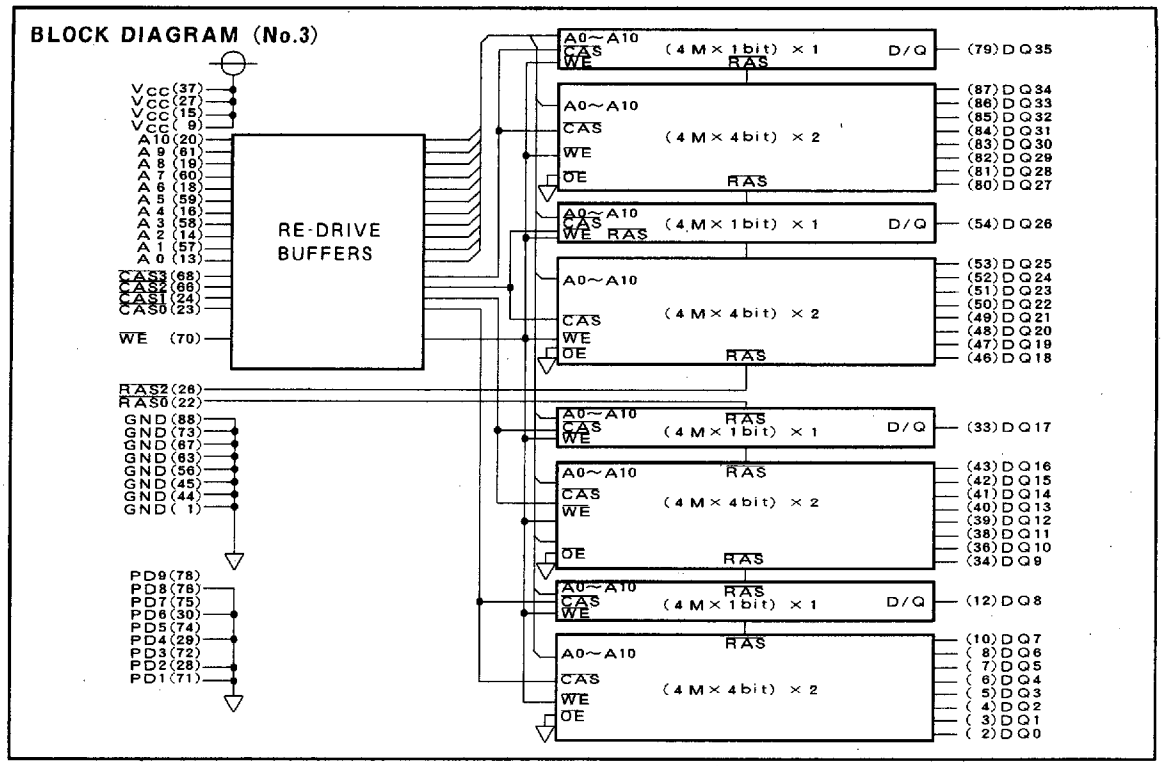
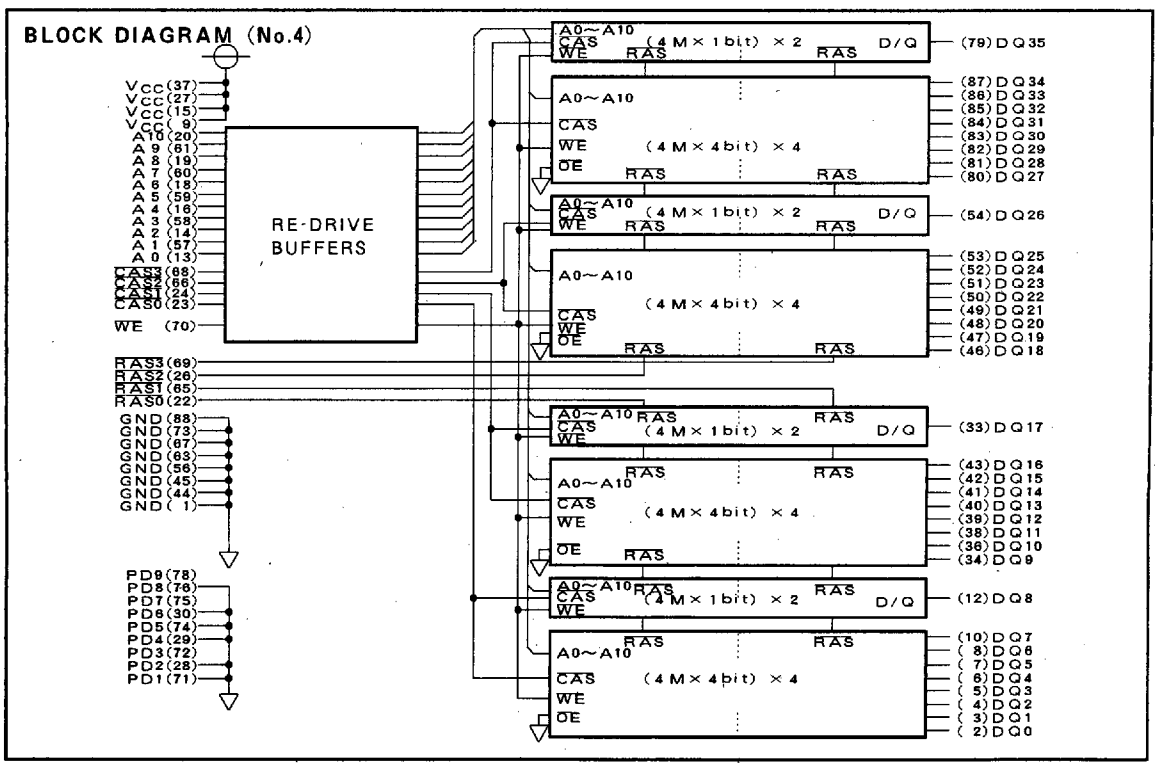


BLOCK DIAGRAM (No.4)



FUNCTION TABLE

Operation	input					input/output		Refresh	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	input	output		
Read	ACT	ACT	NAC	APD	APD	OPN	VLD	YES	Page mode indentical
Early write	ACT	ACT	ACT	APD	APD	VLD	OPN	YES	
$\overline{RAS}$ only refresh	ACT	NAC	DNC	APD	DNC	DNC	OPN	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	OPN	YES	
Self refresh	ACT	ACT	NAC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note 1 : ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, APD : applied, OPN : open
Don't be active the even and odd No. RASs at the same time. (Read/Early write cycle only)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings				Unit
			No. 1	No. 2	No. 3	No. 4	
V_{CC}	Supply voltage	With respect to GND	−1.0~7.0				V
V_I	Input voltage		−1.0~7.0				V
V_O	Output voltage		−1.0~7.0				V
I_O	Output current		50				mA
P_d	Power dissipation	T_a=25℃	8	16	12	24	W
T_{opr}	Operating temperature		0~55				℃
T_{stg}	Storage temperature		−40~80				℃

RECOMMENDED OPERATING CONDITIONS (T_a= 0~55℃, unless otherwise noted): (Note 2)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	Supply voltage	4.75	5	5.25	V
GND	Supply voltage	0	0	0	V
V_{IH}	High input voltage	0.7×V_{CC}		V_{CC}	V
V_{IL}	Low input voltage	0		0.8	V

Note 2 : With respect to GND

ELECTRICAL CHARACTERISTICS (T_a = 0 ~ 55℃, V_{CC} = 5 V ± 5 %, GND = 0 V) : (Note 3)

Symbol	Parameter	Test condition	Limits									Unit
			Min.				Typ.	Max.				
			No. 1	No. 2	No. 3	No. 4		No. 1	No. 2	No. 3	No. 4	
V_{OH}	High output voltage	I_{OH} = − 5 mA	2.4					V_{CC}				V
V_{OL}	Low output voltage	I_{OL} = 4.2 mA	0					0.4				V
I_{OZ}	Off-stage output current	0 V ≦ V_{OUT} ≦ V_{CC}	−10	−20	−10	−20		10	20	10	20	μA
I_I	Input current	0 V ≦ V_{IN} ≦ V_{CC} Other input pins = 0 V	−40		−60			40		60		μA
$I_{CC1(AV)}$	Average supply current from V_{CC}, operating (Note 4, 5, 6)	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = t_{WC} = min, output open						900	920	1250	1280	mA
$I_{CC2(AV)}$	Supply current from V_{CC}, standby (Note 7)	$\overline{RAS}$ = $\overline{CAS}$ ≧ V_{CC} − 0.2V, other input pins ≧ V_{CC} − 0.2V or ≦ 0.2V, output open						3.2	6.4	3.6	7.2	mA
$I_{CC3(AV)}$	Average supply current from V_{CC}, refreshing (Note 4, 6)	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH} t_{RC} = min, output open						890	1750	1240	2450	mA
$I_{CC4(AV)}$	Average supply current from V_{CC}, Page-Mode (Note 4, 5, 6)	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling t_{RC} = min, output open						530	580	890	970	mA
$I_{CC6(AV)}$	Average supply current from V_{CC}, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 4, 6)	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC} = min, output open						850	1700	1160	2300	mA
$I_{CC8(AV)}$	Average supply current from V_{CC}, Extended refresh mode (Note 7)	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling WE ≧ V_{CC} − 0.2V other input pins ≧ V_{CC} − 0.2V or ≦ 0.2V, output open t_{RC} = 62.5 μs						5	10	5.7	11.4	mA
$I_{CC9(AV)}$	Average supply current from V_{CC}, Self refresh mode (Note 7)	$\overline{RAS}$ = $\overline{CAS}$ ≦ 0.2V, WE ≧ V_{CC} − 0.2V output open						5	10	5.7	11.4	mA

Note 3 : Current flowing into a CARD is positive, out is negative.

4 : I_{CC1} (AV), I_{CC3} (AV), I_{CC4} (AV) and I_{CC6} (AV) are dependent on cycle rate. Specified values are obtained at the fastest cycle rate.

5 : I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the outputs open.

6 : Column Address can be changed once or less while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.

SWITCHING CHARACTERISTICS (T_a = 0 ~ 55℃, V_{CC} = 5 V ± 5 %, GND = 0 V): (Note 7)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_{CAC}	Access time from $\overline{CAS}$ (Note 8, 9)		27	ns
t_{RAC}	Access time from $\overline{RAS}$ (Note 8, 10)		70	ns
t_{CAA}	Column Address access time (Note 8, 11)		42	ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (Note12)	0	27	ns

Note 7 : An initial pause of 500 μsec is required after power-up followed by any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles before proper device operation is achieved. Note that $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods of $\overline{RAS}$ inactivity before proper device operation is achieved.

8 : Measured with a load circuit equivalent to 2 TTL loads and 100pF.

9 : Assume that $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$.

10 : Assume that $t_{RCD} \leq t_{RCD(max)}$ and $t_{RAD} \leq t_{RAD(max)}$.

11 : Assume that $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$.

12 : $t_{OFF(max)}$ define the time at which the output achieves the high impedance state ($|I_{out}| \leq 10\,\mu A$ or $20\,\mu A$) and are not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

TIMING REQUIREMENTS (T_a = 0 ~ 55℃, V_{CC} = 5V ± 5 %, GND = 0 V) : (Note 13, 14)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_{REF}	Refresh cycle time		32	ms
t_{REF}	Refresh cycle time ($\overline{CAS}$ before $\overline{RAS}$ refresh cycling)		128	ms
t_{RP}	$\overline{RAS}$ high pulse width	50		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (Note15)	20	43	ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low (Note16)	17		ns
t_{RPC}	Precharge to $\overline{CAS}$ active time.	0		ns
t_{CPN}	$\overline{CAS}$ high pulse width	10		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low (Note 17)	17	28	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low	10		ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low (Note18)	5	10	ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low	10		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low	15		ns
t_T	Transition time (Note19)	3	50	ns

Note 13 : The timing requirements are assumed t_T = 5 ns.

14 : V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals.

15 : t_{RCD}(max) is specified as a reference point only.
If $t_{RCD} \geq t_{RCD}$(max), access time is defined as t_{CAC} and t_{CAA}.

16 : t_{CRP} requirement is applicable for all $\overline{RAS}/\overline{CAS}$ cycles.

17 : t_{RAD}(max) is specified as a reference point only.
If $t_{RAD} \geq t_{RAD}$(max) and $t_{ASC} \leq t_{ASC}$(max), access time is assumed by t_{CAA} for read cycle.

18 : t_{ASC}(max) is specified as a reference point only of address access time.

19 : t_T is measured between V_{IH}(min) and V_{IL}(max).

Read and Refresh Cycles

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_{RC}	Read cycle time	130		ns
t_{RAS}	$\overline{RAS}$ low pulse width	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	70		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	27		ns
t_{RSC}	Read setup time before $\overline{CAS}$ low	5		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high	0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high	10		ns

Write Cycle (Early Write)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_{WC}	Write cycle time	130		ns
t_{RAS}	$\overline{RAS}$ low pulse width	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	70		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	27		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low	5		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	15		ns
t_{DS}	Data setup time	10		ns
t_{DH}	Data hold time after $\overline{CAS}$ low	22		ns

Page Mode Cycle (Read, Early Write)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_{PC}	Read, Write cycle time	55		ns
t_{CP}	$\overline{CAS}$ high pulse width	10		ns
t_{RAS}	$\overline{RAS}$ low pulse width (Note 20)	125	100000	ns

Note 20 : $t_{RAS}(min)$ is specified by the following formula as two cycles of $\overline{CAS}$ input are executed.
$t_{RAS}(min) = t_{CSH}(min) + t_{PC}(min)$.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 21)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_{CSR}	$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh	20		ns
t_{CHR}	$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh	15		ns

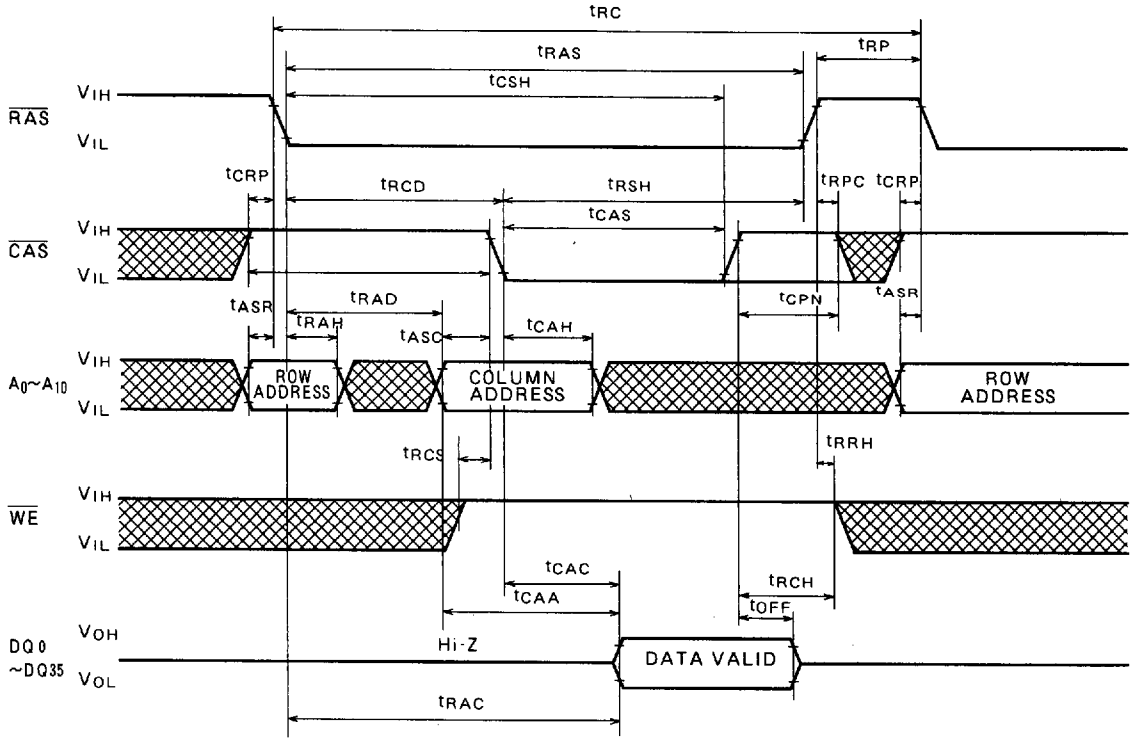
Note 21 : Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Self Refresh Cycle

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_{RASS}	$\overline{RAS}$ low pulse width	100		μs
t_{RPS}	$\overline{CAS}$ high pulse width	130		ns
t_{CHS}	$\overline{RAS}$ hold time after $\overline{RAS}$ high	−50		ns

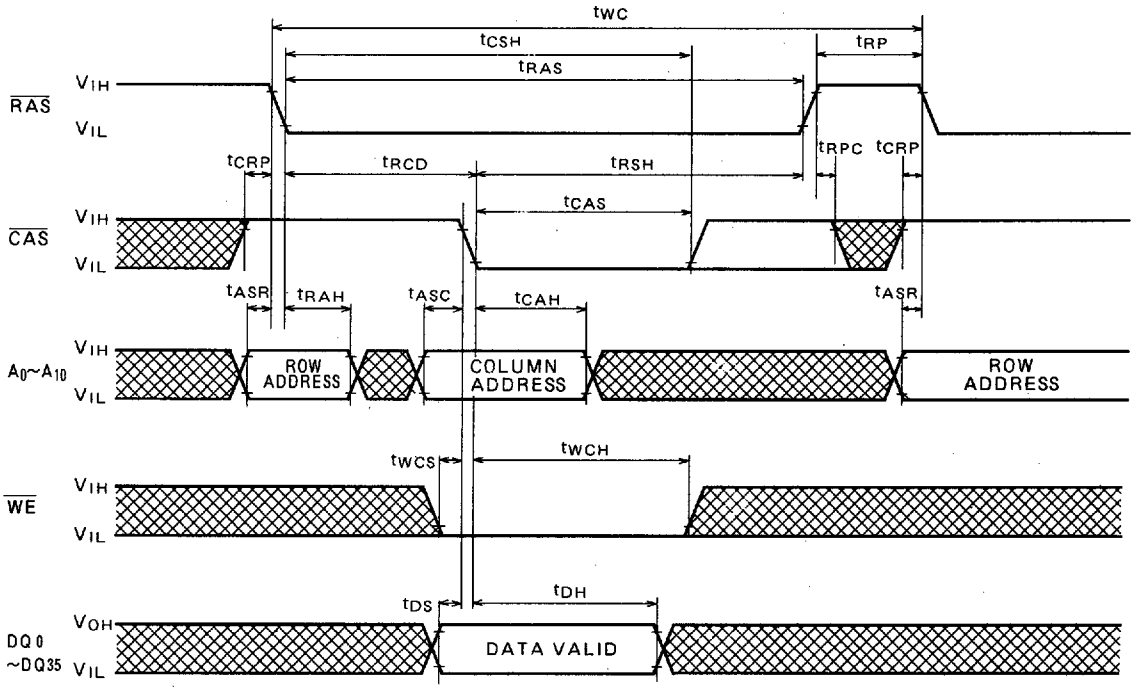
TIMING DIAGRAMS (Note 22)

Read Cycle

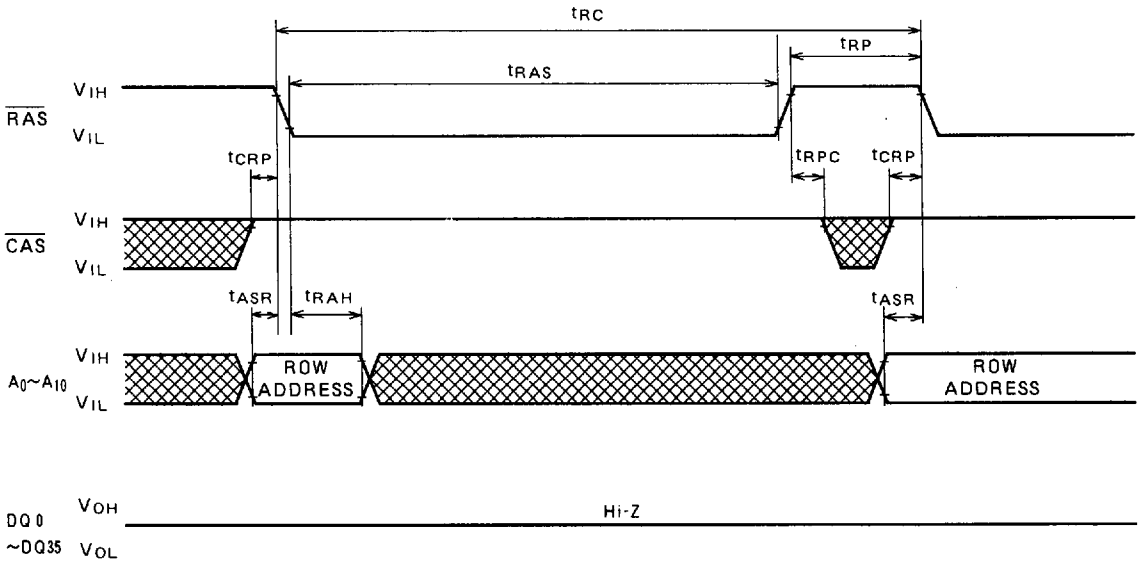


Note 22 : Indicates the don't care input.

Early Write Cycle

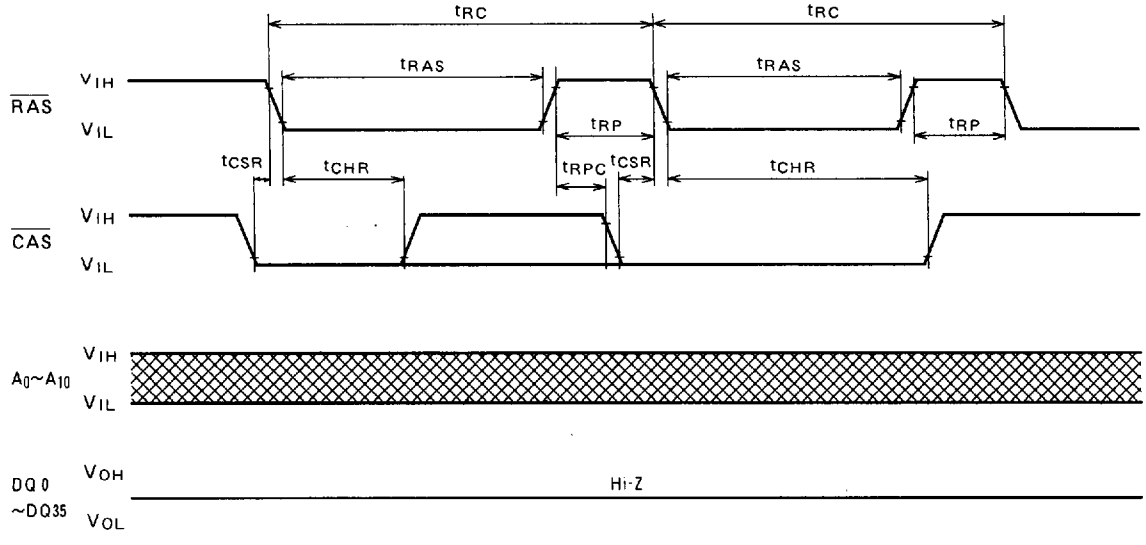


$\overline{RAS}$ only Refresh Cycle (Note 23)



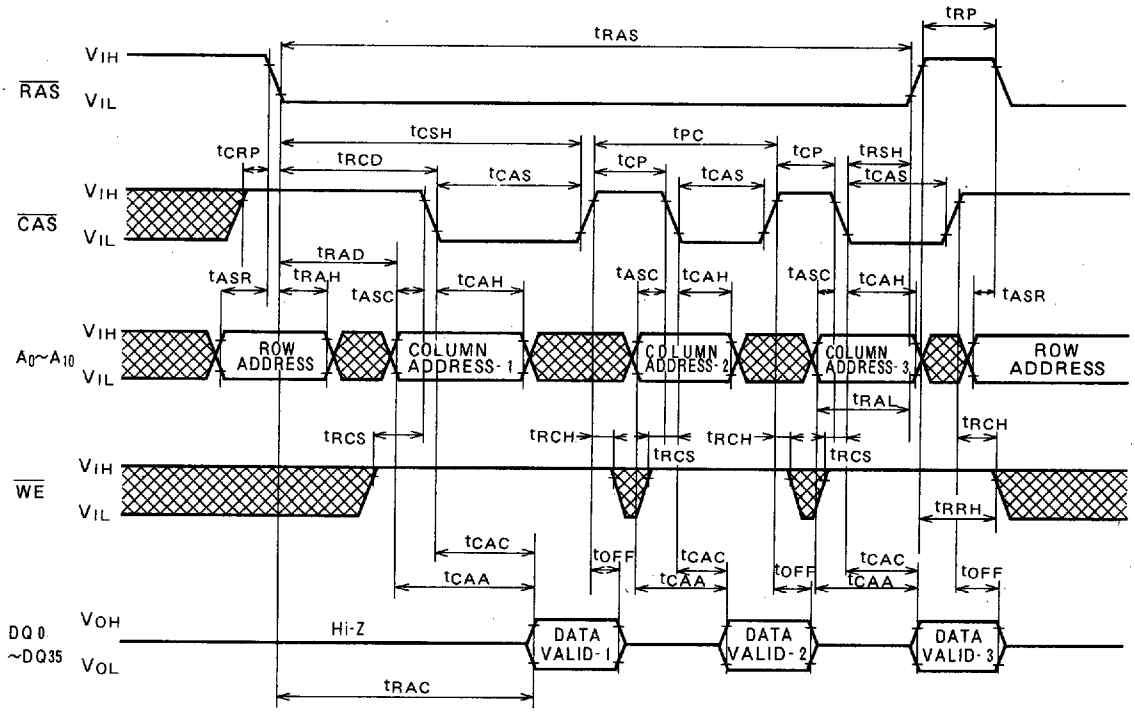
Note 23 : $\overline{WE}$ = don' t care.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 24)

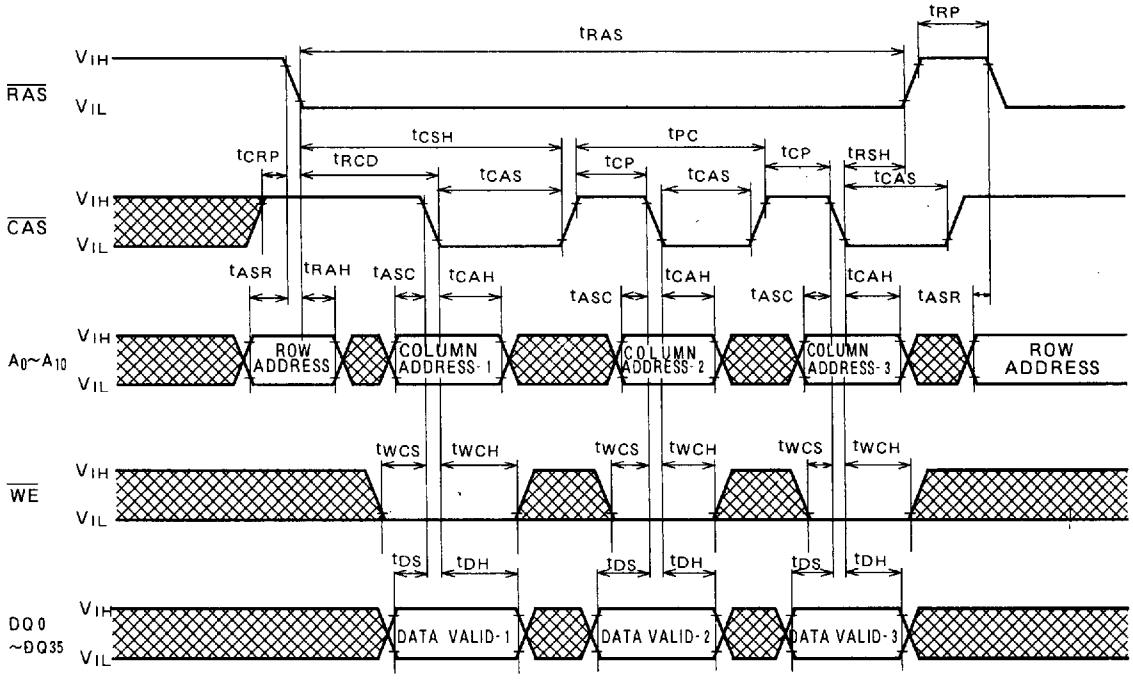


Note 24 : $\overline{WE} = V_{IH}$

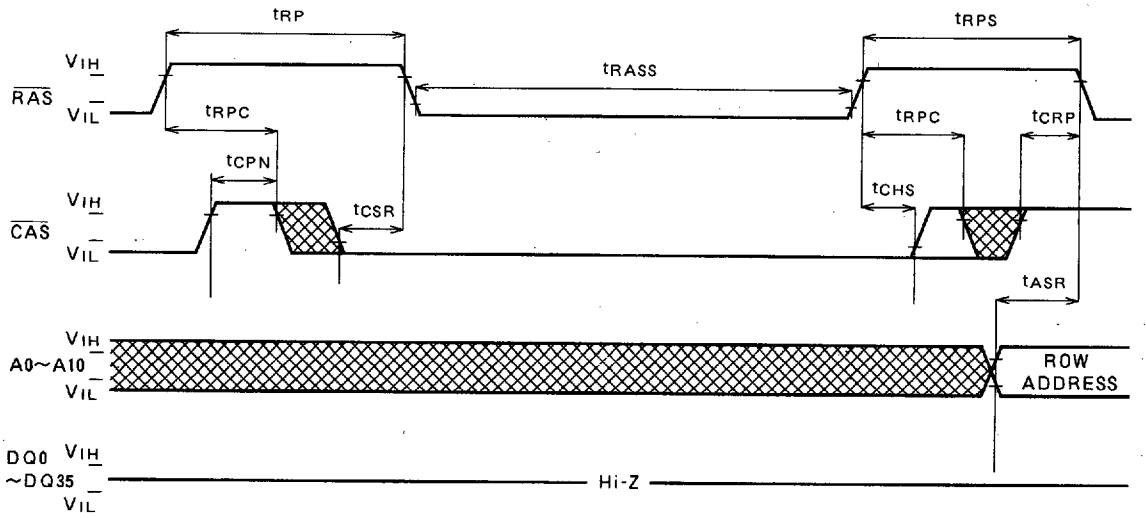
Page-Mode Read Cycle



Page-Mode Early Write Cycle



Self Refresh Cycle (Note 25, 26)



Note 25 : $\overline{WE}$ = VIH

Note 26 : SELF REFRESH ENTRY & EXIT CONDITIONS

(1)In case of distributed refresh

The last/first full refresh cycles (2 K) must be made within t_{NS}/t_{SN} before/after self refresh, on the condition of $t_{NS} \leqq 32ms$ and $t_{SN} \leqq 32ms$.

(2)In case of burst refresh

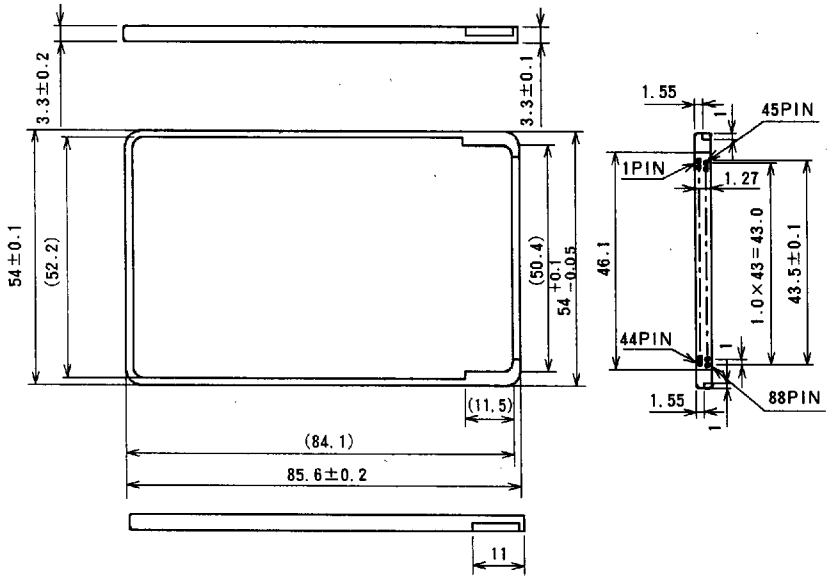
The last/first full refresh cycles (2 K) must be made within t_{NS}/t_{SN} before/after self refresh, on the condition of $t_{NS}+t_{SN} \leqq 32ms$.

CARD DIMENSIONS

88P-001

TWO - PIECE 88 pin (5V connector keying)

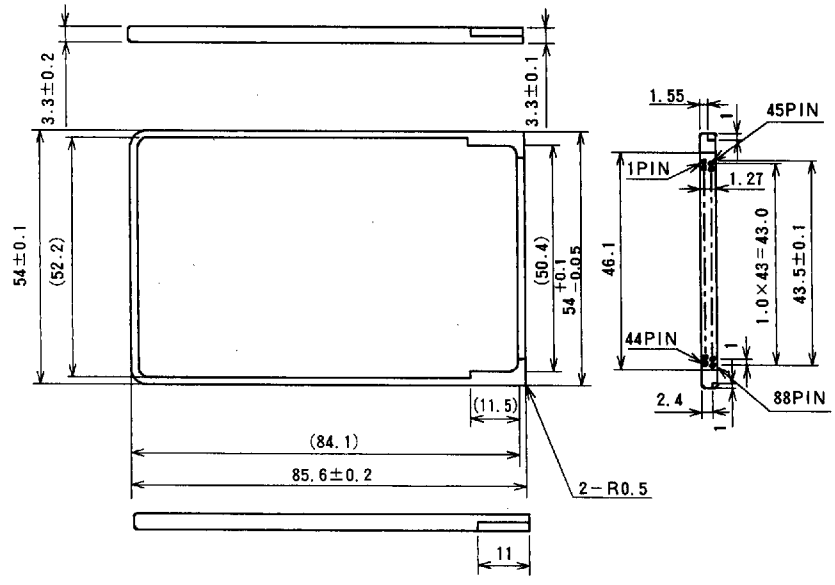
Dimensions in mm



88P-002

TWO - PIECE 88 pin (3.3V connector keying)

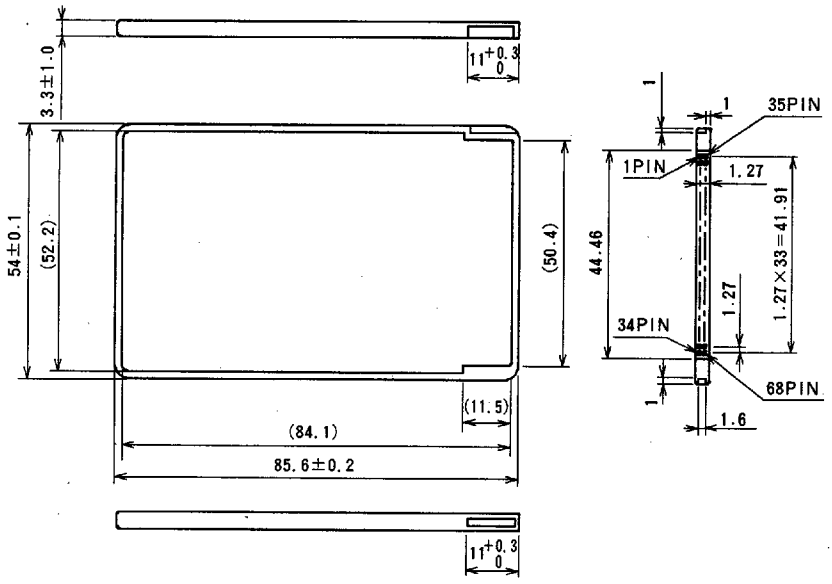
Dimensions in mm



CARD DIMENSIONS

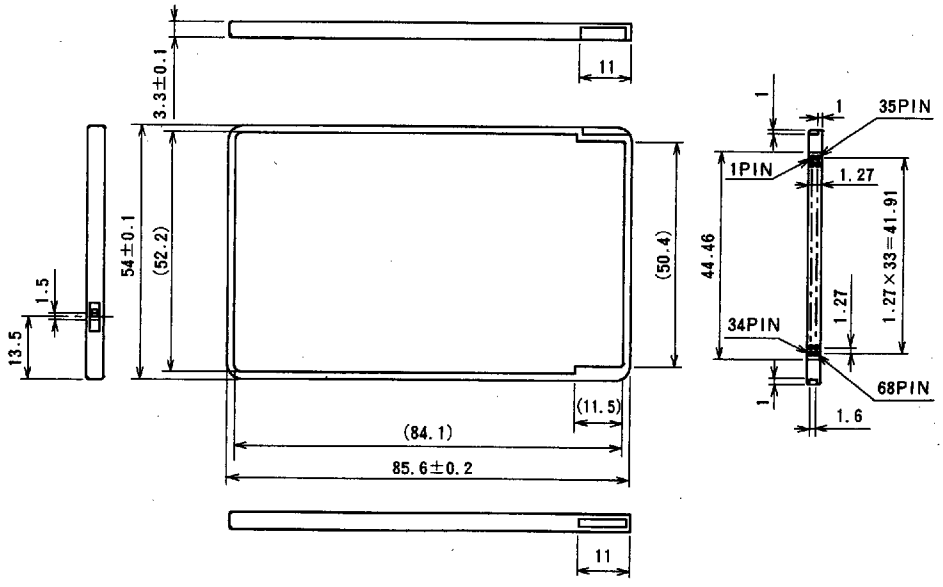
68P-001 TWO - PIECE 68 pin

Dimensions in mm



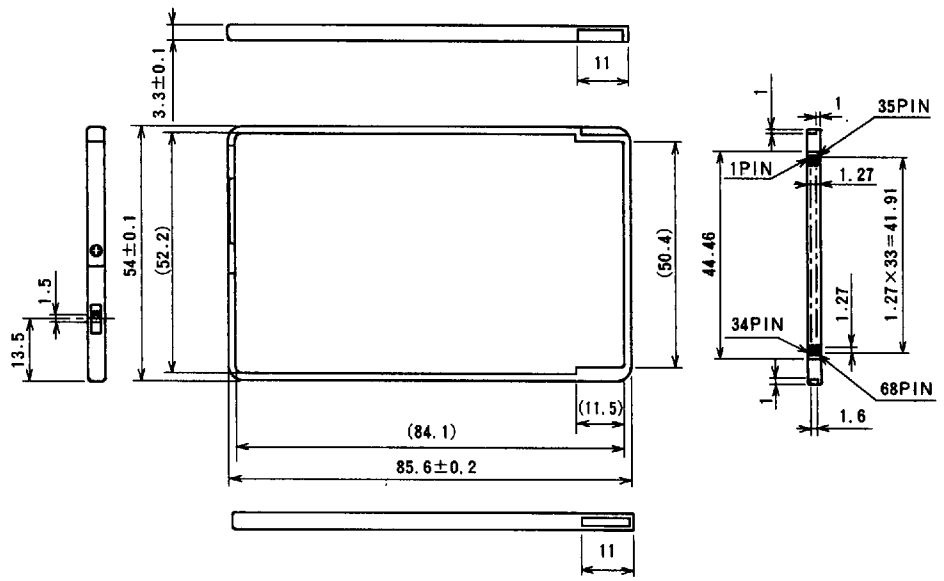
68P-002 TWO - PIECE 68 pin (with WP switch)

Dimensions in mm

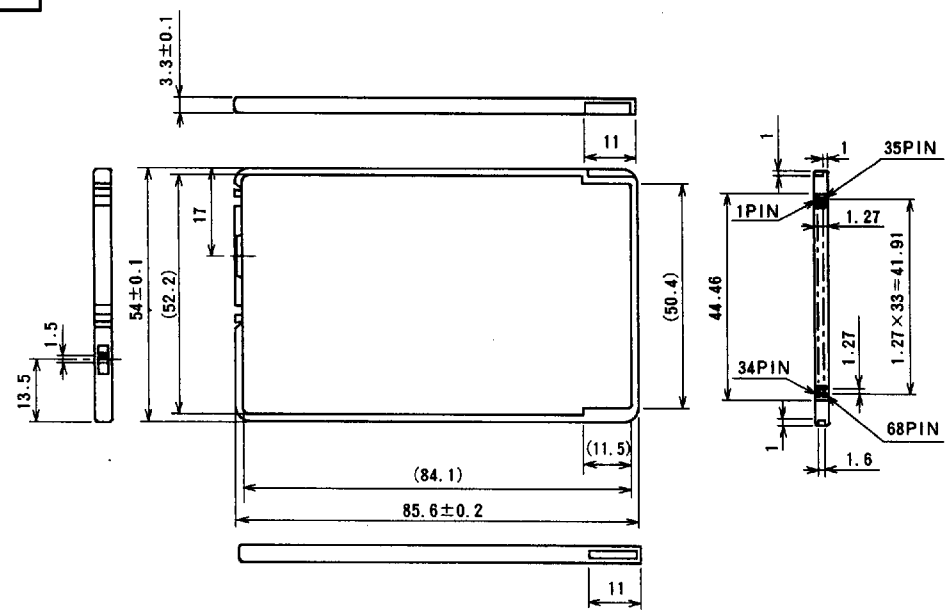


CARD DIMENSIONS

68P-003 TWO - PIECE 68 pin (with WP switch and battery) Dimensions in mm



68P-004 TWO - PIECE 68 pin (with WP switch and battery) Dimensions in mm

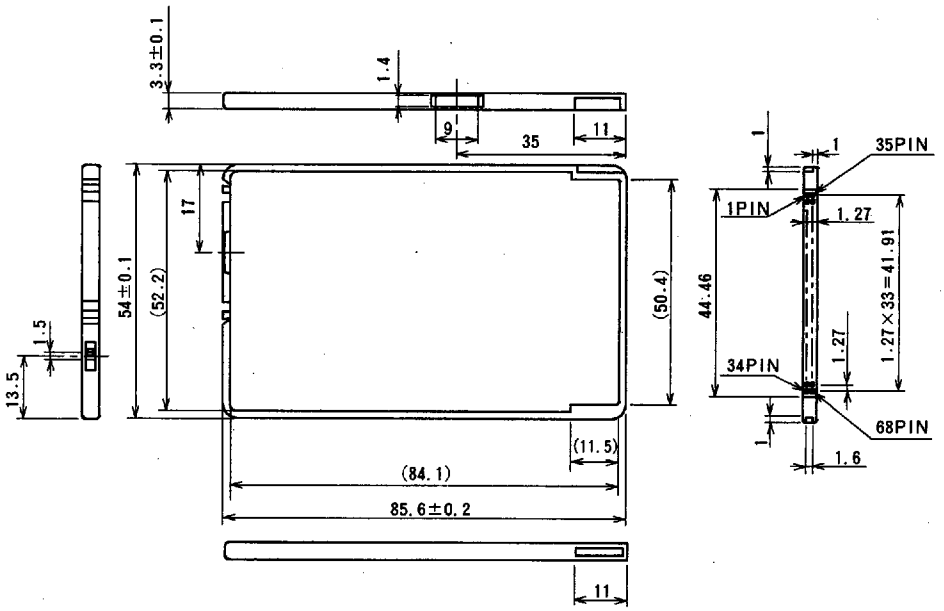


CARD DIMENSIONS

68P-005

TWO - PIECE 68 pin (with WP switch, main battery and auxialiary battery)

Dimensions in mm



60P-004

TWO - PIECE 60 pin (with WP switch and battery)

Dimensions in mm