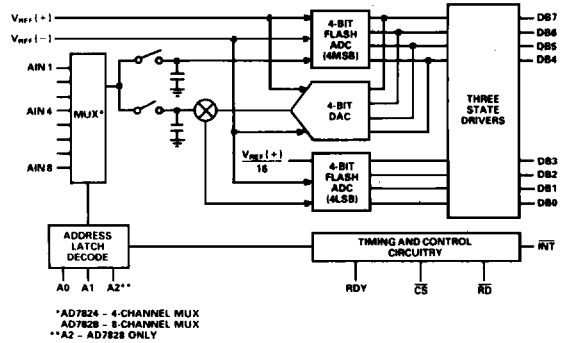


AD7824/AD7828

FEATURES

- 4- or 8-Analog Input Channels**
- Built-in Track/Hold Function**
- 10kHz Signal Handling on Each Channel**
- Fast Microprocessor Interface**
- Single +5V Supply**
- Low Power: 50mW**
- Fast Conversion Rate, 2.5μs/Channel**
- Tight Error Specification: 1/2LSB**

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7824 and AD7828 are high-speed, multichannel, 8-bit ADCs with a choice of 4 (AD7824) or 8 (AD7828) multiplexed analog inputs. A half-flash conversion technique gives a fast conversion rate of 2.5μs per channel and the parts have a built-in track/hold function capable of digitizing full-scale signals of 10kHz (157mV/μs slew rate) on all channels. The AD7824 and AD7828 operate from a single +5V supply and have an analog input range of 0 to +5V, using an external +5V reference.

Microprocessor interfacing of the parts is simple, using standard Chip Select (\overline{CS}) and Read (\overline{RD}) signals to initiate the conversion and read the data from the three-state data outputs. The half-flash conversion technique means that there is no need to generate a clock signal for the ADC. The AD7824 and AD7828 can be interfaced easily to most popular microprocessors.

The AD7824 and AD7828 are fabricated in an advanced, all ion-implanted, Linear-Compatible CMOS process (LC²MOS) and have low power dissipation of 40mW (typ). The AD7824 is available in a 0.3" wide, 24-pin "skinny" DIP, while the AD7828 is available in a 0.6" wide, 28-pin DIP and in 28-terminal surface mount packages.

PRODUCT HIGHLIGHTS

1. 4- or 8-channel input multiplexer gives cost-effective space-saving multichannel ADC system.
2. Fast conversion rate of 2.5μs/channel features a per channel sampling frequency of 100kHz for the AD7824 or 50kHz for the AD7828.
3. Built-in track-hold function allows handling of 4- or 8-channels up to 10kHz bandwidth (157mV/μs slew rate).
4. Tight total unadjusted error spec and channel-to-channel matching eliminate the need for user trims.
5. Single +5V supply simplifies system power requirements.
6. Fast, easy-to-use digital interface allows connection to most popular microprocessors with minimal external components. No clock signal is required for the ADC.

SPECIFICATIONS

($V_{DD} = +5V$, $V_{REF(+)} = +5V$, $V_{REF(-)} = GND = 0V$ unless otherwise noted. All specifications T_{min} to T_{max} unless otherwise noted. Specifications apply for Mode 0.)

AD7824/AD7828

Parameter	K Version ¹	L Version	B, T Versions	C, U Versions	Units	Conditions/Comments
ACCURACY						
Resolution	8	8	8	8	Bits	
Total Unadjusted Error ²	± 1	± 1/2	± 1	± 1/2	LSB max	
Minimum Resolution for which No Missing Codes are guaranteed	8	8	8	8	Bits	
Channel to Channel Mismatch	± 1/4	± 1/4	± 1/4	± 1/4	LSB max	
REFERENCE INPUT						
Input Resistance	1.0/4.0	1.0/4.0	1.0/4.0	1.0/4.0	k Ω min/k Ω max	
$V_{REF(+)}$ Input Voltage Range	$V_{REF(-)}$ / V_{DD}	$V_{REF(-)}$ / V_{DD}	$V_{REF(-)}$ / V_{DD}	$V_{REF(-)}$ / V_{DD}	V min/V max	
$V_{REF(-)}$ Input Voltage Range	GND/ $V_{REF(+)}$	GND/ $V_{REF(+)}$	GND/ $V_{REF(+)}$	GND/ $V_{REF(+)}$	V min/V max	
ANALOG INPUT						
Input Voltage Range	$V_{REF(-)}$ / $V_{REF(+)}$	$V_{REF(-)}$ / $V_{REF(+)}$	$V_{REF(-)}$ / $V_{REF(+)}$	$V_{REF(-)}$ / $V_{REF(+)}$	V min/V max	
Input Leakage Current	± 3	± 3	± 3	± 3	μ A max	Analog Input Any Channel
Input Capacitance ³	45	45	45	45	pF typ	0 to + 5V
LOGIC INPUTS						
RD, CS, A0, A1 & A2						
V_{INH}	2.4	2.4	2.4	2.4	V min	
V_{INL}	0.8	0.8	0.8	0.8	V max	
I_{INH}	1	1	1	1	μ A max	
I_{INL}	- 1	- 1	- 1	- 1	μ A max	
Input Capacitance ³	8	8	8	8	pF max	Typically 5pF
LOGIC OUTPUTS						
DB0-DB7 & INT						
V_{OH}	4.0	4.0	4.0	4.0	V min	$I_{SOURCE} = 360\mu A$
V_{OL}	0.4	0.4	0.4	0.4	V max	$I_{SINK} = 1.6mA$
I_{OUT} (DB0-DB7)	± 3	± 3	± 3	± 3	μ A max	Floating State Leakage
Output Capacitance ³	8	8	8	8	pF max	Typically 5pF
RDY						
V_{OL} ⁴	0.4	0.4	0.4	0.4	V max	$I_{SINK} = 2.6mA$
I_{OUT}	± 3	± 3	± 3	± 3	μ A max	Floating State Leakage
Output Capacitance	8	8	8	8	pF max	Typically 5pF
SLEW RATE, TRACKING³						
	0.7	0.7	0.7	0.7	V/ μ s typ	
	0.157	0.157	0.157	0.157	V/ μ s max	
POWER SUPPLY						
V_{DD}	5	5	5	5	Volts	± 5% for Specified Performance
I_{DD} ⁵	16	16	20	20	mA max	CS = RD = 2.4V
Power Dissipation	50	50	50	50	mW typ	
	80	80	100	100	mW max	
Power Supply Sensitivity	± 1/4	± 1/4	± 1/4	± 1/4	LSB max	± 1/16LSB typ $V_{DD} = 5V \pm 5\%$

NOTES

¹Temperature Ranges are as follows:

K, L Versions; 0 to + 70°C

B, C Versions; - 40°C to + 85°C

T, U Versions; - 55°C to + 125°C

²Total Unadjusted Error includes offset, full-scale and linearity errors.

³Sample tested at 25°C by Product Assurance to ensure compliance.

⁴RDY is an open drain output.

⁵See Typical Performance Characteristics.

Specifications subject to change without notice.

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AD7824/AD7828

TIMING CHARACTERISTICS¹ ($V_{DD} = +5V$; $V_{REF}(+) = +5V$; $V_{REF}(-) = GND = 0V$ unless otherwise stated)

Parameter	Limit at 25°C (All Grades)	Limit at T_{min}, T_{max} (K, L, B, C Grades)	Limit at T_{min}, T_{max} (T, U Grades)	Units	Conditions/Comments
t_{CSS}	0	0	0	ns min	\overline{CS} to \overline{RD} Setup Time
t_{CSH}	0	0	0	ns min	\overline{CS} to \overline{RD} Hold Time
t_{AS}	0	0	0	ns min	Multiplexer Address Setup Time
t_{AH}	30	35	40	ns min	Multiplexer Address Hold Time
t_{RDY}^2	40	60	60	ns max	\overline{CS} to RDY Delay. Pull-Up Resistor 5k Ω .
t_{CRD}	2.0	2.4	2.8	μs max	Conversion Time, Mode 0
t_{ACC1}^3	85	110	120	ns max	Data Access Time after \overline{RD}
t_{ACC2}^3	50	60	70	ns max	Data Access Time after \overline{INT} , Mode 0
t_{INTH}^2	40	65	70	ns typ	\overline{RD} to \overline{INT} Delay
	75	100	100	ns max	
t_{DH}^4	60	70	70	ns max	Data Hold Time
t_P	500	500	600	ns min	Delay Time between Conversions
t_{RD}	60	80	80	ns min	Read Pulse Width, Mode 1
	600	500	400	ns max	

NOTES

¹Sample tested at 25°C to ensure compliance. All input control signals are specified with $t_r = t_f = 20ns$ (10% to 90% of +5V) and timed from a voltage level of 1.6V.

² $C_L = 50pF$.

³Measured with load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.

⁴Defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.

Specifications subject to change without notice.

AD7824		AD7828			CHANNEL
A1	A0	A2	A1	A0	
0	0	0	0	0	AIN 1
0	1	0	0	1	AIN 2
1	0	0	1	0	AIN 3
1	1	0	1	1	AIN 4
		1	0	0	AIN 5
		1	0	1	AIN 6
		1	1	0	AIN 7
		1	1	1	AIN 8

Table 1. Truth Table for Input Channel Selection

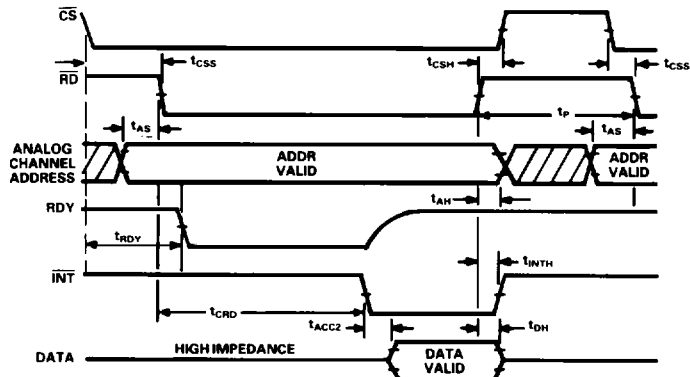


Figure 1. Mode 0 Timing Diagram

ABSOLUTE MAXIMUM RATINGS*

($T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{DD}	0V, +7V
Digital Input Voltage to GND (\overline{RD} , \overline{CS} , A0, A1 & A2)	-0.3V, $V_{DD} + 0.3V$
Digital Output Voltage to GND (DB0, DB7, RDY & INT)	-0.3V, $V_{DD} + 0.3V$
$V_{REF} (+)$ to GND	$V_{REF} (-)$, $V_{DD} + 0.3V$
$V_{REF} (-)$ to GND	0V, $V_{REF} (+)$
Analog Input (Any Channel)	-0.3V, $V_{DD} + 0.3V$
Operating Temperature Range	
Commercial (K, L Versions)	0 to +70°C

Industrial (B, C Versions)	-25°C to +85°C
Extended (T, U Versions)	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C
Power Dissipation (Any Package) to +75°C	450mW
Derates above +75°C by	6mW/°C

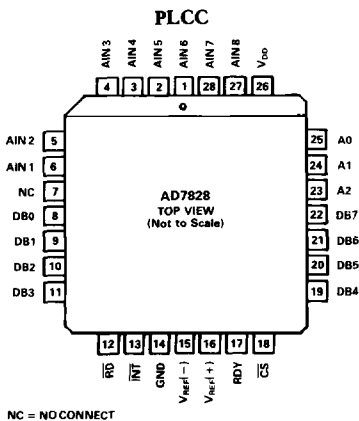
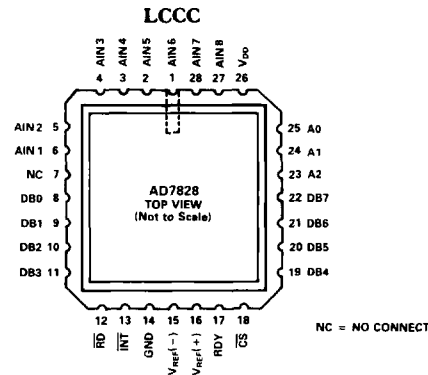
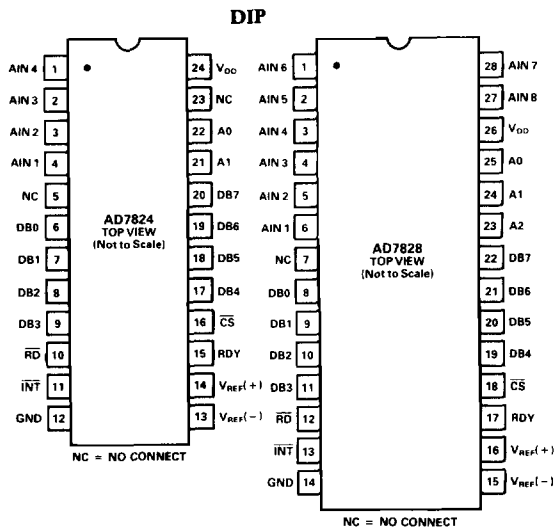
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



PIN CONFIGURATIONS



ORDERING GUIDE

Model	Temperature Range	Total Unadjusted Error (LSBs)	Package Option ¹
AD7824KN	0 to +70°C	±1	N-24
AD7824LN	0 to +70°C	±1/2	N-24
AD7824KR	0 to +70°C	±1	R-24
AD7824BQ	-40°C to +85°C	±1	Q-24
AD7824CQ	-40°C to +85°C	±1/2	Q-24
AD7824TQ ²	-55°C to +125°C	±1	Q-24
AD7824UQ ²	-55°C to +125°C	±1/2	Q-24
AD7828KN	0 to +70°C	±1	N-28
AD7828LN	0 to +70°C	±1/2	N-28
AD7828KP	0 to +70°C	±1	P-28A
AD7828LP	0 to +70°C	±1/2	P-28A
AD7828BQ	-40°C to +85°C	±1	Q-28
AD7828CQ	-40°C to +85°C	±1/2	Q-28
AD7828TQ ²	-55°C to +125°C	±1	Q-28
AD7828UQ ²	-55°C to +125°C	±1/2	Q-28
AD7828TE ²	-55°C to +125°C	±1	E-28A
AD7828UE ²	-55°C to +125°C	±1/2	E-28A

NOTES

¹N = Plastic DIP; Q = Hermetic DIP, R = Small Outline IC; P = Plastic Leaded Chip Carrier; E = Leadless Ceramic Chip Carrier. For outline information see Package Information section.

²Available to /883B processing only. Contact our local sales office for military data sheet. For U.S. Standard Military Drawing (SMD) see DESC Drawing #5692-88764.