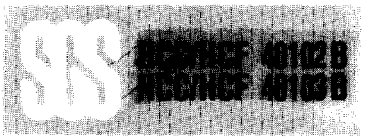
COS/MOS INTEGRATED CIRCUITS

40102B



8-STAGE PRESETTABLE SYNCHRONOUS DOWN COUNTERS
40102B 2-DECADE BCD TYPE
40103B 8-BIT BINARY TYPE

- SYNCHRONOUS OR ASYNCHRONOUS PRESET
- MEDIUM-SPEED OPERATION: f_{CL} = 3.6 MHz (TYP.) @ V_{DD} = 10V
- CASCADABLE
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100 nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD No. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"

The **HCC 40102B, HCC 40103B,** (extended temperature range) and the **HCF 40102B, HCF 40103B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and ceramic flat package. The **HCC/HCF 40102B,** and **HCC/HCF 40103B** consist of an 8-stage synchronous down counter with a single output which is active when the internal count is zero. The **HCC/HCF 40102B** is configured as two cascaded 4-bit BCD counters, and the **HCC/HCF 40103B** contains a single 8-bit binary counter. Each type has control inputs for enabling or disabling the clock, for clearing the counter to its maximum count, and for presetting the counter either synchronously or asynchronously. All control inputs and the CARRY-OUT/ZERO-DETECT output are active-low logic. In normal operation, the counter is decremented by one count on each positive transition of the CLOCK. Counting is inhibited when the CARRY-IN/COUNTER ENABLE ($\overline{CI/CE}$) input is high. The CARRY-OUT/ZERO-DETEC ($\overline{CO/ZD}$) output goes low when the count reaches zero if the $\overline{CI/CE}$ input is low, and remains low for one full clock period. When the SYNCHRONOUS PRESET-ENABLE (SPE) input is low, data at the JAM input is clocked into the counter on the next positive clock transition regardless of the state of the $\overline{CI/CE}$ input. When the ASYNCHRONOUS PRESET-ENABLE ($\overline{APE}$) input is low, data at the JAM inputs is asynchronously forced into the counter regardless of the state of the SPE, $\overline{CI/CE}$, or CLOCK inputs. JAM inputs JO-J7 represent two 4-bit BCD words for the **HCC/HCF 40102B** and a single 8-bit binary word for the **HCC/HCF 40103B**. When the CLEAR ($\overline{CLR}$) input is low, the counter is asynchronously cleared to its maximum count (99_{10} for the **HCC/HCF 40102B** and 255_{10} for the **HCC/HCF 40103B**) regardless of the state of any other input. The precedence relationship between control input is indicated in the truth table. If all control inputs are high at the tieme of zero count, the counters will jump to the maximum count, giving a counting sequence of 100 or 256 clock pulses long. The **HCC/HCF 40102B** and **HCC/HCF 40103B** may be cascaded using the $\overline{CI/CE}$ input and the $\overline{CO/ZD}$ output, in either a synchronous or ripple mode.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage: **HCC** types	-0.5 to 20	V
	HCF types	-0.5 to 18	V
V_i	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op} = full package-temperature range	100	mW
T_{op}	Operating temperature: **HCC** types	-55 to 125	°C
	HCF types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

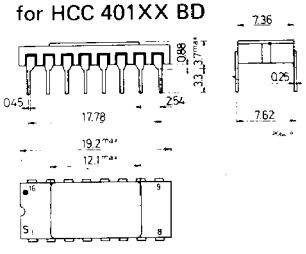
* All voltages are with respect to V_{SS} (GND).

ORDERING NUMBERS:

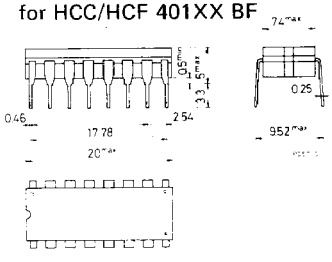
HCC 401XX BD for dual in-line ceramic package
HCC 401XX BF for dual in-line ceramic package, frit seal
HCC 401XX BK for ceramic flat package
HCF 401XX BE for dual in-line plastic package
HCF 401XX BF for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

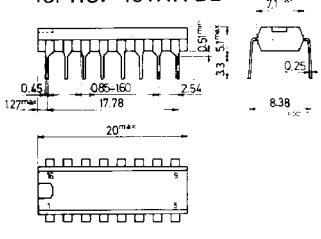
Dual in-line ceramic package for HCC 401XX BD



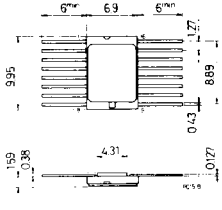
Dual in-line ceramic package for HCC/HCF 401XX BF



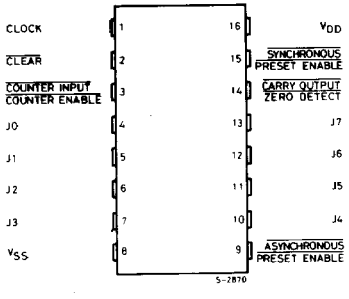
Dual in-line plastic package for HCF 401XX BE



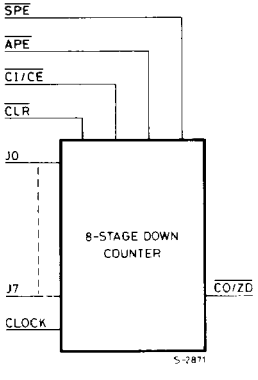
Ceramic flat package for HCC 401XX BK



PIN CONNECTIONS



FUNCTIONAL DIAGRAM

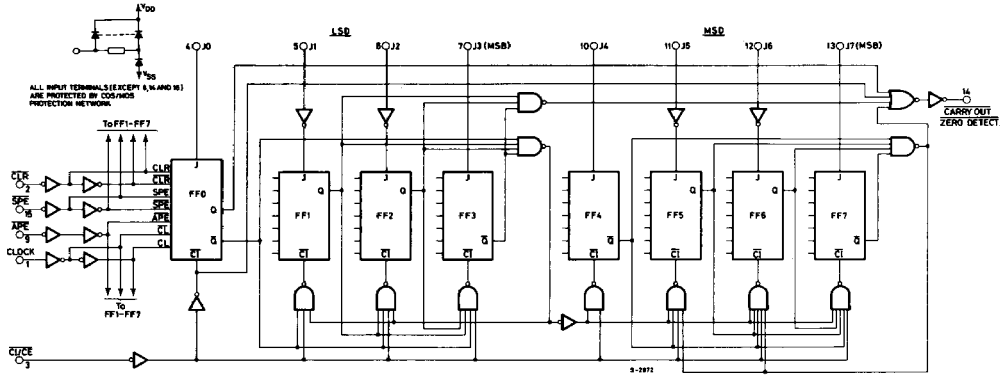


RECOMMENDED OPERATING CONDITIONS

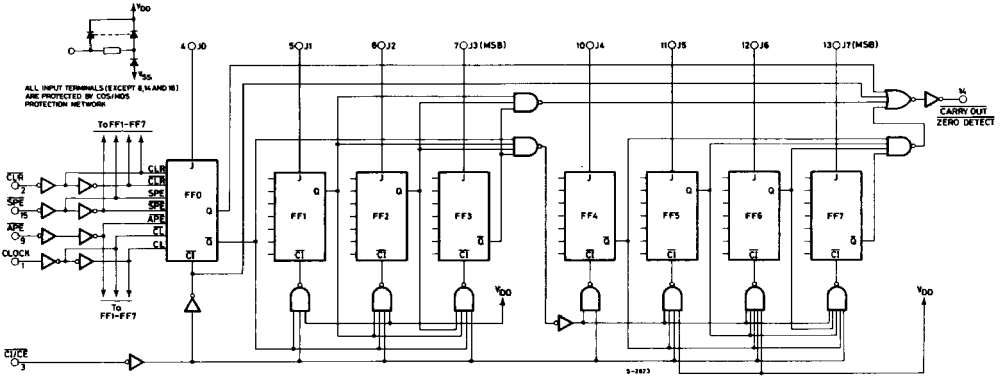
V_{DD}	Supply voltage: **HCC** types	3 to 18	V
	HCF types	3 to 15	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: **HCC** types	-55 to 125	°C
	HCF types	-40 to 85	°C

LOGIC DIAGRAMS

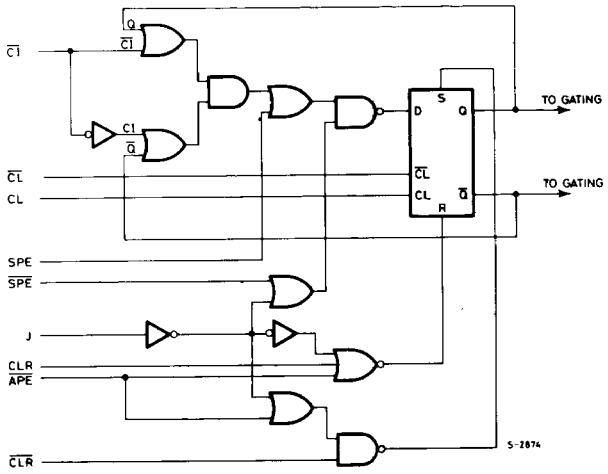
For **40102B**



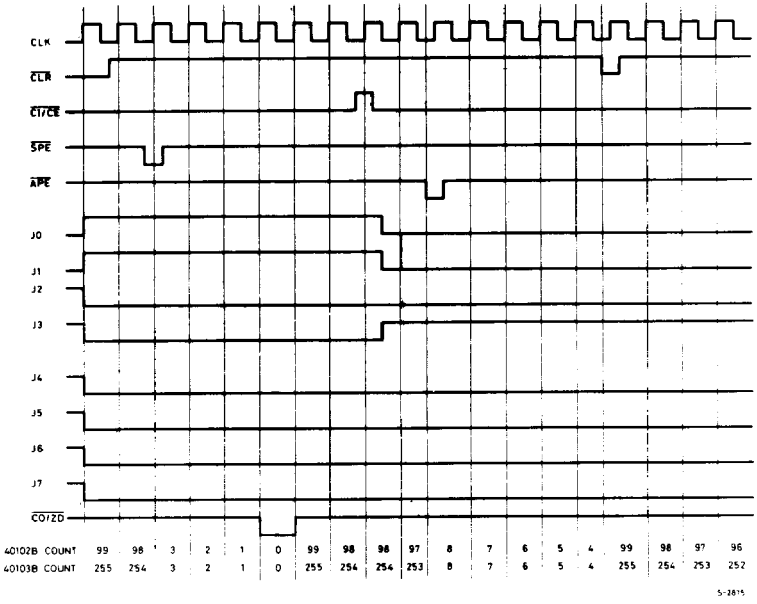
For **40103B**



Detail logic diagram for flip-flops, FF0-FF7 used in logic diagrams for **40102B** and **40103B**



Timing diagram for 40102B and 40103B



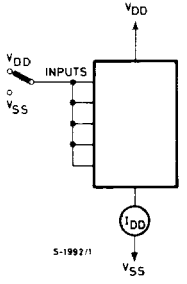
TRUTH TABLE

Control Inputs				Preset Mode	Action
$\overline{CLR}$	$\overline{APE}$	$\overline{SPE}$	$\overline{CI}/CE$		
1	1	1	1	Synchronous	Inhibit counter
1	1	1	0		Count down
1	1	0	X		Preset on next positive clock transition
1	0	X	X	Asynchronous	Preset asynchronously
0	X	X	X		Clear to maximum count

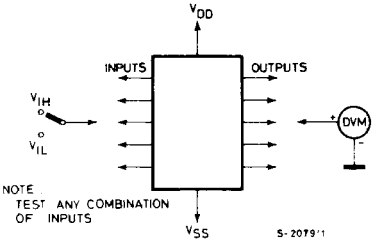
Notes:
1. 0 = Low level
   1 = High level
   X = Don't care
2. Clock connected to clock input.
3. Synchronous operation: changes occur on negative-to-positive clock transitions.
4. JAM inputs: HCC/HCF 40102B BCD; MSD = J7, J6, J5, J4 (J7 is MSB)
   LSD = J3, J2, J1, J0 (J3 is MSB)
   HCC/HCF 40103B Binary; MSB = J7, LSB = J0

TEST CIRCUITS

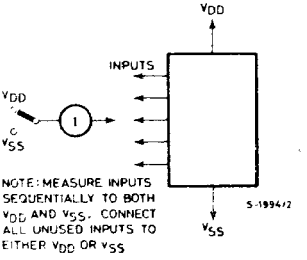
Quiescent device current



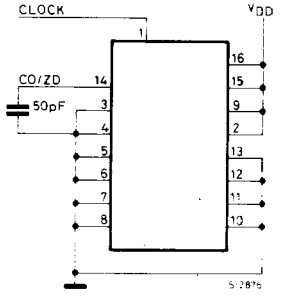
Input voltage



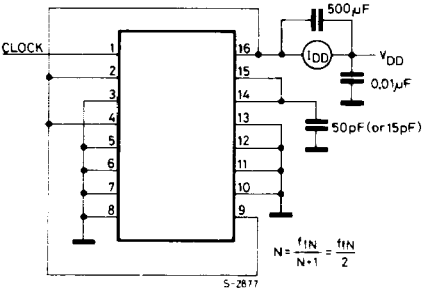
Input current



Maximum clock frequency



Dynamic power dissipation



STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

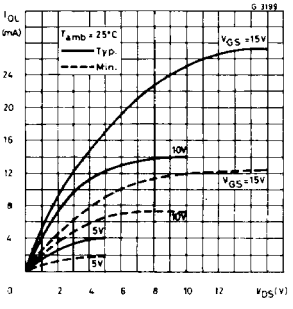
Parameter			Test conditions V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	Values T_{Low}* Min.	T_{Low}* Max.	25°C Min.	25°C Typ.	25°C Max.	T_{High}* Min.	T_{High}* Max.	Unit
I_L	Quiescent current	HCC types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		HCF types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.53		-1.36	-3.2		-1.1		
			0/ 5	4.6		5	-0.52		-0.44	-1		-0.36		
			0/10	9.5		10	-1.3		-1.1	-2.6		-0.9		
			0/15	13.5		15	-3.6		-3.0	-6.8		-2.4		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	HCC types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		± 1	μA
		HCF types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		± 1	
C_I	Input capacitance			Any input						5	7.5			pF

* T_{Low} = - 55°C for **HCC** device: -40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device: +85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}= 5V
2V min. with V_{DD}= 10V
2.5V min. with V_{DD}= 15V

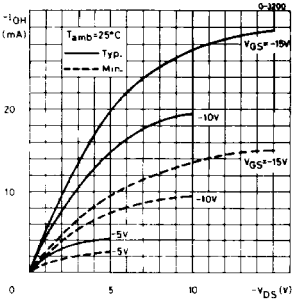
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50 pF, R_L = 200 kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall time = 20 ns)

Parameter		Test conditions	Values				Unit
			V_{DD}(V)	Min.	Typ.	Max.	
t_{PHL}, t_{PLH} Propagation delay time	Clock-to-out		5		300	600	ns
			10		130	260	
			15		95	190	
	Carry In/Counter Enable-to-Output		5		200	400	ns
			10		90	180	
			15		65	130	
	Asynchronous Preset Enable-to-Output		5		650	1300	
			10		300	600	
			15		200	400	
	$\overline{\text{Clear}}$-to-Output		5		375	750	ns
			10		180	360	
			15		100	200	
t_{THL}, t_{TLH} Transition time			5		100	200	ns
			10		50	100	
			15		40	80	
t_W Pulse width	Clock pulse width		5	300	150		ns
			10	180	90		
			15	80	40		
	$\overline{\text{CLR}}$ pulse width		5	320	160		ns
			10	160	80		
			15	100	50		
	$\overline{\text{APE}}$ pulse width		5	360	180		ns
			10	160	80		
			15	120	60		
t_{setup} Setup time	$\overline{\text{SPE}}$ setup time		5	280	140		ns
			10	140	70		
			15	100	50		
	JAM setup time		5	200	100		ns
			10	80	40		
			15	60	30		
f_{CL} Maximum clock input frequency			5	0.7	1.4		MHz
			10	1.8	3.6		
			15	2.4	4.8		

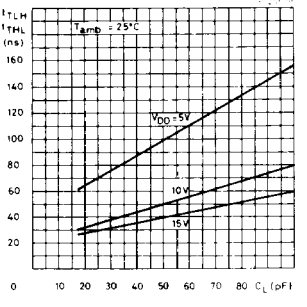
Output low (sink) current characteristics



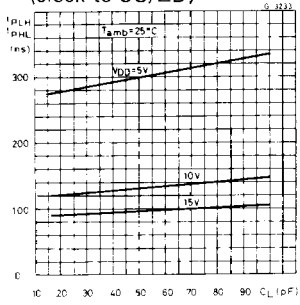
Output high (source) current characteristics



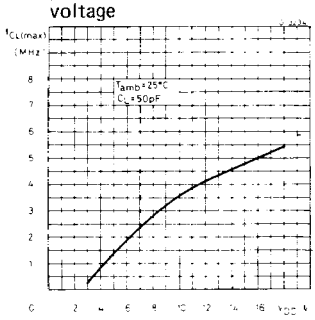
Typical transition time vs. load capacitance



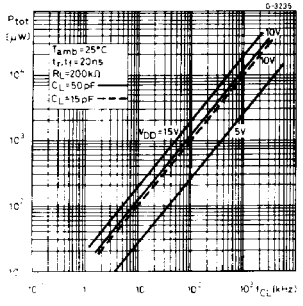
Typical propagation delay time vs. load capacitance (clock to $\overline{CO/ZD}$)



Typical maximum clock input frequency vs. supply voltage

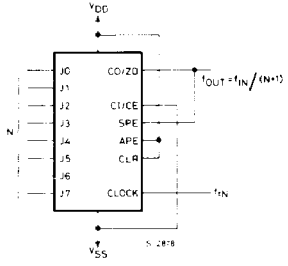


Typical dynamic power dissipation vs. frequency

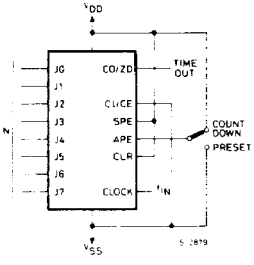


TYPICAL APPLICATIONS

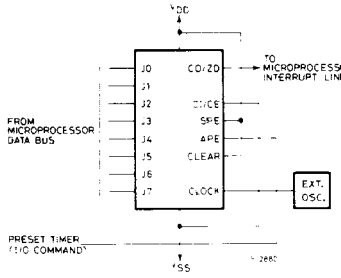
Divide-by-"N" counter



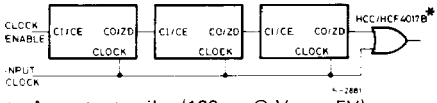
Programmable timer



Microprocessor interrupt timer



Synchronous cascading



* An output spike (160 ns @ V_{DD}= 5V) occurs whenever two or more devices are cascaded in the parallel-clocked mode because the clock-to-carry out delay is greater than the carry-in-to-carry out delay. This spike is eliminated by gating the output of the last device with the clock as shown.

Ripple cascading