Signetics

Military Logic Products

54S181
Arithmetic Logic Unit

4-Bit Arithmetic Logic Unit

Product Specification

FEATURES

- **Provides 16 arithmetic operations: ADD, SUBTRACT, COMPARE, DOUBLE, plus 12 other arithmetic operations**
- **Provides all 16 logic operations of two variables: Exclusive-OR, Compare, AND, NAND, NOR, OR, plus 10 other logic operations**
- **Full lookahead carry for high-speed arithmetic operation on long words**

DESCRIPTION

The 54S181 is a 4-bit high-speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select inputs (S_0-S_3) and the Mode Control Input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active High or active Low operands. The Function Table list these operations.

ORDERING INFORMATION

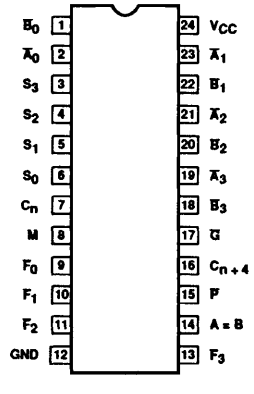
DESCRIPTION	ORDER CODE
24-Pin Ceramic DIP	54S181/BJA
24-Pin Ceramic FlatPack	54S181/BKA
28-Pin Ceramic LLCC	54S181/B3A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54S
Mode	Input	1SUL
$\overline{A}$ or $\overline{B}$	Inputs	3SUL
S	Inputs	4SUL
Carry	Input	5SUL
F_0-F_3 = B, C_{n+4}	Outputs	10SUL
$\overline{G}$	Output	10SUL
$\overline{P}$	Output	10SUL

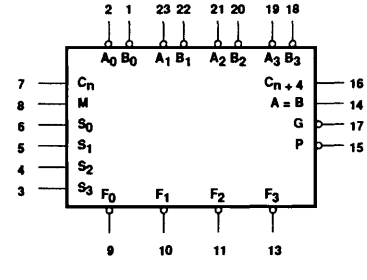
NOTE: Where a 54S Unit Load (SUL) IS 50μA I_{IH} and -2.0mA I_{IL}.

PIN CONFIGURATION



For LLCC Pin Assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC Pin Assignments, see JEDEC Standard No. 2

When the Mode Control Input (M) is High, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control input is Low, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry lookahead between packages using the signals $\overline{P}$ (Carry Propagate) and $\overline{G}$ (Carry Generate). $\overline{P}$ and $\overline{G}$ are not affected by carry in. When speed requirements are not stringent, it can be used in a simple ripple carry mode by connecting the Carry output (C_{n+4}) signal to the Carry input (C_n) of the next unit. For high-speed operation the device is used in conjunction with the '182 carry lookahead circuit. One carry lookahead package is required for each group of four '181 devices. Carry lookahead can be provided at various levels and offers high-speed capability over extremely long word lengths.

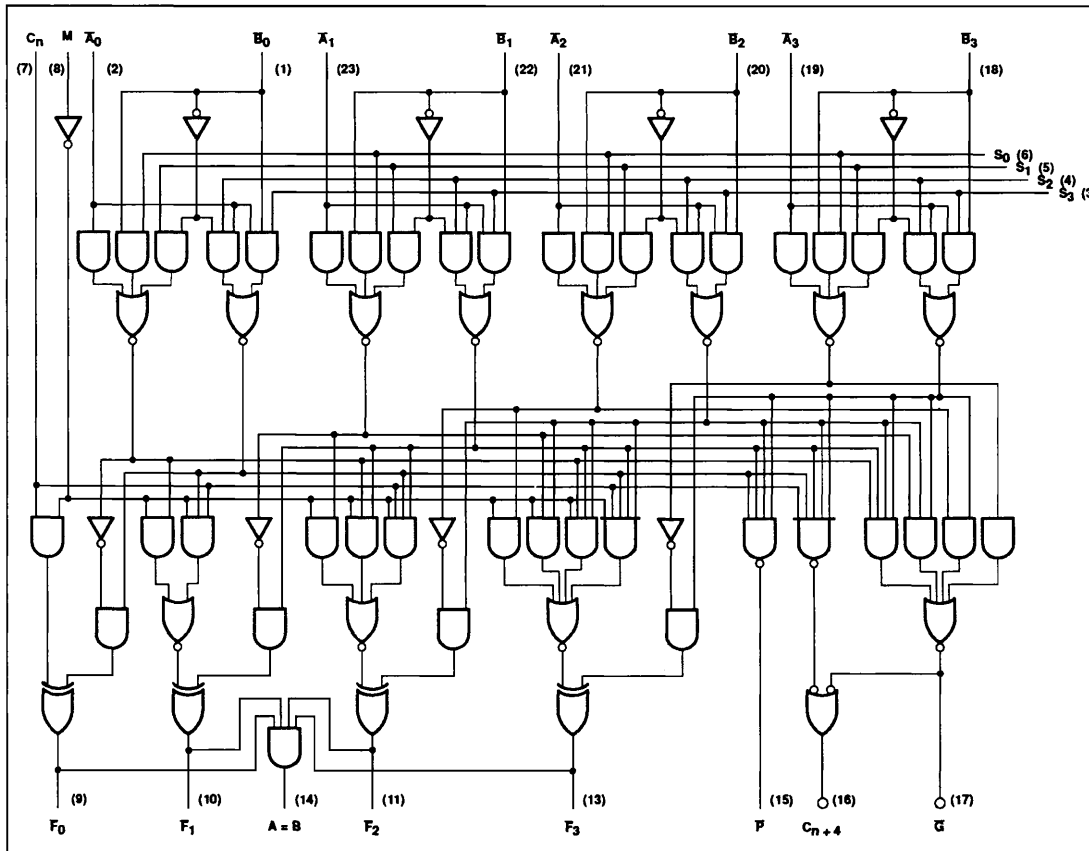
The A = B output from the device goes High when all four F outputs are High and can be used to indicate logic equivalence over 4 bits when the unit is in the subtract mode. The A = B output is open collector and can be wired-AND with other A = B outputs to give a comparison for more than 4 bits. The A = B signal can also be used with the C_{n+4} signal to indicate A > B and A < B.

The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied.

Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus, a carry is generated when there is not underflow and no carry is generated when there is underflow.

As indicated, this device can be used with either active Low inputs producing active Low outputs or with active High inputs producing active High outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

LOGIC DIAGRAM



VCC = Pin 24
GND = Pin 12
( ) = Pin numbers
Pin 14 is O.C.

For LLCC pin assignments, see JEDEC Standard No. 2

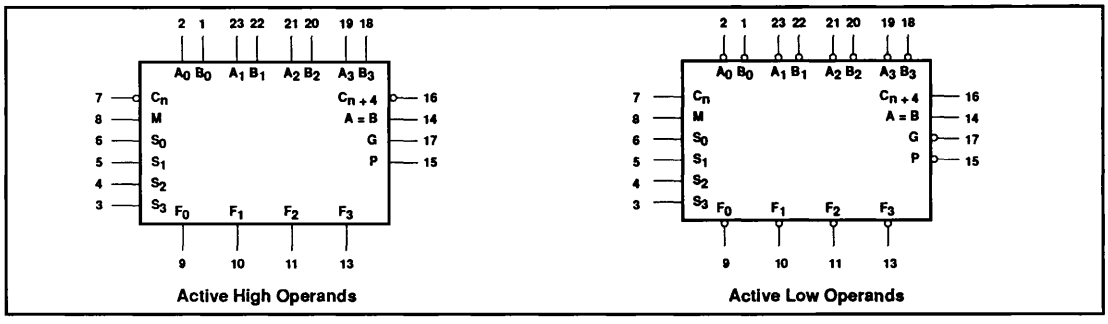
MODE SELECT — FUNCTION TABLE

MODE SELECT INPUTS				ACTIVE HIGH INPUTS & OUTPUTS	
S_3	S_2	S_1	S_0	Logic (M = H)	Arithmetic ** (M = L) (C_n = H)
L	L	L	L	$\overline{A}$	A
L	L	L	H	$\overline{A+B}$	A + B
L	L	H	L	$\overline{A}B$	$A+\overline{B}$
L	L	H	H	Logical 0	minus 1
L	H	L	L	$A\overline{B}$	A plus $A\overline{B}$
L	H	L	H	$\overline{B}$	(A + B) plus $A\overline{B}$
L	H	H	L	$A \oplus B$	A minus B minus 1
L	H	H	H	$A\overline{B}$	AB minus 1
H	L	L	L	$\overline{A}+B$	A plus AB
H	L	L	H	$\overline{A \oplus B}$	A plus B
H	L	H	L	B	(A + $\overline{B}$) plus AB
H	L	H	H	AB	AB minus 1
H	H	L	L	Logical 1	A plus A*
H	H	L	H	$A+\overline{B}$	(A + B) plus A
H	H	H	L	A + B	(A + $\overline{B}$) plus A
H	H	H	H	A	A minus 1

MODE SELECT — FUNCTION TABLE

MODE SELECT INPUTS				ACTIVE LOW INPUTS & OUTPUTS	
S_3	S_2	S_1	S_0	Logic (M = H)	Arithmetic ** (M = L) (C_n = H)
L	L	L	L	$\overline{A}$	A minus 1
L	L	L	H	$\overline{AB}$	AB minus 1
L	L	H	L	$\overline{A}+B$	$A\overline{B}$ minus 1
L	L	H	H	Logical 1	minus 1
L	H	L	L	$\overline{A+B}$	A plus (A + $\overline{B}$)
L	H	L	H	$\overline{B}$	AB plus (A + $\overline{B}$)
L	H	H	L	$\overline{A \oplus B}$	A minus B minus 1
L	H	H	H	$A+\overline{B}$	$A+\overline{B}$
H	L	L	L	$\overline{A}B$	A plus (A + B)
H	L	L	H	$A \oplus B$	A plus B
H	L	H	L	B	$A\overline{B}$ plus (A + B)
H	L	H	H	A + B	A + B
H	H	L	L	Logical 0	A plus A*
H	H	L	H	$A\overline{B}$	AB plus A
H	H	H	L	AB	$A\overline{B}$ plus A
H	H	H	H	A	A

L = Low voltage
H = High voltage level
* = Each bit is shifted to the next more significant position.
** = Arithmetic operations expressed in 2s complement notation.



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	7.0	V
V_I	Input voltage range	-0.5 to +5.5	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				+0.8	V
		+125°			+0.7	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current except A = B				-1000	µA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature range		-55		+125	°C

SUM MODE TEST TABLE I

FUNCTION INPUTS: $S_0 = S_3 = 1$, $S_1 = S_2 = M = 0V$

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply 1	Apply GND	Apply 1	Apply GND	
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	F_i
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	F_i
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{N+4}
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	C_N	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}

NOTE:

1. $2.7V \leq HI \leq V_{CC}$

DIFF MODE TEST TABLE II

FUNCTION INPUTS: $S_0 = S_3 = 1$, $S_1 = S_2 = M = 0V$

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply 1	Apply GND	Apply 1	Apply GND	
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	F_i
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	F_i
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}
t_{PHL} t_{PHL}	C_N	None	None	All $\overline{A}$ and $\overline{B}$	None	Any $\overline{F}$ or C_{n+4}

LOGIC MODE TEST TABLE III

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	FUNCTION INPUTS
		Apply 1	Apply GND	Apply 1	Apply GND		
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	F_i	$S_1 = S_2 = M = 1$ $S_0 = S_3 = 0V$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	F_i	$S_1 = S_2 = M = 1$ $S_0 = S_3 = 0V$

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max	Any output except A = B	2.5	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max,				0.5	V
		I_{OH} = Max	+125°			0.45	V
V_{IK}	Input clamp voltage	V_{CC} = Min, $I_I = I_{IK}$				-1.2	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 5.5V	Mode input			1.0	mA
			$\overline{A}$ or $\overline{B}$ inputs			1.0	mA
			S inputs			1.0	mA
			Carry input			1.0	mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V	Mode input			50	µA
			$\overline{A}$ or $\overline{B}$ inputs			150	µA
			S inputs			200	µA
			Carry input			250	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.5V	Mode input			-2	mA
			$\overline{A}$ or $\overline{B}$ inputs			-6	mA
			S inputs			-8	mA
			Carry input			-10	mA
I_{OH}	High-level output current	V_{IH} = Min, V_I = Max, V_{OH} = 5.5V A = B only				250	µA
I_{OS}	Short-circuti output current[4]	V_{CC} = Max Any output except A = B		-40		-100	mA
I_{CC}	Supply current[5] (total)	V_{CC} = Max	Note 5a		120	220	mA
			Note 5b		120	220	mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			$C_L = 15pF$		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay C_n to C_{n+4}	M = 0V, Sum or Diff Mode see Waveform 2 and Tables I & II		10.5 10.5	ns ns
t_{PLH} t_{PHL}	Propagation delay C_n to $\overline{F}$ outputs	M = 0V, Sum or Diff Mode see Waveform 2 and Tables I & II		12 12	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ or $\overline{B}$ inputs to $\overline{G}$ output	$M = S_1 = S_2 = 0V$, $S_0 = S_3 = 4.5V$ Sum Mode, see Waveform 2 and Table I		12 12	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ or $\overline{B}$ inputs to $\overline{G}$ output	$M = S_0 = S_3 - 0V$, $S_1 = S_2 = 4.5V$ Diff Mode, see Waveform 3 and Table II		15 15	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ or $\overline{B}$ inputs to $\overline{P}$ output	$M = S_1 = S_2 = 0V$, $S_0 = S_3 = 4.5V$ Sum Mode, see Waveform 2 and Table I		12 12	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ or $\overline{B}$ inputs to $\overline{P}$ output	$M = S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$ Diff Mode, see Waveform 3 and Table II		15 15	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ or $\overline{B}_i$ inputs to $\overline{F}_i$ outputs	$M = S_1 = S_2 = 0V$, $S_0 = S_3 = 4.5V$ Sum Mode, see Waveform 2 and Table I		16.5 16.5	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ or $\overline{B}_i$ inputs to $\overline{F}_i$ outputs	$M = S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$ Diff Mode, see Waveform 3 and Table II		20 22	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ or $\overline{B}_i$ inputs to $\overline{F}_i$ outputs	M = 4.5V, Logic Mode see Waveform 2 and Table III		20 22	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ or $\overline{B}$ inputs to C_{n+4} output	$M = 0V$, $S_0 = S_3 = 4.5V$, $S_1 = S_2 = 0V$ Sum Mode, see Waveform 1 and Table I		18.5 18.5	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ or $\overline{B}$ inputs to C_{n+4} outputs	$M = 0V$, $S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$ Diff Mode, see Waveform 4 and Table II		23 23	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ or $\overline{B}$ inputs to A = B output	$M = S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$ Diff Mode, see Waveform 3 and Table II		23 30	ns ns

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$[6]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			$C_L = 50pF$		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay C_n to C_{n+4}	M = 0V, Sum or Diff Mode see Waveform 2 and Tables I & II		13.0 13.0	ns ns
t_{PLH} t_{PHL}	Propagation delay C_n to $\overline{F}$ outputs	M = 0V, Sum or Diff Mode see Waveform 2 and Tables I & II		14.0 14.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ or $\overline{B}$ inputs to $\overline{G}$ output	$M = S_1 = S_2 = 0V$, $S_0 = S_3 = 4.5V$ Sum Mode, see Waveform 2 and Table I		14.0 14.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ or $\overline{B}$ inputs to $\overline{G}$ output	$M = S_0 = S_3 - 0V$, $S_1 = S_2 = 4.5V$ Diff Mode, see Waveform 3 and Table II		18.0 18.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ or $\overline{B}$ inputs to $\overline{P}$ output	$M = S_1 = S_2 = 0V$, $S_0 = S_3 = 4.5V$ Sum Mode, see Waveform 2 and Table I		14.0 14.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ or $\overline{B}$ inputs to $\overline{P}$ output	$M = S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$ Diff Mode, see Waveform 3 and Table II		18.0 18.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ or $\overline{B}_i$ inputs to $\overline{F}_i$ outputs	$M = S_1 = S_2 = 0V$, $S_0 = S_3 = 4.5V$ Sum Mode, see Waveform 2 and Table I		20.0 20.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ or $\overline{B}_i$ inputs to $\overline{F}_i$ outputs	$M = S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$ Diff Mode, see Waveform 3 and Table II		23.0 25.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ or $\overline{B}_i$ inputs to $\overline{F}_i$ outputs	M = 4.5V, Logic Mode see Waveform 2 and Table III		24.0 26.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ or $\overline{B}$ inputs to C_{n+4} output	$M = 0V$, $S_0 = S_3 = 4.5V$, $S_1 = S_2 = 0V$ Sum Mode, see Waveform 1 and Table I		23.0 23.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ or $\overline{B}$ inputs to C_{n+4} outputs	$M = 0V$, $S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$ Diff Mode, see Waveform 4 and Table II		27.0 26.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ or $\overline{B}$ inputs to A = B output	$M = S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$ Diff Mode, see Waveform 3 and Table II		27.0 33	ns ns

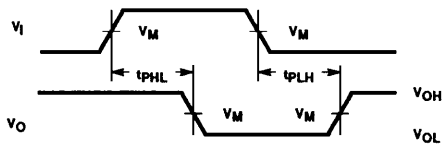
AC ELECTRICAL CHARACTERISTICS T_A = -55°C and +125°C, V_{CC} = 5.0V[6]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay C_n to C_{n+4}	M = 0V, Sum or Diff Mode see Waveform 2 and Tables I & II		14.5 14.5	ns ns
t_{PLH} t_{PHL}	Propagation delay C_n to $\overline{F}$ outputs	M = 0V, Sum or Diff Mode see Waveform 2 and Tables I & II		16.0 16.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ or $\overline{B}$ inputs to $\overline{G}$ output	M = S_1 = S_2 = 0V, S_0 = S_3 = 4.5V Sum Mode, see Waveform 2 and Table I		16.0 16.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ or $\overline{B}$ inputs to $\overline{G}$ output	M = S_0 = S_3 - 0V, S_1 = S_2 = 4.5V Diff Mode, see Waveform 3 and Table II		20.0 20.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ or $\overline{B}$ inputs to $\overline{P}$ output	M = S_1 = S_2 = 0V, S_0 = S_3 = 4.5V Sum Mode, see Waveform 2 and Table I		16.0 16.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ or $\overline{B}$ inputs to $\overline{P}$ output	M = S_0 = S_3 = 0V, S_1 = S_2 = 4.5V Diff Mode, see Waveform 3 and Table II		20.0 20.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ or $\overline{B}_i$ inputs to $\overline{F}_i$ outputs	M = S_1 = S_2 = 0V, S_0 = S_3 = 4.5V Sum Mode, see Waveform 2 and Table I		23.0 23.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ or $\overline{B}_i$ inputs to $\overline{F}_i$ outputs	M = S_0 = S_3 = 0V, S_1 = S_2 = 4.5V Diff Mode, see Waveform 3 and Table II		26.0 28.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ or $\overline{B}_i$ inputs to $\overline{F}_i$ outputs	M = 4.5V, Logic Mode see Waveform 2 and Table III		26.0 28.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ or $\overline{B}$ inputs to C_{n+4} output	M = 0V, S_0 = S_3 = 4.5V, S_1 = S_2 = 0V Sum Mode, see Waveform 1 and Table I		25.0 25.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ or $\overline{B}$ inputs to C_{n+4} outputs	M = 0V, S_0 = S_3 = 0V, S_1 = S_2 = 4.5V Diff Mode, see Waveform 4 and Table II		29.0 29.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ or $\overline{B}$ inputs to A = B output	M = S_0 = S_3 = 0V, S_1 = S_2 = 4.5V Diff Mode, see Waveform 3 and Table II		29.0 36.0	ns ns

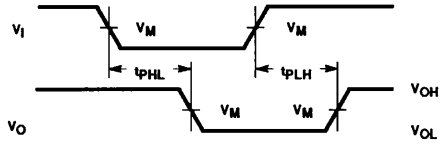
NOTES:

2. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
3. All typical values are at V_{CC} = 5V, T_A = 25°C.
4. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
5. I_{CC} is measured with the following conditions:
   a. S_0 through S_3, M, and A inputs are $\geq$ 4.0V, other inputs grounded, all outputs open.
   b. S_0 through S_3 and M inputs are $\geq$ 4.0V, other inputs grounded, all outputs open.
6. These parameters are guaranteed, but not tested.

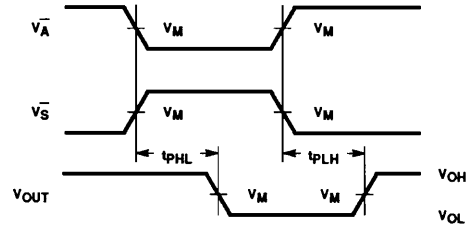
AC WAVEFORMS



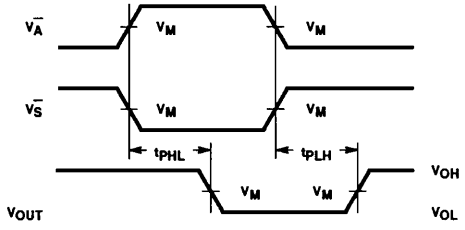
Waveform 1



Waveform 2



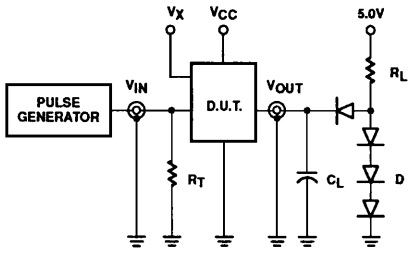
Waveform 3



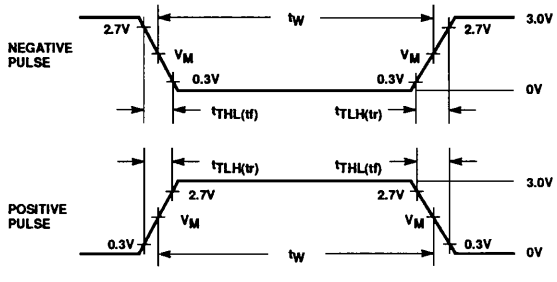
Waveform 4

NOTE: V_M = 1.5V

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54SXXX	280kΩ	1.5V	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.